Application Note

Stability Analysis and Design of Internally-Compensated Peak Current Mode TPS62933 - Part I: How to Select the Output Capacitor

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ABSTRACT

Peak current mode (PCM) control is widely used in buck controllers and converters due to its advantages as good dynamic performance and easy compensation. TPS62933 is a peak current mode buck converter with 3.8- to 30-V input voltage and max 3-A output current. To simplify the BOM and save the application design effort, the internal compensation is integrated in the device. For common applications, the inductance and capacitance range in the recommended table can be used to guide the component selection. The stability analysis and design methods for special application designs with large or small output capacitance are explored in this application note.

The method proposed in this application note can only be used as a reference material. Due to the simplification in deduction and non-ideal factors in reality, the calculated results will differ from the bench test. Also, the application design method for a converter with a feedforward capacitor is not included in this application note.

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Trademarks

1 Introduction

Peak current mode control is widely used in buck controllers and converters due to its advantages for good dynamic performance and easy compensation. Most peak current mode converters have a COMP pin and customers can implement type 2 or type 3 external compensation by adjusting external resistors and capacitors. In recent years, internal compensation attracts more and more attention to reduce solution size and achieve simple application design. The TPS62933 is a buck converter with an internally compensated peak current mode that supports 3.8- to 30-V input voltage and maximum 3-A output current. The device has superior features like low I_Q and a wide output voltage range. Compared to the conventional PCM devices, it does not need external resistors or capacitors for compensation setting, but the stability restriction limits the range of inductance and output capacitance.

For common applications, components can be selected based on the recommended table and implement fast design for application. For special application design to choose large output capacitance or small output capacitance, a stability design method is proposed in this application report. The application with a feedforward capacitor is not included in the analysis.

2 Loop Response of Peak Current Mode Converter

Figure 2-1 shows the schematic of a PCM buck converter. A type 2 compensation is used to ensure the stability of the converter.

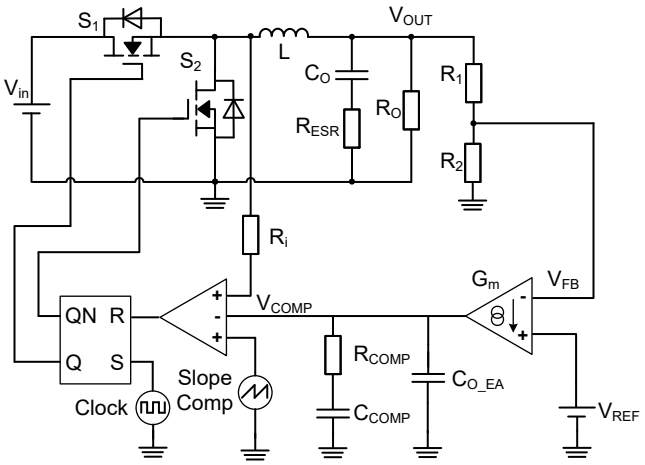


Figure 2-1. Simplified Schematic of PCM Buck Converter

The loop response model of PCM buck converters is introduced in the application report[(2)]. Figure 2-2 shows the bode plot.

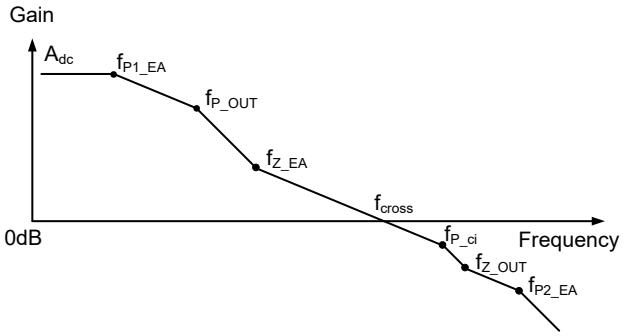


Figure 2-2. Bode Plot of PCM Buck Converter Open Loop Response

In the loop response of PCM converters, the DC gain is affected by output current.

- f_{P1_EA}, f_{P2_EA} and f_{Z_EA} are the frequencies of poles and zero generated by the type2 compensation
- f_{P1_EA} is the initial pole at low frequency to boost DC gain for improving output voltage accuracy
- f_{Z_EA} is a zero to enlarge bandwidth and boost phase margin
- f_{P2_EA} is a high-frequency pole to increase gain margin and attenuate high frequency noise

In TPS62933, the DC gain, f_{P1_EA}, f_{P2_EA}, and f_{Z_EA} are all determined by the device internal compensation circuit, which is expressed as Equation 1 and Equation 2.

$$A_{DC}=\frac{352000}{I_{OUT}} \tag{1}$$

where

- I_{OUT} is the output current of the converter

$$\begin{cases} f_{P1\_EA}=1.2Hz \\ f_{P2\_EA}=275kHz \\ f_{Z\_EA}=10.6kHz \end{cases} \tag{2}$$

- f_{Z_OUT} and f_{P_OUT} are zero and pole introduced by the output capacitor and load

For the application with all MLCC or small ESR output capacitors, f_{Z_OUT} is at high-frequency range and has limited effects on converter stability.

$$f_{Z\_OUT}=\frac{1}{2\pi R_{ESR}C_O} \tag{3}$$

$$f_{P\_OUT}=\frac{1}{2\pi(R_{ESR}+R_O)C_O} \tag{4}$$

where

- C_O is the output capacitance
- R_{ESR} is the ESR of output capacitors
- R_O is the output resistor, which equals to V_{OUT} / I_{OUT}.

f_{P_ci} is a pole introduced by the inside current loop and related with device slope compensation. Its expression for TPS62933 is shown as Equation 5.

$$f_{P\_ci}=\frac{V_{IN}f_{sw}}{\pi(4356000L+V_{IN}-2V_O)} \tag{5}$$

3 Output Capacitance Upper Limit for Internally-Compensated PCM Buck Converter

1. Limits for –20 dB/dec at gain crossover frequency

For system loop stability, a –20 dB/dec slope near crossover frequency is ideal for loop gain, since that can normally bring sufficient phase margin[3].

Figure 2-2 shows the loop gain slope of the PCM converter changes from 0 to –20 dB/dec at the initial pole frequency, f_{P1_EA}. At pole f_{P_OUT}, the loop gain slope changes to –40 dB/dec. With the compensation of zero f_{Z_EA}, the gain slope becomes –20 dB/dec and the gain curve crosses 0 dB with this slope. That could bring sufficient phase margin for the converter.

Figure 3-1 (a) illustrates that the converter crossover frequency f_c becomes lower with reduced pole frequency f_{P_OUT}. If $f_c < f_{Z\_EA}$, the zero f_{Z_EA} is out of crossover frequency and loop gain crosses 0 dB with a –40 dB/dec slope. If these conditions occur, they may cause insufficient phase margin.

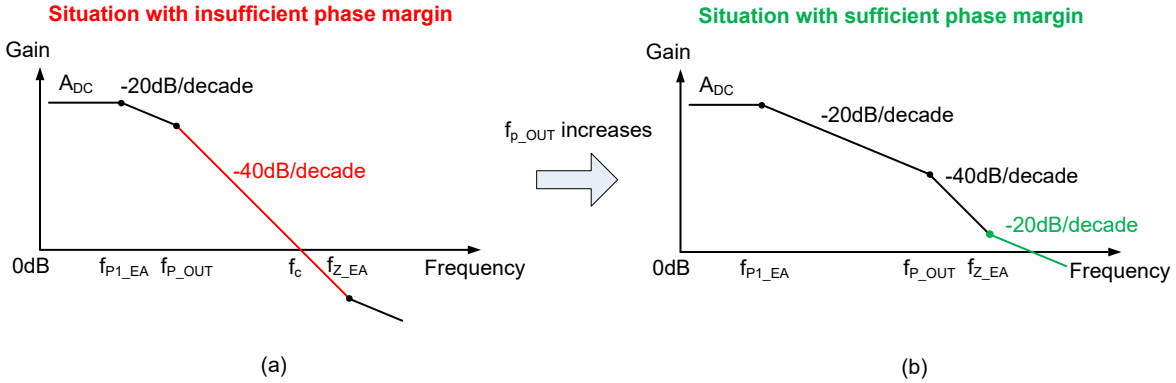


Figure 3-1. Loop Gain of TPS62933 Converter With Zero f_{Z_EA} (a) Out of Bandwidth (b) Inside Bandwidth

Equation 4 shows that pole f_{P_OUT} is inversely related with output capacitance C_O. Reducing C_O can make both f_{P_OUT} and f_c increase. As shown in Figure 3-1 (b), after increasing the pole frequency f_{P_OUT}, f_{Z_EA} could be smaller than the crossover frequency f_c and the loop gain crosses 0 dB with a –20 dB/dec slope. These conditions could normally ensure converter phase margin.

Based on the previous analysis, use Equation 6 to calculate the limitation for –20 dB/dec slope at gain crossover frequency:

$$f_c > f_{Z\_EA} \tag{6}$$

As Equation 2 shows, f_{Z_EA} is fixed at 10.6 kHz for TPS62933. To get the relation between output capacitance C_o and f_c, first calculate the relation between gain and frequency using Equation 7 and Equation 8.

$$\frac{20\lg(A_{DC})-20\lg(A_{P\_OUT})}{\lg(f_{P1\_EA})-\lg(f_{P\_OUT})}=-20\text{dB/decade} \tag{7}$$

$$\frac{20\lg(A_{P\_OUT})-0}{\lg(f_{P\_OUT})-\lg(f_c)}=-40\text{dB/decade} \tag{8}$$

where

- A_{P_OUT} is the loop gain at frequency f_{P_OUT}

Equation 7 and Equation 8 can be simplified as:

$$A_{P\_OUT}=\frac{A_{DC}f_{P1\_EA}}{f_{P\_OUT}} \tag{9}$$

$$f_c=f_{P\_OUT}\sqrt{A_{P\_OUT}}=\sqrt{f_{P\_OUT}A_{DC}f_{P1\_EA}} \tag{10}$$

With Equation 4, Equation 6, and Equation 10, the upper limit for output capacitance is calculated using Equation 11.

$$C_O<\frac{A_{DC}f_{P1\_EA}}{2\pi(R_{ESR}+R_O)\,f_{Z\_EA}^{\ 2}} \tag{11}$$

Substituting parameters in Equation 1 and Equation 2, the upper limit for TPS62933 is:

$$C_O<\frac{5.98\times10^{-4}}{I_{OUT}R_{ESR}+V_{OUT}} \tag{12}$$

2. **Limits for 45 degree phase margin**

Normally for a buck converter, a 45 degree phase margin can be achieved with –20 dB/dec slope at gain crossover frequency. But for a buck regulator with peak current-mode control, when a larger inductance is used, the frequency of the inner current loop pole f_{P_ci} will be lower and bring more phase drop at the gain crossover frequency. These conditions may cause a phase margin lower than 45 degrees, even with –20 dB/dec crossing. Therefore, the capacitance upper limit for a 45 degree phase margin is also deducted in this section.

Figure 3-2 is a bode plot of a PCM buck converter with –20 dB/dec crossing. f_{Z_OUT} and f_{P2_EA} are normally at very high frequency so their effects on phase margin at gain crossover frequency can be ignored at first. Pole f_{P1_EA} is at a very low frequency and brings about –90° phase drop at gain crossover frequency.

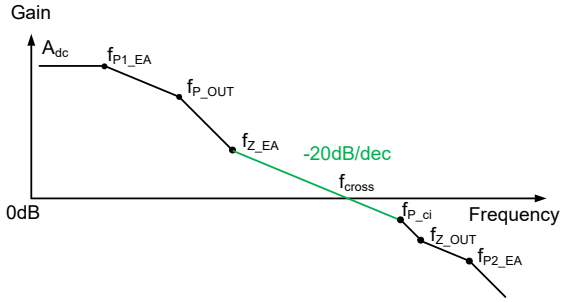


Figure 3-2. Bode Plot of PCM Buck Converter Open Loop Response

Next, calculate the phase margin using Equation 13. Equation 14 constitutes the limitation to make the phase margin larger than 45 degrees.

$$PM=180+Phase_{P1\_EA}(f_{cross})+Phase_{P\_OUT}(f_{cross})+Phase_{Z\_EA}(f_{cross})+Phase_{P\_ci}(f_{cross}) \tag{13}$$

$$PM=90+\tan^{-1}\left(\frac{f_{cross}}{f_{P\_OUT}}\right)+\tan^{-1}\left(\frac{f_{cross}}{f_{Z\_EA}}\right)+\tan^{-1}\left(\frac{f_{cross}}{f_{P\_ci}}\right)>45 \tag{14}$$

Calculate gain crossover frequency f_{cross} using Equation 15, Equation 16 and Equation 17, based on Figure 3-2.

$$\frac{20\lg(A_{DC})-20\lg(A_{P\_OUT})}{\lg(f_{P1\_EA})-\lg(f_{P\_OUT})}=-20dB/decade \tag{15}$$

$$\frac{20\lg(A_{P\_OUT})-20\lg(A_{Z\_EA})}{\lg(f_{P\_OUT})-\lg(f_{Z\_EA})}=-40dB/decade \tag{16}$$

$$\frac{20\lg(A_{Z\_EA})-0}{\lg(f_{Z\_EA})-\lg(f_{cross})}=-20dB/decade \tag{17}$$

Derive f_{cross} using equation Equation 18:

$$f_{cross}=\frac{A_{DC}f_{P1\_EA}f_{P\_OUT}}{f_{Z\_EA}} \tag{18}$$

Substituting Equation 1, Equation 2, and Equation 4 into Equation 18, f_{cross} is expressed with:

$$f_{cross}=\frac{6.35}{(I_{OUT}R_{ESR}+V_{OUT})C_O} \tag{19}$$

Substituting Equation 2, Equation 4, Equation 5, and Equation 19 into Equation 14 and ignoring ESR impacts, the upper limit for output capacitance for phase margin restriction is calculated using the following example equation:

```
(50*(111936*IOUT - 4460544))/(441013* IOUT *VOUT*(422400/ IOUT + (8954880000/ IOUT +
178421760000/ IOUT ^2 + (2500* VIN ^2* fsw ^2)/(24649*(4356000*L + VIN - 2* VOUT)^2) - (3180000*
VIN *fsw)/(157*(4356000*L + VIN - 2* VOUT)) + (84480000* VIN * fsw)/(157* IOUT *(4356000*L +
VIN - 2* VOUT)) - (267632640000* VIN * fsw)/(8321* IOUT ^2*(4356000*L + VIN - 2* VOUT)) +
(10560000* VIN ^2* fsw ^2)/(1306397* IOUT *(4356000*L + VIN - 2* VOUT)^2) + (11151360000* VIN
^2* fsw ^2)/(69239041* IOUT ^2*(4356000*L + VIN - 2* VOUT)^2) + 112360000)^(1/2) - (50* VIN *
fsw)/(157*(4356000*L + VIN - 2* VOUT)) - (105600* VIN * fsw)/(8321* IOUT *(4356000*L + VIN - 2*
VOUT)) + 10600))
```

Since the expression for output capacitance upper limit with phase margin restriction is very complicated, an example of how to use Microsoft® Excel® or MATLAB® for the calculation is introduced in Appendix A.

4 Output Capacitance Lower Limit for Internally-Compensated PCM Buck Converter

The chosen capacitance, C_O, cannot be too small. An output capacitance that is too small could cause worse load-transient performance and loop instability at the same time. Normally for a peak current-mode converter, the lower limit with loop stability is much smaller than the limit with the load-transient performance restriction. So the only method to derive the lower limit through load-transient restriction is introduced in this section.

To calculate the lower limit for output capacitance for a specified V_{OUT} overshoot and undershoot in load transient, see the *Output Capacitor Selection* section in the *TPS62933 3.8-V to 30-V, 3-A Synchronous Buck Converter in SOT583 Package* data sheet(1).

$$C_O > \frac{\Delta I_{OUT}}{f_{SW} \Delta V_{OUT} K} \left[(1-D)(1+K) + \frac{K^2}{12} (2-D) \right] \tag{20}$$

where

- $D = V_{OUT} / V_{IN}$, duty cycle of steady state
- ΔV_{OUT} is targeted output voltage change for load transient
- ΔI_{OUT} is output current change in load transient
- K is the ripple ratio of the inductor current ($\Delta I_L / I_{OUT\_MAX}$)

If the C_O lower limit calculated from Equation 20 is bigger than the upper limit from Equation 12, there is no available output capacitance range with limitation. A feedforward capacitor must be used to increase phase margin at this condition, which is introduced in the *Stability Analysis and Design of Internally-Compensated Peak Current Mode TPS62933 - Part II: How to Select the Feedforward Capacitor* application note.

5 Design Example and Experimental Validation for TPS62933

Figure 5-1 illustrates the conclusion of the application design method.

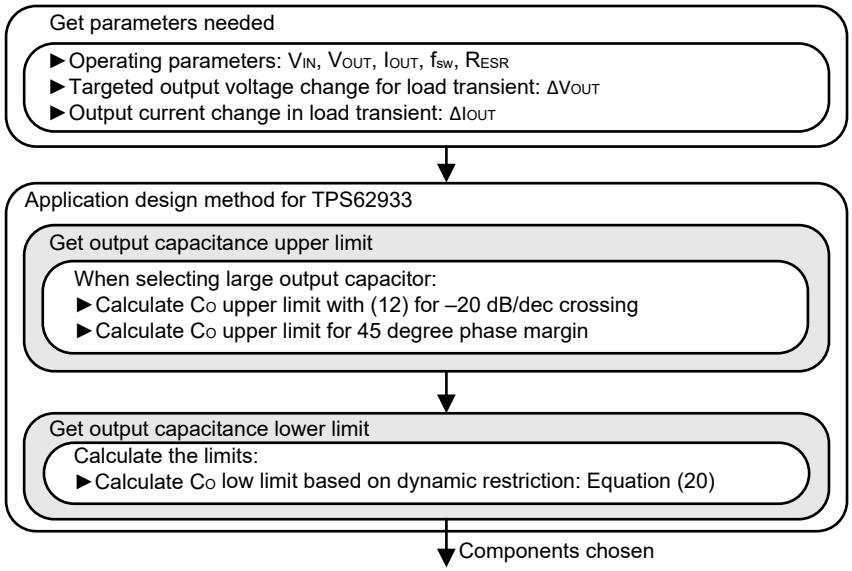


Figure 5-1. TPS62933 Application Design Flow Chart

Take the typical application as an example: V_{in} = 24 V, V_{out} = 5 V, I_{out} = 3 A, f_{sw} = 1200 kHz.

Based on the inductor selection method introduced in the data sheet, choose an inductance of 3.3 µH for the application.

Here the upper limit of output capacitance is verified. The C_O upper limit of 119.6 µF is obtained with Equation 12 for –20 dB/dec crossing and also C_O upper limit of 131 µF for 45 degree phase margin restriction.

Note here the calculated C_O is the effective value.

The example is validated on the EVM. The C3216X5R1V226M160AC (22 µF) and CGA5L1X7R1H106K160AC (10 µF) are selected here as C_O. When biased at 5 V, the effective of C3216X5R1V226M160AC is about 13.2 µF and the effective of CGA5L1X7R1H106K160AC is about 9.4 µF.

The upper output capacitance limit is verified with choosing C_O = 8 × 22 µF. The effective capacitance is about 105.6 µF and slightly lower than the upper limit of 119.6 µF. Figure 5-2 shows the phase margin is 45.827 degrees.

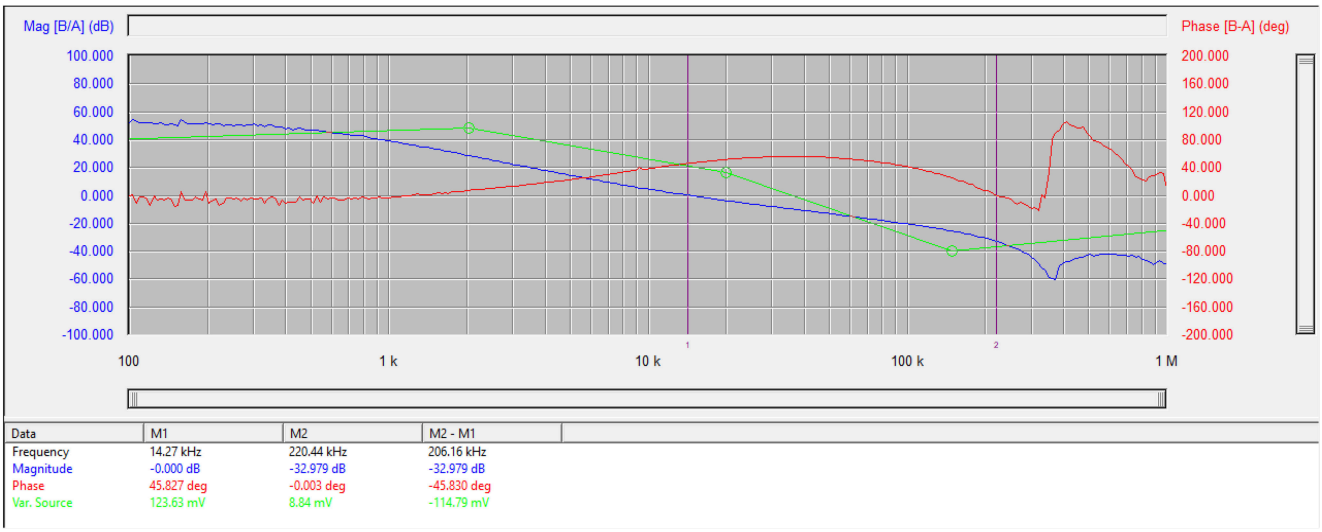


Figure 5-2. Bode Plot for Output Capacitance Lower Limit Validation

The test results in Figure 5-2 show the effectiveness of the proposed method. See more validation results in Appendix A.

6 Summary

This application note presents a method for selecting an output capacitor for an internally-compensated peak current mode converter, TPS62933. The limitation for output capacitance is derived based on restriction of loop stability and load transient performance. In conclusion, the proposed methods are validated on the EVM.

7 References

1. Texas Instruments, *TPS62933 3.8-V to 30-V, 3-A Synchronous Buck Converter in SOT583 Package* Data Sheet
2. Texas Instruments, *Loop Response Considerations in Peak Current Mode Buck Converter Design* Application Report
3. Franklin, G. F., Powell, J. D., and Emami-Naeini, A. F. (2019). *Feedback Control of Dynamic Systems*, 8th Edition. Pearson.

A Validation and Calculating the Output Capacitance Upper Limit

This appendix contains the *table of validation results* for the methods proposed in this document and examples using Excel or MATLAB to calculate the output capacitance upper limit.

Table A-1. Validation of Inductance Limit and Capacitance Upper Limit

V_{IN} (V)	V_{OUT} (V)	f_{SW} (kHz)	L_{choose}(µH)	High Limit C_O(µF) Without C_{ff}	C_{choose}(µF)	PM_{bench}
24	5	500	6.8	106	7 × 22 µF ($C_{effective}$: 92.4 µF)	45.034
24	5	1200	3.3	119.6	8 × 22 µF ($C_{effective}$: 105.6 µF)	45.827
24	12	500	12	40.7	7 × 22 µF ($C_{effective}$: 34.475 µF)	46.153

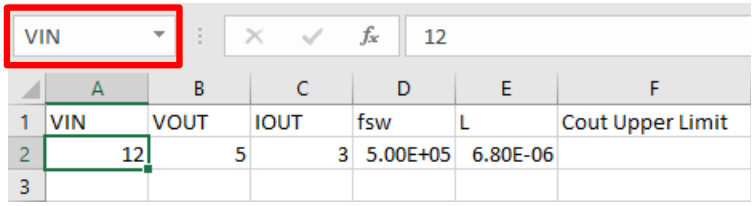
Note

For V_{OUT} = 12-V application, if C_O is bigger than the high limit, add the feedforward capacitor C_{ff} to the boost phase margin. For C_{ff} selection, see *Stability Analysis and Design of Internally-Compensated Peak Current Mode TPS62933 - Part II: How to Select the Feedforward Capacitor* application note.

If Microsoft Excel is used to calculate the output capacitance upper limit, first input parameters using the following format:

	A	B	C	D	E	F
1	VIN	VOUT	IOUT	fsw	L	Cout Upper Limit
2	12	5	3	5.00E+05	6.80E-06	
3						

- Change the variable name of value A2-E2 to the name A1-E1.



- Input the following equation in F2. Input "=" first, then copy and paste the expression of output capacitance upper limit for 45 degree phase margin:

```
(50*(111936*IOUT - 4460544))/(441013* IOUT *VOUT*(422400/ IOUT + (8954880000/ IOUT +
178421760000/ IOUT ^2 + (2500* VIN ^2* fsw ^2)/(24649*(4356000*L + VIN - 2* VOUT)^2) - (3180000*
VIN *fsw)/(157*(4356000*L + VIN - 2* VOUT)) + (84480000* VIN * fsw)/(157* IOUT *(4356000*L +
VIN - 2* VOUT)) - (267632640000* VIN * fsw)/(8321* IOUT ^2*(4356000*L + VIN - 2* VOUT)) +
(10560000* VIN ^2* fsw ^2)/(1306397* IOUT *(4356000*L + VIN - 2* VOUT)^2) + (11151360000* VIN
^2* fsw ^2)/(69239041* IOUT ^2*(4356000*L + VIN - 2* VOUT)^2) + 112360000)^(1/2) - (50* VIN *
fsw)/(157*(4356000*L + VIN - 2* VOUT)) - (105600* VIN * fsw)/(8321* IOUT *(4356000*L + VIN - 2*
VOUT)) + 10600))
```

	A	B	C	D	E	F
1	VIN	VOUT	IOUT	fsw	L	Cout Upper Limit
2	12	5	3	5.00E+05	6.80E-06	8.53334E-05
3						

- Now the output capacitance upper limit for 45 degree phase margin can be calculated with Excel.

If MATLAB is used, implement the following code (as an example):

```
VIN=12;
VOUT=5;
IOUT=3;
fsw=500e3;
L=6.8e-6;
Cout_upper=(50*(111936*IOUT - 4460544))/(441013* IOUT *VOUT*(422400/ IOUT + (8954880000/ IOUT +
178421760000/ IOUT ^2 + (2500* VIN ^2* fsw ^2)/(24649*(4356000*L + VIN - 2* VOUT)^2) - (3180000*
VIN *fsw)/(157*(4356000*L + VIN - 2* VOUT)) + (84480000* VIN * fsw)/(157* IOUT *(4356000*L +
VIN - 2* VOUT)) - (267632640000* VIN * fsw)/(8321* IOUT ^2*(4356000*L + VIN - 2* VOUT)) +
(10560000* VIN ^2* fsw ^2)/(1306397* IOUT *(4356000*L + VIN - 2* VOUT)^2) + (11151360000* VIN ^2*
fsw ^2)/(69239041* IOUT ^2*(4356000*L + VIN - 2* VOUT)^2) + 112360000)^(1/2) - (50* VIN * fsw)/
(157*(4356000*L + VIN - 2* VOUT)) - (105600* VIN * fsw)/(8321* IOUT *(4356000*L + VIN - 2* VOUT)) +
10600))
```

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