Functional Safety Information

UCC2808A-xQ1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview

This document contains information for UCC2808A-xQ1 (UCC2808A-1Q1 and UCC2808A-2Q1 in SOIC 8 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

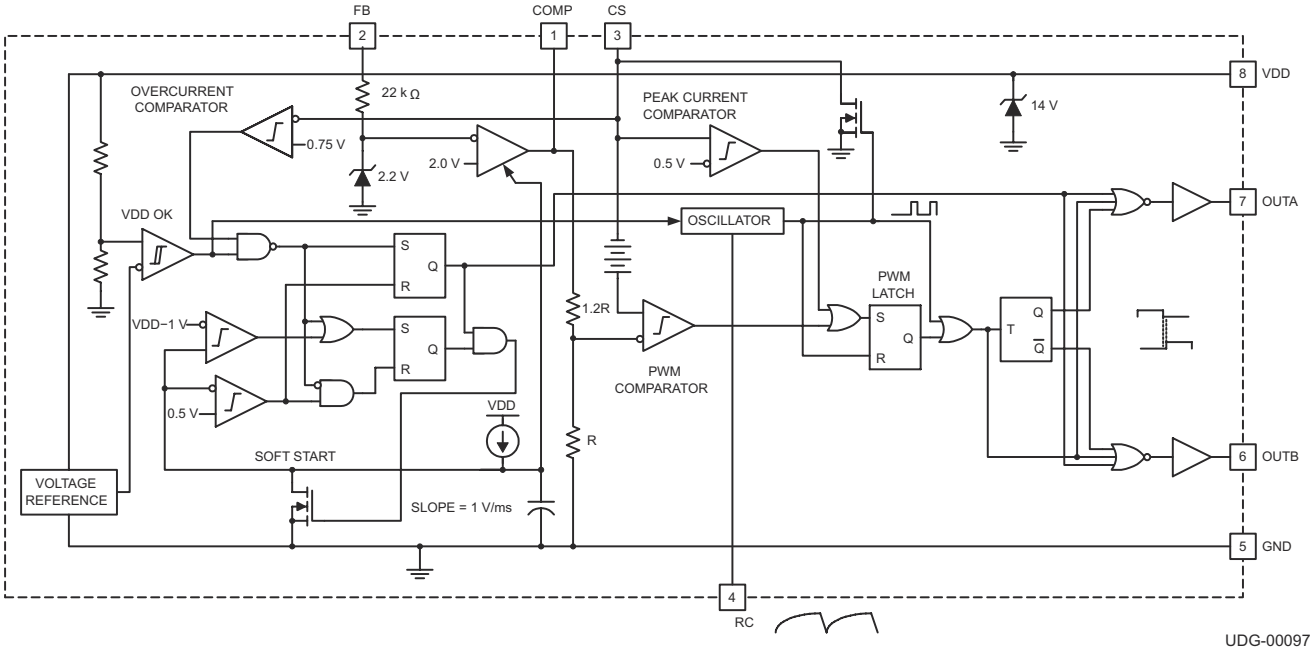

Figure 1-1. Functional Block Diagram

UCC2808A-xQ1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for UCC2808A-xQ1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	75	10
	150	11
	300	15
Die FIT rate	75	3
	150	4
	300	7
Package FIT rate	75	7
	150	7
	300	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 75mW, 150mW, 300mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC2808A-xQ1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTA and OUTB stuck low	15
OUTA and OUTB pulse width not as expected	17
OUTA stuck low	9.5
OUTA stuck high	9.5
OUTB stuck low	9.5
OUTB stuck high	9.5
System is unstable	7
No effect	23

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC2808A-xQ1(SOIC 8). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the UCC2808A-xQ1 (SOIC 8) pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC2808A-xQ1 data sheet.

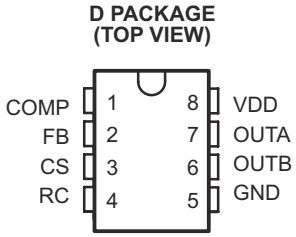

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The UCC2808A-xQ1 devices are connected according to the *Typical Application* diagram in the UCC2808A-xQ1 data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMP	1	No output.	B
FB	2	OUTA and OUTB operate with maximum duty cycle. The converter output cannot regulate.	C
CS	3	OUTA and OUTB operate with maximum duty cycle. The converter output cannot regulate.	C
RC	4	No output.	B
GND	5	No impact.	D
OUTB	6	OUTB stays low. Device damage is possible.	A
OUTA	7	OUTA stays low. Device damage is possible.	A
VDD	8	The device is not biased. No output.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMP	1	COMP pin voltage is unstable. OUTA and OUTB duty cycle is unstable. The converter output voltage oscillates.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB	2	COMP voltage stays high. OUTA and OUTB operate with maximum duty cycle. The converter output voltage cannot regulate.	C
CS	3	COMP voltage stays high. OUTA and OUTB operate with maximum duty cycle. The converter output voltage cannot regulate.	C
RC	4	No output.	B
GND	5	Converter operation is unpredictable. Device damage is possible.	A
OUTB	6	The converter operates as a forward converter. The converter output might not be regulated.	C
OUTA	7	The converter operates as a forward converter. The converter output might not be regulated.	C
VDD	8	The device is not biased.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
COMP	1	FB	The converter output loses regulation.	C
FB	2	CS	OUTA and OUTB operate with maximum duty cycle. The converter output loses regulation.	C
CS	3	RC	No output.	B
RC	4	N/A	N/A	N/A
GND	5	OUTB	OUTB stays low. Device damage is possible.	A
OUTB	6	OUTA	OUTA and OUTB stay low. Device damage is possible.	A
OUTA	7	VDD	OUTA stays high. Device damage is possible	A
VDD	8	N/A	N/A	N/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMP	1	OUTA and OUTB operate with maximum duty cycle. Device damage is possible.	A
FB	2	OUTA and OUTB stay low. Device damage is possible.	A
CS	3	OUTA and OUTB stay low. Device damage is possible.	A
RC	4	OUTA and OUTB stay low. Device damage is possible.	A
GND	5	The device is not biased. OUTA and OUTB stay low.	B
OUTB	6	OUTB stays high. Device damage is possible.	A
OUTA	7	OUTA stays high. Device damage is possible.	A
VDD	8	No effect.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2021) to Revision A (June 2025) **Page**

- Updated format and language to the latest functional safety template and TI writing standards..... 2
- Updated the *Die Failure Modes and Distribution* table..... 4
- Added the *Pin Failure Mode Analysis* section and contents..... 5

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