Application Report
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Minimize On-Time-Jitter and Ripple by Optimizing Compensation

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ABSTRACT

The TPS546D24A family of synchronous buck converters operate in continuous conduction mode (CCM) under all load conditions. The compensation components are integrated into each device, and programmable via the PMBus™ command or with the external pin MSEL1 resistor values to select pre-set values based on switching frequency and output LC filters. Noise in the current loop can affect jitter and ripple, and when designers require low output ripple and minimal on-time jitter, optimizing the voltage and current loop gain improves performance.

Table 1. Pin-Compatible TPS546D24A Family of Devices

Part Number	Output Current
TPS546D24A	40A
TPS546B24A	20A
TPS546A24A	10A

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Trademarks

PMBus is a trademark of SMIF, Inc.
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1 Introduction

The devices use an average current-mode control architecture with independently programmable current error integration and voltage error integration loops. This architecture provides similar performance to peak current-mode control without restricting the minimum on-time or minimum-off time control, allowing the gain selection of the current loop to effectively set the slope compensation. Consider the following suggestions to reduce jitter and improve output voltage ripple.

Table 2. Table of Terms

Description	Symbol
Current loop gain	GMI*RVI
Voltage loop gain	GMV*RVV
Voltage loop integrating capacitor	CZV
Current loop integrating capacitor	CZI
Voltage loop filter capacitor	CPV
Current loop filter capacitor	CPI

2 Reduce Current Loop Gain: GMI*RVI

- Reduce current loop gain to reduce impact of noise in the current loop.
- Using a lower GMI gives some improvement even if the product of GMI*RVI is kept the same. Use either 25 µS or 50 µS. Consider using 50 µS to help with the placement of the pole from CPI. Higher GMI allows lower RVI and larger CPI for the same pole location.
- Set the ILOOP gain set to target an ILOOP crossover near 1/4th the switching frequency (fsw) or lower. Consider compensation which gives an estimated ILOOP crossover below the VLOOP crossover. Only set the ILOOP crossover < VLOOP crossover if you measure the bode plot to ensure sufficient phase margin.

3 Increase Voltage Loop Gain: GMV*RVV

- Increase voltage loop gain so the voltage loop can react to noise from the current loop.
- When maximizing the VLOOP gain, consider increasing the GMV to reduce the required RVV resistor. This will help push the pole from CPV to a higher frequency.
- Again, consider trying to set the VLOOP crossover near or above the estimated ILOOP crossover.

4 Adjusting Capacitance Values

- Minimize **CZV** capacitance to increase low frequency gain of the voltage loop.
- Based on measurements, it appears most of the noise appearing on the output is <10 kHz, and increasing the low frequency gain may help. However, this does not seem to have a significant effect in all cases.
- To start out, try choosing **CZV** capacitance to target a zero at VLOOP fco/4.
- Choose **CZI** capacitance to the target ILOOP fco/4. However, it will not have much impact on the low frequency ripple.
- Minimize **CPV** capacitance to keep the pole it creates well-above the VLOOP fco, but keep some capacitance to help filter any high frequency noise.
- Keep **CPI** capacitance small, but try adjacent values. Start out selecting this capacitor to place the pole near fsw/2 to give the best balance between phase margin and jitter.

5 Other Suggestions

Reducing VDD5 to 4.1 V can reduce the ripple, but with the trade-off of some additional power loss and lower efficiency.

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