

# Convert UCC28064A EVM to Higher Switching Frequency Using UCC28065

## ABSTRACT

Interleaved transition mode PFC is a popular topology in many applications due to its high efficiency and smaller EMI filter size. To improve the power density of the design, reducing the Boost inductor height, designers need to increase the switching frequency. The new generation interleaved transition mode PFC controller, UCC28065, doubles the switching frequency capability compared with its previous generation devices and makes it a more suitable device for high-frequency designs. In this application note, the main differences between the UCC28065 and UCC28064A devices are discussed in detail. A summary of how to convert the UCC28064A EVM to evaluate the UCC28065 device is presented.

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## 1 Introduction

The interleaved transition mode (TM) Power Factor Correction (PFC) has been implemented in different applications, including digital TVs, personal computers, and many other applications. This topology allows power supply designers to use the transition mode PFC to a higher power level, while maintaining a similar input current ripple as a continuous conduction mode (CCM) PFC. This provides the benefits of higher efficiency, ease of low profile design, lower system cost, as well as better thermal design. During recent years, TI has released a family of interleaved TM PFC controllers including [UCC28060](#), [UCC28061](#), [UCC28063A](#), and [UCC28064A](#). This series of devices address different aspects of the design, for better THD, lower audible noise, or better light load efficiency.

Other than these performance improvements, the recent design trend is to achieve a higher power density or further reduction on the converter profile (height). To achieve this, the most straightforward method is to operate the PFC at a higher switching frequency. This allows the converter to use a lower value Boost inductor, which means a smaller inductor size, lower overall profile, or both.

A new generation device, the UCC28065, is introduced to enable doubling or tripling the switching frequency of the current design. This helps to reduce the inductor size, improve the design profile and power density, while maintaining high efficiency and high power factor performance. In this paper, the differences between the UCC28065 device and its previous generation device UCC28064A are discussed in detail. This application note also shows a simple method to convert the UCC28064A EVM ([UCC28064EVM\\_004](#)) to a higher switching frequency design using the UCC28065 device.

## 2 TM PFC Operating With Higher Switching Frequency

The TM PFC operates in the transition mode (boundary of discontinuous conduction mode and continuous conduction mode) to eliminate the PFC diode reverse recovery issue. This allows the use of lower cost PFC diodes, reducing the system cost and improving EMI.

### 2.1 TM PFC Operation Principle

Ideally, in each switching cycle, the TM PFC inductor current starts from zero. When the Boost switch turns on, the inductor current rises linearly with the rate determined by the input voltage and inductor value. After the Boost switch turns off, the inductor current reduces linearly, with the rate determined by the difference between the input and output voltage, and the inductor value. Given the inductor current is a perfect triangle, its average value is half of its peak value.

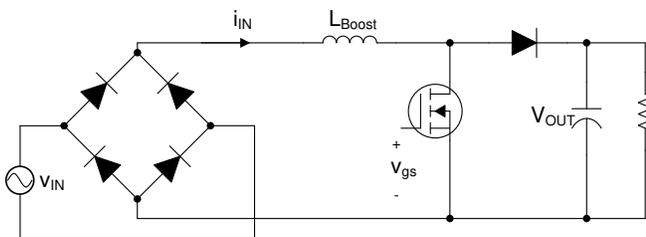


Figure 1. Transition Mode PFC Diagram

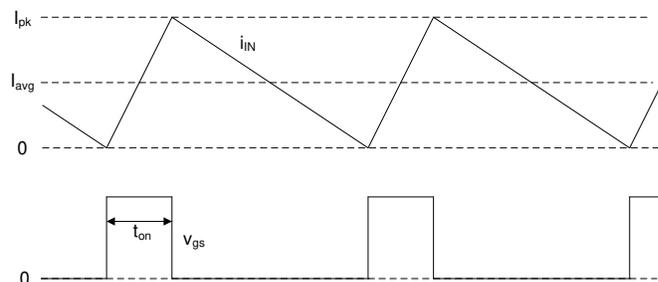


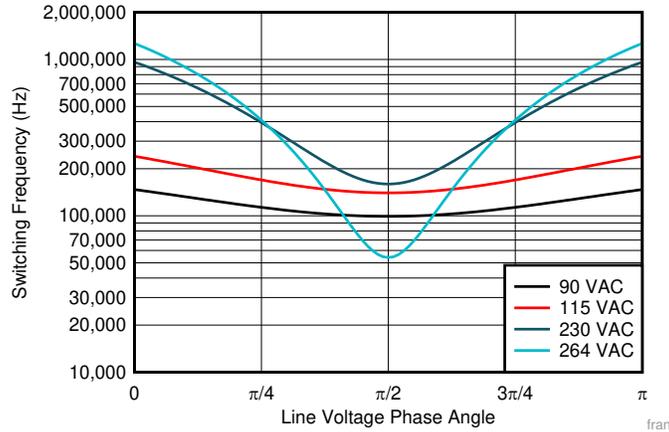
Figure 2. TM PFC Key Waveforms

According to [Equation 1](#), if the on time is kept constant along a line cycle (constant on-time control), the average inductor current is proportional to the input voltage and perfect PFC can be achieved.

$$I_{avg} = \frac{1}{2} I_{pk} = \frac{1}{2} \frac{V_{IN}}{L_{Boost}} t_{on} \tag{1}$$

## 2.2 Switching Frequency Clamping

Due to the transition mode operation, the switching frequency of the PFC is not a fixed value. It changes with the input voltage and output load. Generally, the switching frequency is higher when the load becomes lighter or the input voltage becomes higher. As Figure 3 shows, the theoretical derived switching frequency changes with different line voltages.



**Figure 3. Theoretical Switching Frequencies of TM PFC for Different Line Voltages**

It can be seen that the switching frequency gets much higher when the line voltage is zero crossing, compared with the switching frequency at the peak of the line. Also, the switching frequency becomes much higher at lighter loads, compared with the switching frequency at heavier loads at the same line voltage due to the smaller inductor current.

To prevent the excessive switching frequency, which could result in excessive switching loss, the UCC28064A implements a maximum switching frequency clamping, or a minimum switching period clamping. The controller monitors the switching frequency of the Boost switch, when the ZCD signal arrives before the minimum period expires, the ZCD signal is ignored and the controller waits for the next ZCD signal after the minimum period expires. The operation of this frequency clamping is illustrated in Figure 4.

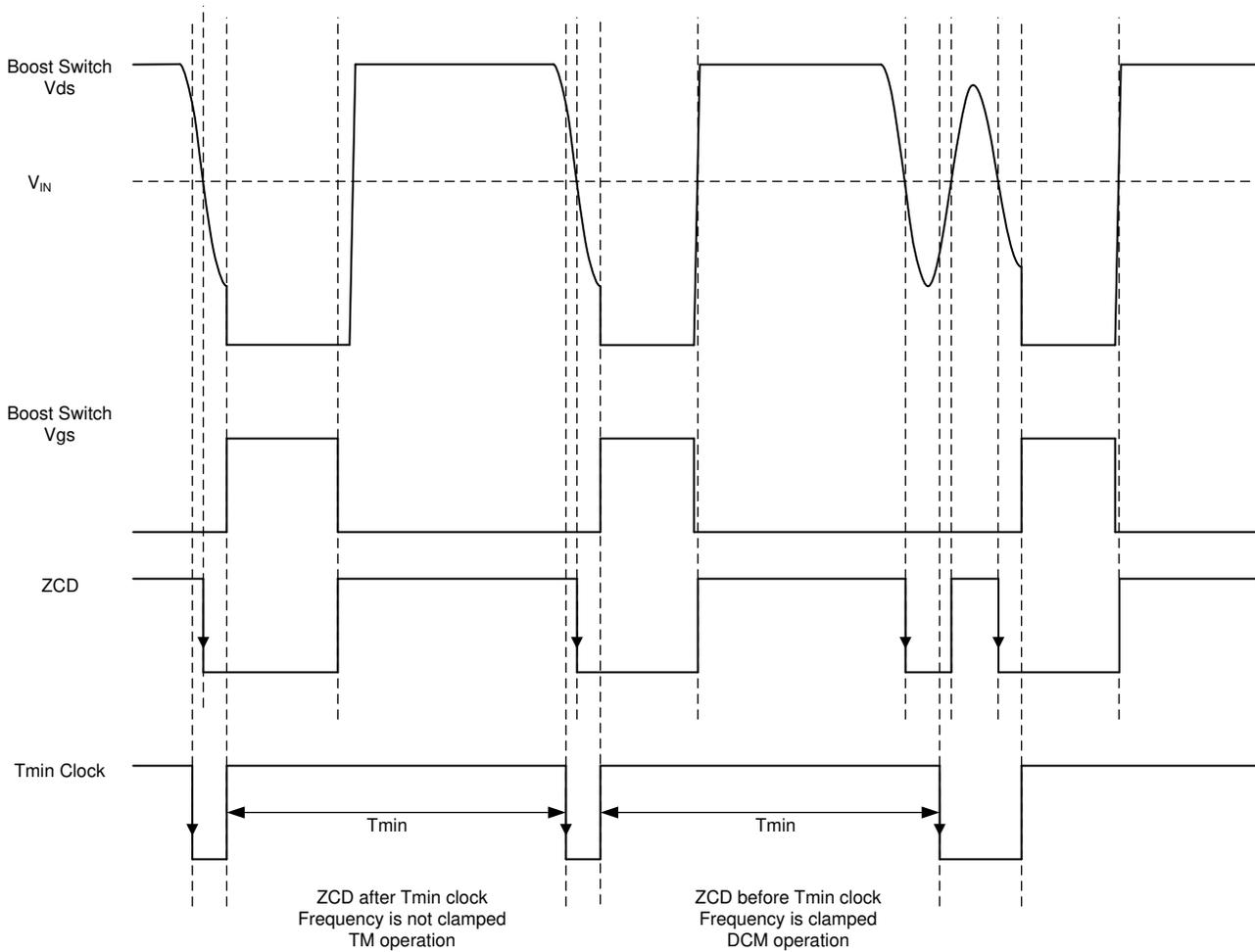


Figure 4. TM PFC Operates in Frequency Clamp

The minimum period of UCC28064A is defined as Equation 2 and is illustrated in Figure 5.

$$T_{min} = \frac{16C_t V_t}{5 \left( I_2 - \frac{1}{8} \frac{V_{TSET}}{R_{TSET}} \right)} \quad (2)$$

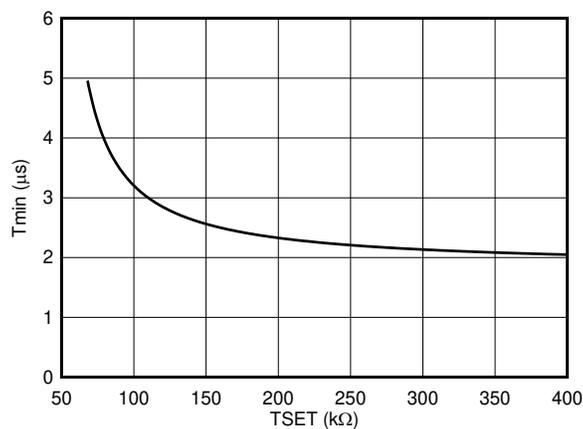


Figure 5. Minimum Period of UCC28064A for Different TSET Resistor Values

In this equation,  $V_{TSET}$  is 2.63 V,  $C_i$  is 1.0087 pF,  $I_2$  is 7.66  $\mu$ A, and  $V_i$  is 4.34 V (These are IC internal parameters). Based on this equation, for the largest recommended TSET pin resistor value of 400 k $\Omega$ , the minimum period is 2.05  $\mu$ s, which is equivalent to a switching frequency of about 500 kHz.

For a traditional design with UCC28064A or earlier generation devices, the minimum switching frequency is typically around 50 kHz. This frequency is reached at the peak of the line cycle at the lowest AC input voltage and full load. With such a low switching frequency design, the frequency clamping is always above the maximum switching frequency the converter demands.

With the demand of higher power density and lower profile, the switching frequency needs to be higher so that the PFC inductor size can be reduced. Equation 3 shows the relationship between the Boost inductor value and switching frequency. Because the input, output voltage, and the load are the design targets, while the inductor current and the RMS current remain the same regardless of the switching frequency, the Boost inductor size is purely determined by the switching frequency selection. To significantly shrink the inductor size, the switching frequency needs to be significantly increased. Therefore, the frequency clamp of the UCC28064A device also needs to be increased to meet the high-frequency design requirement.

$$L_{Boost} = \frac{V_{IN}^2 (V_{OUT} - \sqrt{2}V_{IN})}{\frac{P_{OUT}}{\eta} V_{OUT} f_{SW}} \tag{3}$$

### 2.3 Zero Crossing Compensation

As discussed earlier, the constant on-time control gives perfect PFC, if the inductor current starts from and returns to zero in each switch cycle. In reality, due to the Boost switch parasitic capacitor, the inductor current flows negatively in each switching cycle to achieve valley switching. This negative current adds an offset to the average current and causes zero crossing distortion. Often this is observed as a flat current duration at the zero crossing. To compensate the zero crossing distortion and improve the input current THD performance, the zero crossing compensation (ZCC) is implemented in the UCC28064A and its earlier generations. The principle is to increase the Boost switch on time, when the line voltage is zero crossing, to compensate the offset caused by the negative current. Since the negative current becomes much less a problem when the input voltage instantaneous value is higher, the compensation is only implemented at the input line voltage zero crossing. The extra on time is shown in the data sheet typical characteristic curves. The  $T_{ZCC}$  of UCC28064A at different TSET resistor values are shown in Figure 6.

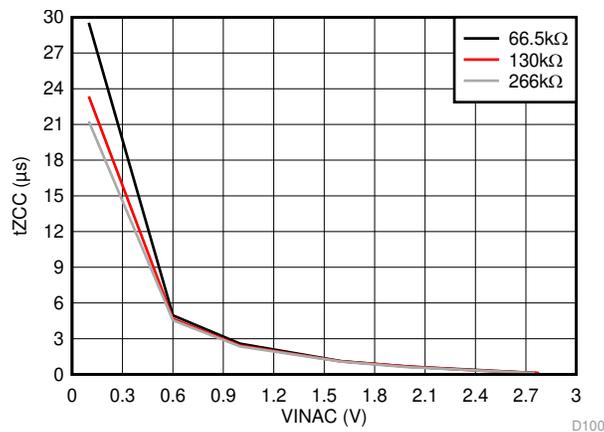


Figure 6. Zero Crossing Compensation Time ( $T_{zcc}$ ) of UCC28064A

This set of curves shows that the extra on time increases significantly when the input voltage zero crossing (VINAC pin voltage approaching zero). Also, the extra on time is almost identical for different TSET resistor values, which means the extra on time is not adjusted according to the switching frequency. This set of curves works well when the design operates at relatively low switching frequency designs. When the designed switching frequency becomes higher, the inductor value is much smaller. Therefore, the extra on time could cause a lot higher compensation current. The effectiveness of the compensation based on this set of curves begins to deteriorate.

### 3 UCC28065 Changes

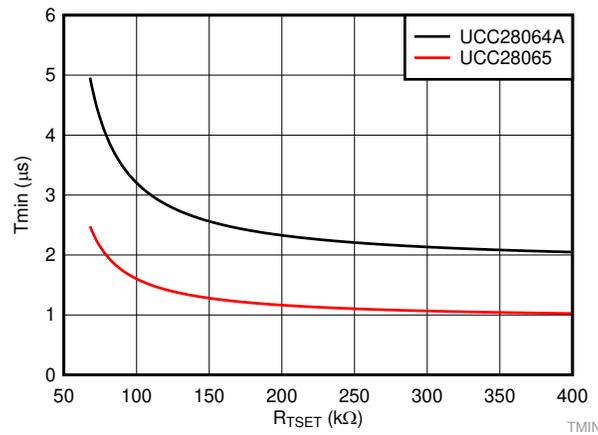
To enable the higher switching frequency designs, the frequency clamp and the zero crossing compensation are modified in the UCC28065 device. This allows the UCC28065 device to become a dedicated device targeting higher switching frequency interleaved TM PFC design. The differences between these two devices are summarized in [Table 1](#).

**Table 1. Summary of Differences Between UCC28064A and UCC28065**

|           | Frequency Clamping (Minimum Period)  | Zero Crossing Compensation |
|-----------|--|----------------------------|
| UCC28064A | $T_{min} = \frac{16C_t V_t}{5 \left( I_2 - \frac{1}{8} \frac{V_{TSET}}{R_{TSET}} \right)}$ | Yes                        |
| UCC28065  | $T_{min} = \frac{8C_t V_t}{5 \left( I_2 - \frac{1}{8} \frac{V_{TSET}}{R_{TSET}} \right)}$  | No                         |

From this table, the UCC28065 removes the zero crossing compensation. This allows UCC28065 to operate with much higher switching frequency without worrying about over-compensating the zero crossing distortion. Despite the additional zero crossing distortion that is added by eliminating this compensation, the PFC performance still meets most power factor and harmonic standards.

Other than the zero crossing compensation, the UCC28065 device has half of the minimum period as the UCC28064A device, which means the UCC28065 doubles the clamping frequency compared with the UCC28064A. Theoretically, this doubles the switching frequency of the UCC28064A. However, given current design is not fully utilizing the full switching frequency capability of the UCC28064A, the UCC28065 would allow 2 to 3 times of the switching frequency increasing compared with current designs. Based on the IC characterization data, the maximum frequency clamp that can be achieved, considering the process and temperature variations, is 800 kHz. The comparison of the minimum period for UCC28064A and UCC28065 is shown in [Figure 7](#)



**Figure 7. Minimum Period Comparison Between UCC28064A and UCC28065**

### 4 Modifying UCC28064A EVM to UCC28065

The UCC28065 is pin-to-pin compatible with the UCC28064A device. The UCC28065 is drop in compatible with any UCC28064A design, such as the UCC28064A EVM [UCC28064EVM-004](#). The only difference observed is the zero crossing distortion. The measured input current waveforms using the UCC28064A EVM and the same board when replacing the UCC28064A with the UCC28065 are shown in [Figure 8](#) and [Figure 9](#).



To fully demonstrate the higher switching frequency capability, the UCC28064A EVM can be modified using UCC28065 and much smaller Boost inductors, with minimum modification to the EVM components. The changes made from the UCC28064A EVM are listed in [Table 2](#).

**Table 2. Component Changes on UCC28064EVM-004 for UCC28065 Evaluation**

| Controller                   | Component Designator | UCC28064A      | UCC28065        |
|------------------------------|----------------------|----------------|-----------------|
| Boost Inductor               | T1, T2               | 340 $\mu$ H    | 110 $\mu$ H     |
| TSET Pin Resistor            | R15                  | 115 k $\Omega$ | 300 k $\Omega$  |
| PFC MOSFETs                  | Q1, Q2               | IRFB11N60APBF  | STF33N60M6      |
| Burst Level Setting Resistor | R17                  | 15 k $\Omega$  | 7.5 k $\Omega$  |
| PHB Setting Resistor         | R29                  | 47 k $\Omega$  | 36.5 k $\Omega$ |

Other than changing the controller IC, the major changes of the board are the Boost inductors. The Boost inductors with roughly 1/3 of the original inductance are used in this modified board. Because of the much smaller inductor value, the Boost inductor size is largely reduced. As demonstrated in [Table 3](#) and [Figure 11](#), the new inductor can achieve approximately 25% diameter reduction and approximately 30% height reduction.

**Table 3. Boost Inductor Comparison**

|           | Inductor Value | Inductor Dimensions    | Switching Frequency @ 90 V 300 W |
|-----------|----------------|------------------------|----------------------------------|
| UCC28064A | 340 $\mu$ H    | D: 38 mm, H: 17.5 mm   | 53.5 kHz                         |
| UCC28065  | 110 $\mu$ H    | D: 28.3 mm, H: 12.3 mm | 165 kHz                          |



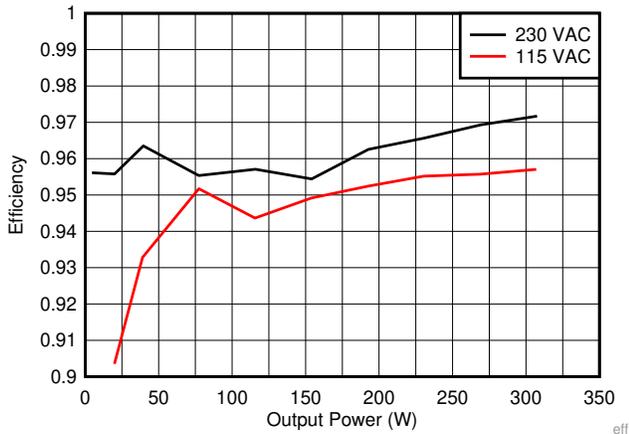
**Figure 11. Boost Inductor Comparison**

Because of a much smaller Boost inductor, the timing of the PFC control changes. Some further modification is required. Firstly, the TSET pin resistor value needs to be adjusted. The TSET pin resistor sets up the gain between the PFC switch on time and the COMP pin voltage. With a higher switching frequency, the gain is expected to be smaller. Therefore, the TSET resistor value needs to be increased. Please note here that due to the design change, the larger TSET value gives a smaller gain for the UCC28064A and UCC28065 devices. While in the earlier generation devices, UCC28063 and before, the smaller TSET resistor value gives a smaller gain. The [UCC28065 design calculator](#) can be used to calculate the suitable TSET pin resistor value with the new inductor. A 300-k $\Omega$  resistor is used for the design.

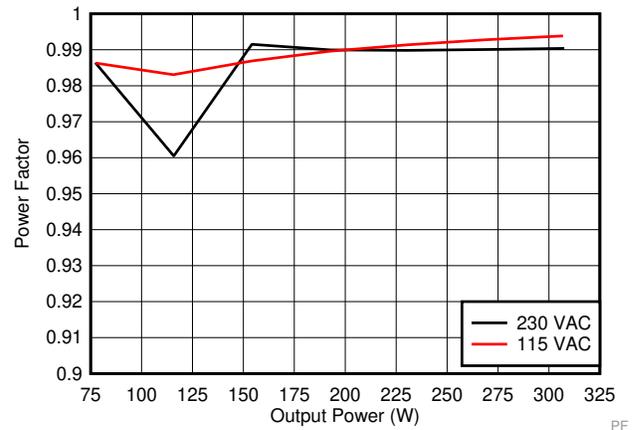
Besides the TSET pin resistor value change, the PHB and the BRST pin voltage level can be adjusted to further optimize the light load operation performance. [Table 2](#) gives some initial recommended values. Further adjustment might be needed to get the optimal performance for the design target.

Furthermore, the PFC MOSFET should be changed to get a better high-frequency operation performance. The UCC28064A EVM uses an old generation MOSFET. There are much better performance Si-based MOSFETs available today that offer lower on-state resistance and lower junction capacitance. The latest GaN technology further improves the performance of the MOSFET through much less junction parasitic capacitances. Both of these devices would further help to improve the overall converter performance.

With all these modifications, the efficiency and power factor performance are summarized in [Figure 12](#) and [Figure 13](#).



**Figure 12. UCC28065 Efficiency at Different Line and Load Conditions**



**Figure 13. UCC28065 Power Factor at Different Line and Load Conditions**

## 5 Summary

The interleaved TM PFC provides a high-efficiency, high-performance, and low-cost solution for many applications. To further reduce the converter size and improve the power density, the switching frequency needs to be increased. The UCC28065 device allows the converter to operate up to 800 kHz, doubling or tripling switching frequency of current interleaved TM PFC design. The UCC28065 device is a preferred solution for high-frequency interleaved TM PFC designs.

## 6 References

- Texas Instruments, [UCC28065 Natural Interleaving™ Transition-Mode PFC Controller with High Light-Load Efficiency Supporting High-Frequency Switching up to 800 kHz Data Sheet](#)
- Texas Instruments, [UCC28064A Natural Interleaving™ Transition-Mode PFC Controller with High Light-Load Efficiency Data Sheet](#)
- Texas Instruments, [UCC28064EVM-004 User's Guide](#)
- Texas Instruments, [An Interleaving PFC Pre-Regulator for High-Power Converters](#), Power Supply Design Seminar 2006-2007, SEM1700, Topic 5

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