Application Report
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Enhanced performance 100-V gate driver increases efficiency in advanced telecom power modules

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ABSTRACT

Telecom applications use power modules based on half-bridge, full-bridge or sync-buck power topologies. These topologies use high performance half-bridge drivers to achieve high frequency operation and high efficiency. The technology behind half-bridge gate drivers has been proven in the industry for decades and the UCC27282 120-V 2.5A/3.5A half-bridge driver is the latest advancement.

The UCC27282 provides a new level of performance paired with new features and operating range improvements in order to improve the robustness of the power modules and allow for more flexibility in optimizing power stage design.

This application note will outline the advantages of the UCC27282 over previous generation drivers to allow optimization of the design and enhance robustness.

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1 Introduction

Telecom and datacom equipment capabilities keep increasing with demand for more processing power within a given size, or even size reduction as well. Increased capabilities of the equipment result in more demand from the power supplies. The power supplies in these systems must be optimized from a space utilization and efficiency standpoint. The complexity of telecom and datacom systems is also increasing which makes them more susceptible to noise and transients. The power consumption of datacenters is a growing concern. There is a focus on increasing efficiency for this reason while also reducing the standby or idle power of equipment not being actively used. Most datacom and telecom power modules have enable functions to minimize the input standby power.

2 New Features of the UCC27282 120-V Half-Bridge Driver

The UCC27282 120-V half-bridge driver has several new features and parameter improvements to help achieve the next level in power module performance and robustness. A low signal on the EN pin disables the driver and sets the UCC27282 in a very low I_{DD} current state. This very low current will help achieve very low input standby power when the power module is disabled. The UCC27282 V_{DD} operating range has been extended to operate from 5.5V to 16V. This allows the designer to optimize the V_{DD} operating voltage to achieve lower gate drive losses. The UCC27282 includes an input interlock feature which prevents both gate driver outputs from being in the high state at the same time in the event that both LI and HI inputs are high at the same time.

3 Extended VDD Operating Range of UCC27282

3.1 Gate Drive Loss and Conduction Loss

The majority of 48V V_{IN} telecom and datacom power module designs have gate driver V_{DD} voltages in the 9V to 10V range using 100-V half-bridge drivers driving 100V V_{DS} rated power MOSFETs. The gate drive losses are reduced with lower V_{GS} drive voltage and many MOSFET devices $R_{DS(on)}$ vs V_{GS} curves indicate that there is little reduction in $R_{DS(on)}$ beyond 8V to 10V V_{GS}. One consideration of selecting the driver V_{DD} is the turn on UVLO threshold and including some margin for negative voltage transients on the bias voltage. With the previous generation drivers this may result in selecting the driver V_{DD} to be higher than the optimum gate drive and conduction loss operating point.

The CSD19531 100V 5.3mΩ MOSFET Q_g vs V_{GS} is shown as an example in Figure 1, and the $R_{DS(on)}$ Vs V_{GS} is shown in Figure 2. Although this MOSFET has an $R_{DS(on)}$ specification with V_{GS}=6V you can see that the $R_{DS(on)}$ curve still has a noticeable declining $R_{DS(on)}$ vs V_{GS} at 6V. At V_{GS}=8V the curve becomes much more flat. Figure 1 indicates an increasing gate charge with V_{GS} with a slope change close to the threshold voltage as one would expect.

The gate drive losses are dependent on V_{DD}, switching frequency (F_{SW}), and MOSFET Q_g as shown in equation 1 below.

$$P_{GD} = V_{DD} \times F_{SW} \times Q_G \quad (1)$$

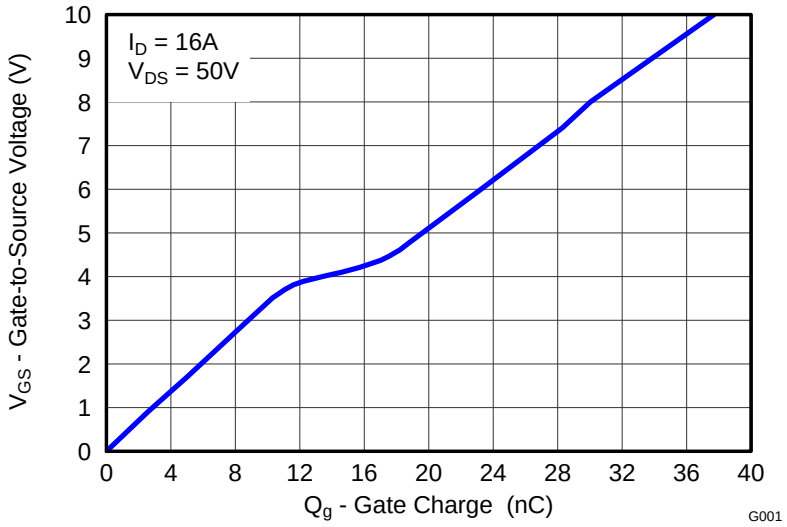

Figure 1. CSD19531 Gate Charge vs V_{GS}

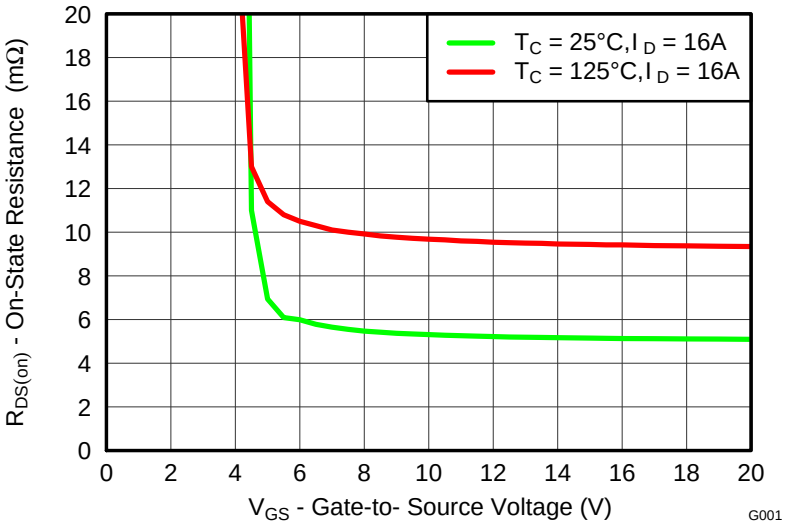

Figure 2. CSD19531 $R_{DS(on)}$ vs V_{GS}

The specific optimum gate drive amplitude is dependent on the power train operating conditions including switching frequency and MOSFET RMS current. Also the characteristics on the power MOSFET are important regarding the Q_g vs V_{GS} curve and $R_{DS(on)}$ vs V_{GS} curve. Refer to the TI application note "Optimizing MOSFET Characteristics by Adjusting Gate Drive Amplitude" for guidance in optimizing the losses.

To illustrate the total power train, gate drive losses and combined losses the synchronous-buck converter shown in Figure 3 was tested under the following conditions: V_{IN}=48V, F_{sw}=200kHz, I_{OUT}=4A(DC), LI/HI deadtime=50ns.

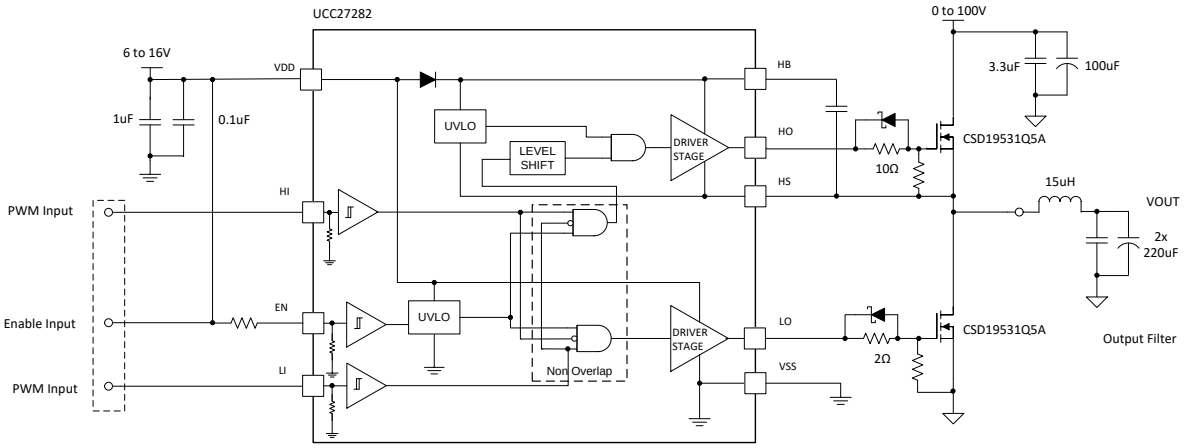

Figure 3. UCC27282 Sync-Buck Test Circuit

The synchronous-buck test circuit data with an output power of 96W is shown in Figure 4 below. You can see the gate drive power dissipation increases with V_{DD} as expected. The power converter losses are higher at 6V and 7V V_{DD} and are relatively stable from 8V V_{DD} and higher. The combined gate drive and power converter losses are minimum at 8V V_{DD}. This particular MOSFET is not a logic level FET, with logic level MOSFETs the optimum gate drive voltage will likely be lower.

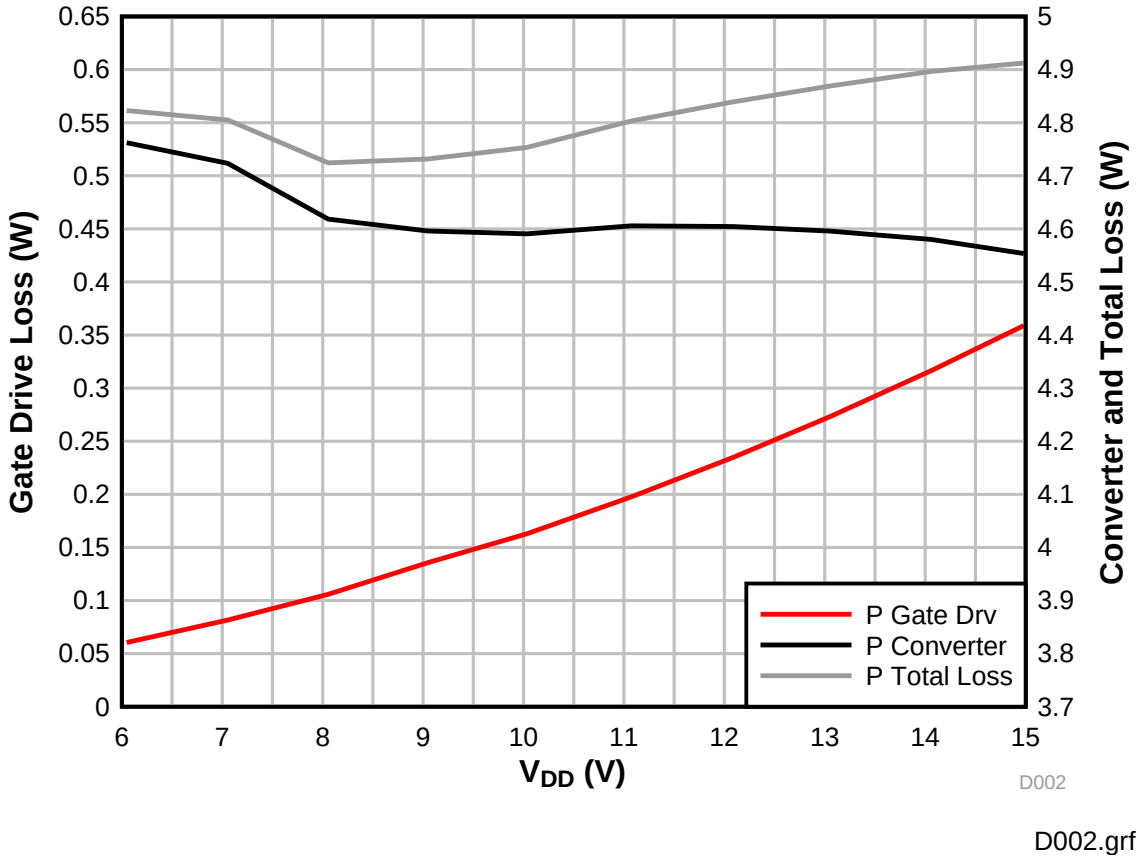

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Figure 4. Sync-Buck Gate Drive, Power Converter, and Total Power Loss

3.2 Gate Drive Strength Over VDD Range

The previous test data discussion covered the tradeoff of gate drive losses and the conduction losses vs the driver V_{DD} operating point. Another important aspect of the gate driver over the V_{DD} operating range is maintaining adequate drive strength especially at lower V_{DD} levels. The UCC27282 gate driver has adequate drive strength of 2.5A source and 3.5A sink current specified at 12V V_{DD} which is the operating voltage most 100-V half-bridge gate drivers are specified. Although the gate drive strength is affected by the V_{DD} voltage level on the UCC27282, the gate drive strength of a similar competitor device is significantly less at lower V_{DD} levels as shown in Figure 5 and Figure 6.

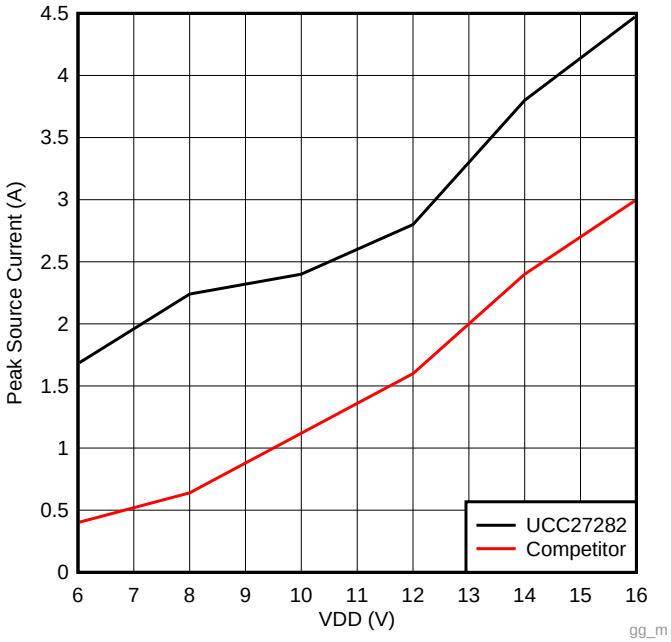

Figure 5. UCC27282 and Competitor Peak Source Current vs V_{DD}

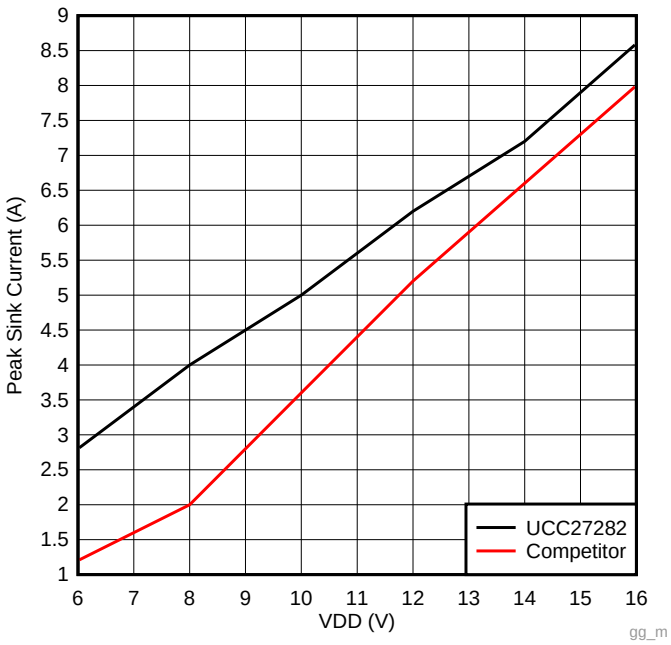

Figure 6. UCC27282 and Competitor Peak Sink Current vs V_{DD}

The reduced drive strength at lower V_{DD} results in increased V_{GS}rise and fall times which will increase the switching losses. Using the same test circuit shown in Figure 3 and the same operating conditions, the competitor gate driver test data is compared to the UCC27282 operating in the same conditions. In Figure 7 the efficiency accounting for all losses including gate driver and power converter is compared between the UCC27282 and competitor device. You can see a noticeable improvement at the V_{DD} range from 6V to 10V of the UCC27282 gate driver converter efficiency over the competitor device.

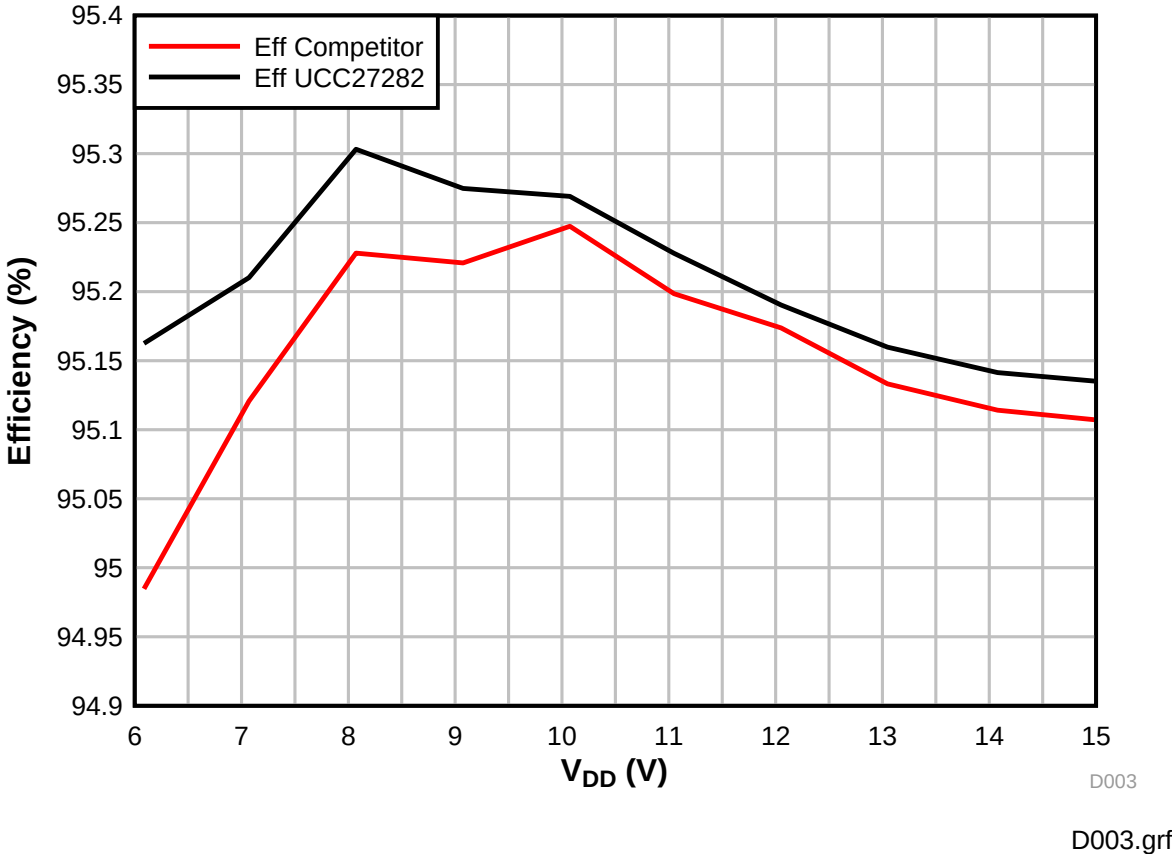

Figure 7. UCC27282 and Competitor Sync-Buck Efficiency vs V_{DD}

4 UCC27282 Enable Function

The enable function of the UCC27282 sets the IC into a very low I_{DD} current state and disables both LO and HO outputs of the driver when the EN pin is below the typical falling threshold of 1.21V. The I_{SD} of the UCC27282 is 7uA typical at V_{DD}=12V when in the disabled state. This is much lower than typical previous generation drivers when in the non-switching state as shown in Figure 8 below. Figure 8 compares the UCC27282 I_{DD} in the enable state non-switching condition and disable condition to the UCC27201A driver in the non-switching condition. The non-switching current of the UCC27201A is typical of many earlier generation 100-V half-bridge drivers. The UCC27201A UVLO is typically 7.1V so the IC will not operate below this UVLO rising threshold. This UVLO rising threshold is also typical of many earlier generation 100-V drivers. You can see that the UCC27282 disable current, I_{SD}, is much lower than the I_Q of the UCC27201A. At V_{DD}=8V the UCC27201A I_Q is 297uA and the UCC27282 I_{SD} is 4.1uA, this is a standby power of ~2.4mW compared to ~33uW for the UCC27282. At V_{DD}=10V the UCC27201A I_Q is 389uA vs UCC27282 I_{SD} of 5.54uA which results in a standby power of 3.89mW compared to 55.4uW. Refer to Table 1 for details on the standby power and current comparison.

If the end application requires multiple drivers the difference in standby power is relative to the number of drivers required. Coupled with careful design of the supervisory and bias circuits and selection of controller IC's, the UCC27282 can help achieve very low standby power.

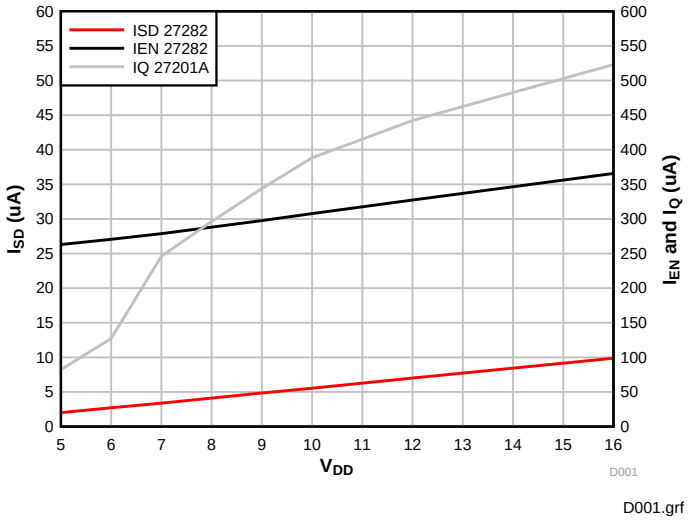

Figure 8. UCC27282 I_{EN}, I_{SD}, and UCC27201A I_Q

Table 1. UCC27282 I_{SD} and P_{SD}vs UCC27201 I_Q and P_Q

V_{DD}	I_{SD} 27282 (uA)	P_{SD} 27282 (uW)	I_Q 27201 (uA)	P_Q 27201 (mW)
6	2.71	16.26	127.2	0.76
7	3.38	23.66	246.1	1.72
8	4.11	32.88	296.2	2.37
9	4.85	43.65	343.9	3.1
10	5.54	55.4	388.4	3.88
12	7.01	84.12	442.2	5.31

5 UCC27282 Input Interlock Feature

The UCC27282 driver includes an input interlock feature that prevents both LO and HO outputs from being in a high state at the same time. Many topologies including synchronous-buck, half-bridge, full-bridge and full-bridge synchronous rectification cannot tolerate the high side and low side MOSFETs to be turned on at the same time, or cross conduction and possible damage can occur. There are a number of events which may result in voltage spikes or ringing beyond the normal observed behavior, including fault conditions such as short circuit or transients from ESD or EFT (electrical fast transient) events. These abnormal conditions can result in disturbances on critical control signals such as the gate driver input signals. The UCC27282 does not have a forced dead time between the LO and HO output rising and falling edges, so the timing can still be determined by the controller for precise dead time control. Figure 9 below illustrates the LO and HO outputs both in the low state corresponding to the 20ns overlap on the LI and HI inputs.

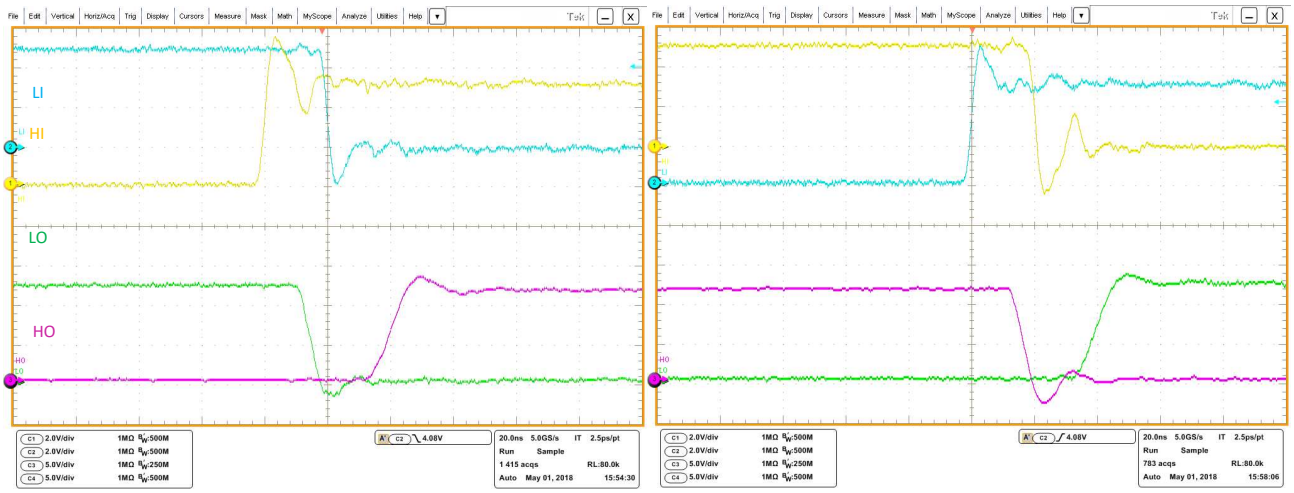

Figure 9. UCC27282 LO and HO with 20ns Overlap on LI and HI

6 Summary

The UCC27282 gate driver has several features to help achieve a higher level of performance and robustness in telecom and datacom modules.

The V_{GS} gate drive voltage operating range can be extended to lower levels with the UCC27282 to achieve the optimum operating parameters for highest efficiency. If the optimum operating point is 8V or 9V V_{DD} range the UCC27282 driver will have more margin for bias voltage transients or droop without triggering the UVLO shutdown than previous generation drivers.

The UCC27282 can maintain ample gate drive strength when operating at the lower V_{DD} range compared to competitor devices. This can result in a measurable improvement in power converter efficiency.

The enable function can reduce the standby current by 300uA to 450uA per driver in the power converter. This will help achieve very low standby power which may be a feature advantage in the end equipment.

Robustness of the power converter using the UCC27282 gate driver will improve due to the input interlock feature. The power MOSFET power stage will not have significant cross conduction due to false triggering of the gate driver from input signal voltage spikes or noise.

7 References

- UCC27282 120-V Half-Bridge Driver with Cross Conduction Protection and Low Switching Losses
- CSD19531Q5A 100V N-Channel NexFET Power MOSFETs

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