How to overcome negative voltage transients on low-side gate drivers' inputs

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Switch-Mode Power Supplies (SMPS) and Merchant DC-DC converter applications often require high current drive and hard switching to drive large loads. This hard switching of the power FETs in combination with layout constraints often lead to noise in the system. This noise appears as ground bounce and ringing at the driver's input/output terminals as the power ground and controller ground are connected. Most gate drivers are equipped to handle short negative pulses at the output stage through the internal FET's body diodes in the output stage. It is necessary to take precautions to prevent the overshoot and undershoot from damaging the driver's inputs.

Causes of Negative Voltages at the Inputs of Gate Driver

Low-side drivers are used between the controller and the power MOSFETs to help minimize switching losses in the PFC stage. Achieving this requires high drive current during hard switching of the power FET to quickly pass through the Miller plateau region. Figure 1 shows a simplified schematic of a low-side gate drive. During the switching transition of the MOSFET, there is a pulse of high di/dt generated by quick turn-on/off of the MOSFET. This fast changing slew rate coupled with the parasitic inductance from the high current loop generates a negative voltage spike that can be estimated using the equation: $V_n = L_{ss}$* di/dt. L_{ss} represents the parasitic inductance of the internal bond wires of the power MOSFET and the PCB trace inductance in the return ground loop and can range anywhere from a few nanoHenries (nH) to more than 10 nH depending on layout and device package.

From this equation, it is obvious that this negative voltage is proportional to the parasitic inductance in the circuit (influenced by the PCB trace length and width) and the change in current of the power switch. In a typical low-side gate drive circuit, the controller and the power stage share the same DC ground reference, but some AC parasitics exist when the controller is some distance away from the driver. The high di/dt from the MOSFET's source flows through the low impedance ground path shown on Figure 1 and causes a negative V_n voltage on the power stage ground. This can corrupt the gate driver input signal by changing the differential voltage between input pins and the driver's ground reference pin, which leads to a false turn-on of the driver and potentially damage to the power FET. The transient currents from the high di/dt switching coupled with the trace inductance L_{ss2} on the controller ground path also create a voltage that can damage the controller.

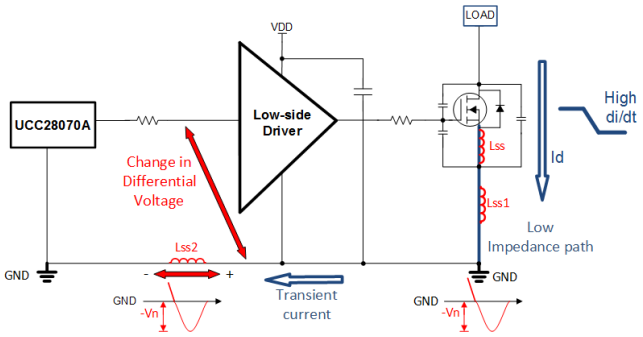

Figure 1. Simplified Schematic of a Low-side Gate Drive Using UCC27511A

Figure 2 shows a simulation of a simplified power stage in a low-side gate drive where DRV_OUT represents the driver's output and L_{ss} and L_{ss1} represent the previously described internal parasitic source inductance of the power FET and the parasitic inductance from the PCB trace length of the ground return loop.

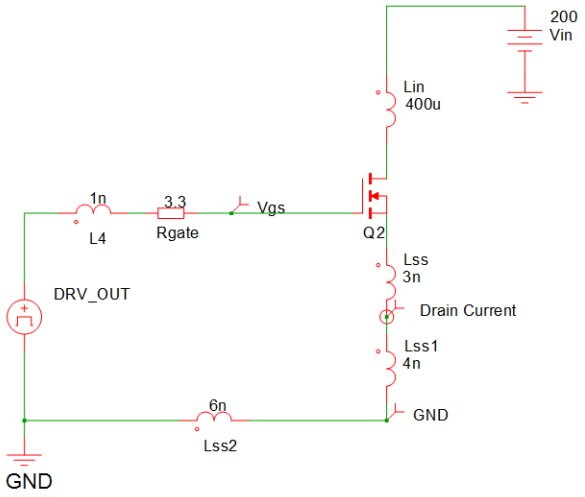

Figure 2. Example Simulation of a Simplified Low-side Gate Drive Power Stage

Figure 3 and Figure 4 show the simulation results when switching at 300 kHz with a gate voltage V_{GS} = 12 V. We can observe the ground shifting during the rising and falling transitions of the gate voltage V_{GS}. The high frequency switching causes rapid change in drain current di/dt which coupled with the parasitic inductances on the source of the MOSFET L_{ss} and L_{ss1}, cause the negative transients on the circuit's ground (blue waveform) to reach up to –3 V. This can damage the driver's input stage if an appropriate driver is not selected to handle such transients.

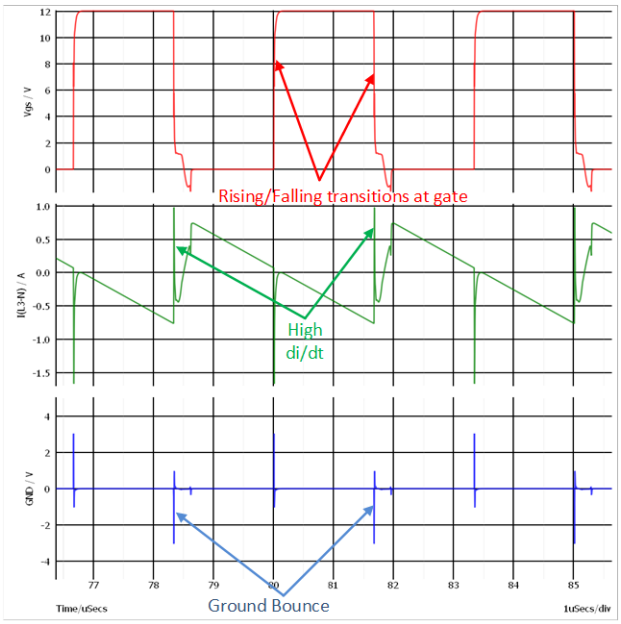

Figure 3. Simulation Results

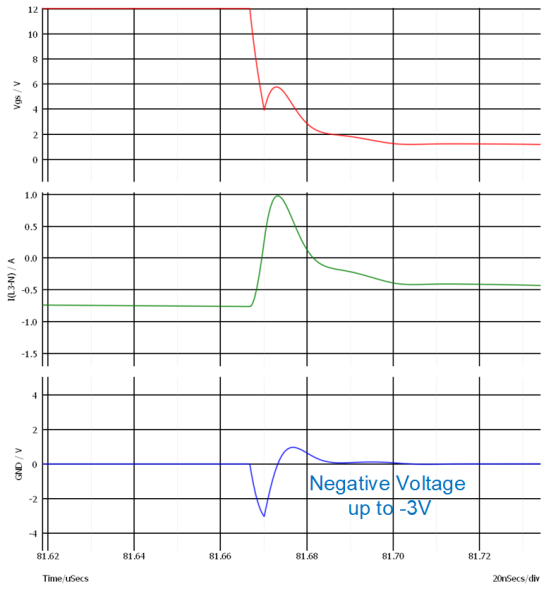

Figure 4. Zoomed-in Simulation Results

Design Guidelines

The simplest method to prevent these negative transients on the driver's input stage is to slow down the switching transitions at the gate. Series gate resistors help limit the rise and fall times of the power FET while reducing the power dissipation across the gate driver IC. An optimized layout helps minimize the effects of the parasitic inductance L_{ss} contributing to the negative transients on the input stage. In general, it is recommended to place the driver very close to the power FETs to reduce PCB trace length throughout the power stage and to use bypass capacitors placed very close to the driver's V_{DD} pin. A small input RC filter ranging between 0 Ω to 100 Ω and 10 pF to 100 pF helps to minimize differential input voltage changes at the driver, but only if the capacitor is placed very close to the driver's input pins. But in SMPS applications where fast switching and large input transients are unavoidable, it is essential to select a robust driver capable of tolerating negative transients at its inputs. UCC27511A is part of TI's portfolio of low-side drivers capable of handling negative voltage transients up to –5 V at its inputs. This device gives designers sufficient margins for driving large loads and improve the overall system efficiency and reliability.

In summary, this tech note discusses negative transients on gate drivers' inputs common in SMPS applications and their impact in the gate drive. It is important for designers to consider these transients when driving large loads and selecting a robust driver in order to improve reliability in the system.

Related Documentation

Find more information on low-side gate drivers at ti.com/gatedrivers

UCC27511A Product Folder

UCC27524A Product Folder

UCC28070A Product Folder

UCC27517A Product Folder

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