Application Report
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AC Ripple Rejection in AC/DC Systems Using LLC

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ABSTRACT

AC ripple rejection is a performance metric of offline, AC/DC power systems that characterizes how well a given power supply is able to reject the low-frequency voltage ripple present at the bulk capacitance of PFC stages. AC ripple is inherent to PFC operation and is a function of the total capacitance of the PFC output. The ability of the downstream converter to reject AC ripple depends on the control scheme used as well as the loop response of the converter. Hybrid hysteretic control in the UCC25630x controller offers superior AC ripple rejection. This control scheme offers system benefits by reducing the contribution of AC ripple to total peak-to-peak output voltage ripple and potentially reducing the required PFC output capacitance to meet a given hold-up time requirement, offering both superior performance and BOM cost savings.

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1 Introduction

In a traditional AC/DC power system using a power factor correction (PFC) stage and a downstream isolated DC/DC converter, AC ripple rejection is a performance metric that characterizes how well a power supply is able to reject the low-frequency AC ripple component on the bulk PFC output capacitance. In an ideal power supply, there is a sufficient feedforward component in the isolated DC/DC control scheme, which minimizes the effect of an AC ripple on the output voltage regulation. In conventional LLC designs, this AC ripple component can lead to undesirable effects in the LLC output such as significant output ripple. Figure 1 illustrates this issue in a half-bridge LLC topology.

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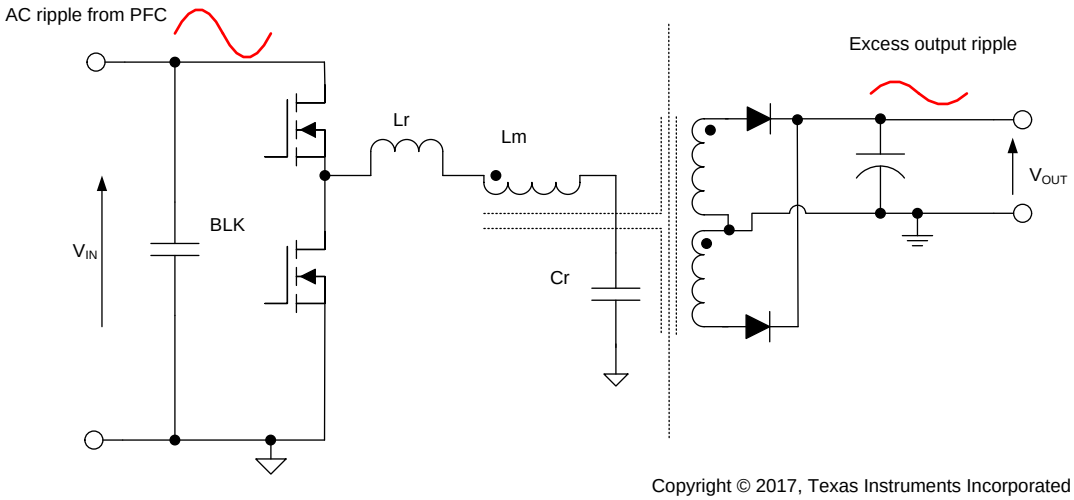

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Figure 1. LLC AC Ripple

2 AC Ripple Causes and System Considerations

To better understand this issue, it is important to examine why AC ripple is present at the output of PFC stages. Figure 2 shows an example PFC circuit.

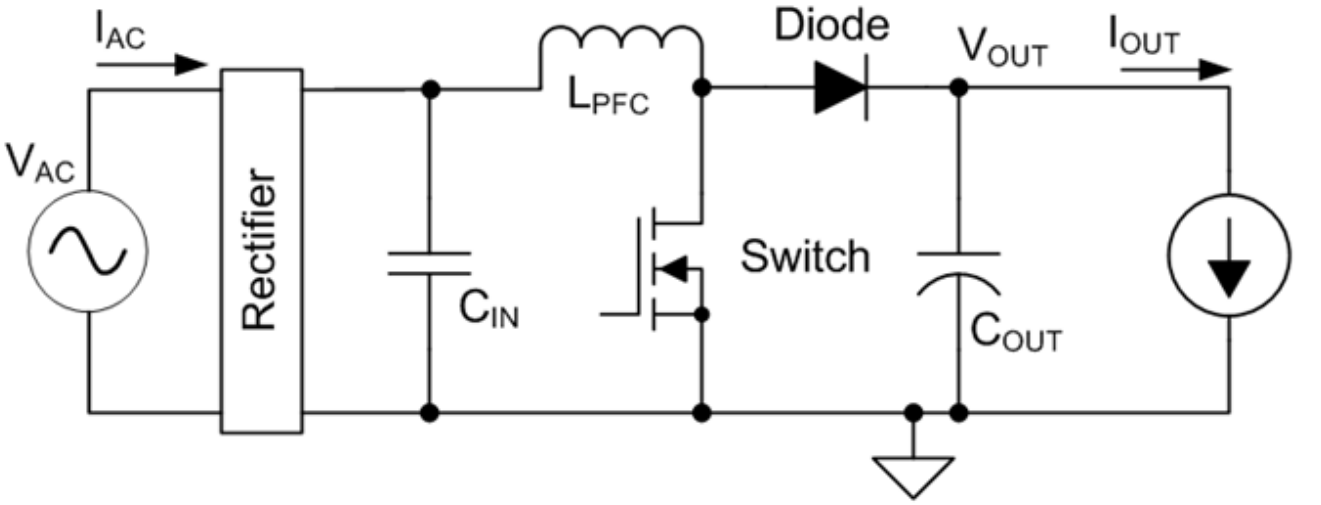

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Figure 2. Single-Phase Boost PFC Circuit

One of the primary functions of the PFC stage is to track the input current to be in phase with the input voltage. This tracking is done to obtain a high power factor across the load range and to limit the total harmonic distortion of the line current. The input current tracking action means the instantaneous input power to the PFC stage from the AC source fluctuates during the line cycle. For a transition mode PFC, the input power can be expressed using Equation 1:

$$P_{IN} = 2 \cdot V_{LineRMS} \cdot I_{LineRMS} \cdot (\sin \theta)^2 \quad (1)$$

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Assuming a typical application with a constant power load, there are instances during the line cycle where the power drawn from the AC source exceeds the power demand of the load. In this instance, the excess power is stored in the bulk output capacitance. Conversely, there are instances during the line cycle where the power demanded by the load is greater than the power drawn from the AC source. In this case, the power deficit is supplied from the output capacitance. At steady state, this behavior results in a low-frequency voltage ripple at the output of the PFC stage as a function of the total output capacitance of the PFC. For transition mode PFC, this low-frequency voltage ripple can be expressed using Equation 2:

$$\nabla V_{ripple} = \frac{P_{out}}{2 \cdot \pi \cdot F_{Line} \cdot V_{out} \cdot C_{out}} \quad (2)$$

While it is possible to reduce this ripple by increasing the PFC output capacitance, this approach can be expensive due to the high cost of high-voltage capacitors capable of handling the significant current ripple of a boost PFC.

3 LLC Control Method

A second approach is to mitigate the AC ripple in the LLC converter. To implement this, consider the input voltage variation when selecting an appropriate control scheme for the LLC converter. Figure 3 shows a simplified diagram for hybrid hysteretic control (HHC) of a half-bridge LLC converter.

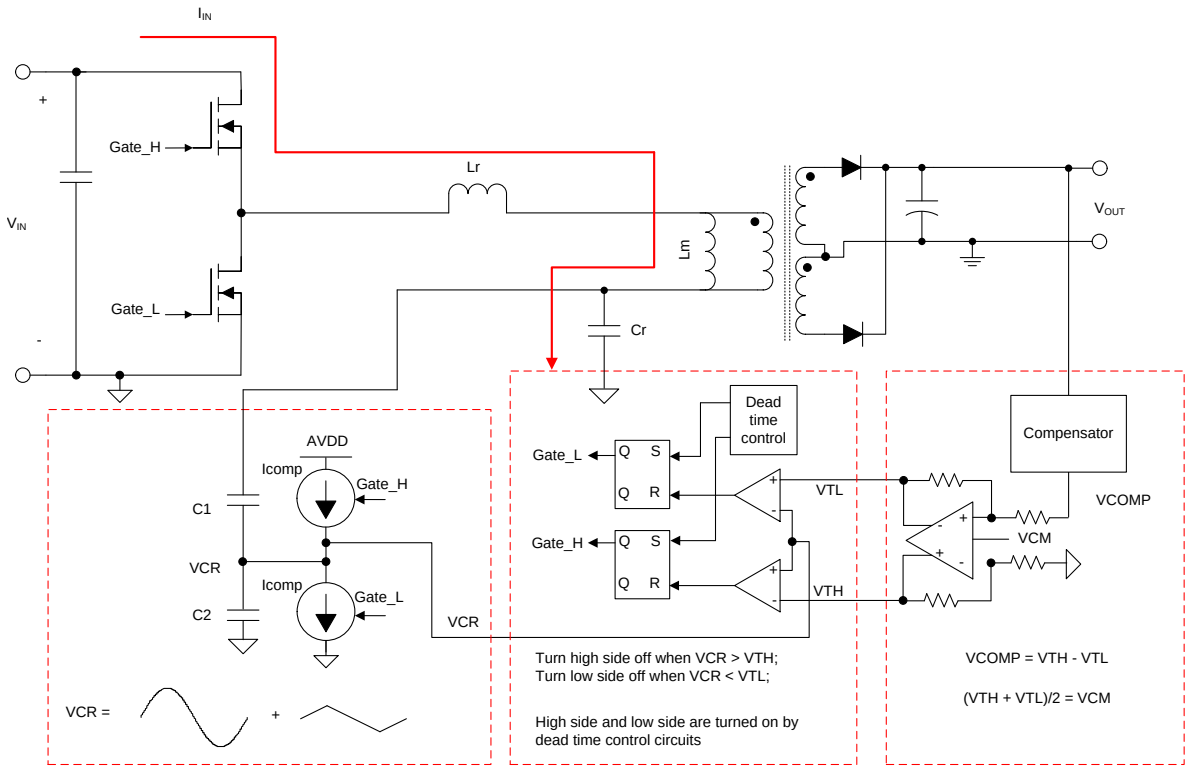

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Figure 3. Hybrid Hysteretic Control Diagram

HHC combines charge control and frequency control. The voltage variation on the resonant capacitor, Cr, is sampled through the capacitive divider and used to control the switching logic. The two current sources connected to the midpoint of the capacitive divider add a frequency compensation ramp to the sampled signal.

By controlling the voltage variation of the resonant capacitor, the net input charge going into the resonant tank is controlled, and thus the input power delivered to the output is controlled. This control scheme enables the designer to account for AC ripple variation at the input of the LLC converter.

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4 Practical Considerations

Measuring output voltage ripple requires proper probing technique to prevent noise from coupling into the probe and corrupting the ripple measurement. The long ground clip used in a traditional probing technique forms an antenna capable of picking up high-frequency noise, especially in the presence of switching elements carrying high current. A preferred probing method is to use a differential probe or use a "tip and barrel" probing method. Tip and barrel involves removing the probe hat and wrapping a short piece of wire around the ground connection of the probe. This wire shortens the length of the probe tip that is exposed to high electromagnetic radiation near the power supply. It is recommended to measure output voltage ripple directly at the pads of an output capacitor to reduce the effect of parasitic trace inductance on the board. The following figures illustrate the difference between traditional probing and tip and barrel probing.

In Figure 4, a traditional probing technique is used. The probe is connected to an output voltage test point and a ground terminal. The ground clip is quite far from the point of measurement. One can expect poor ripple measurement using this setup.

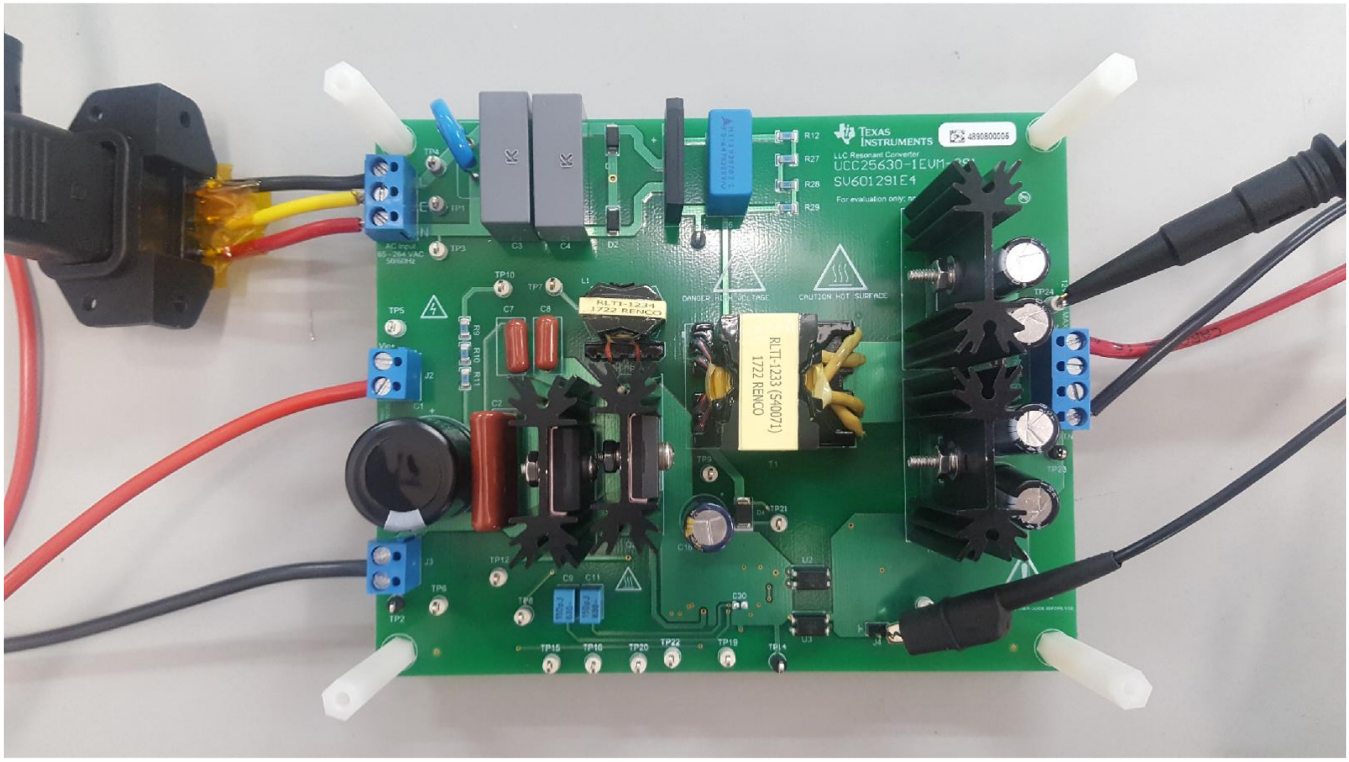

Figure 4. Traditional Probing

In Figure 5, tip and barrel probing technique is used. Measurement is taken directly at the leads of one of the output capacitors through a 2×1 probe head. One can expect less noise using this ripple measurement setup.

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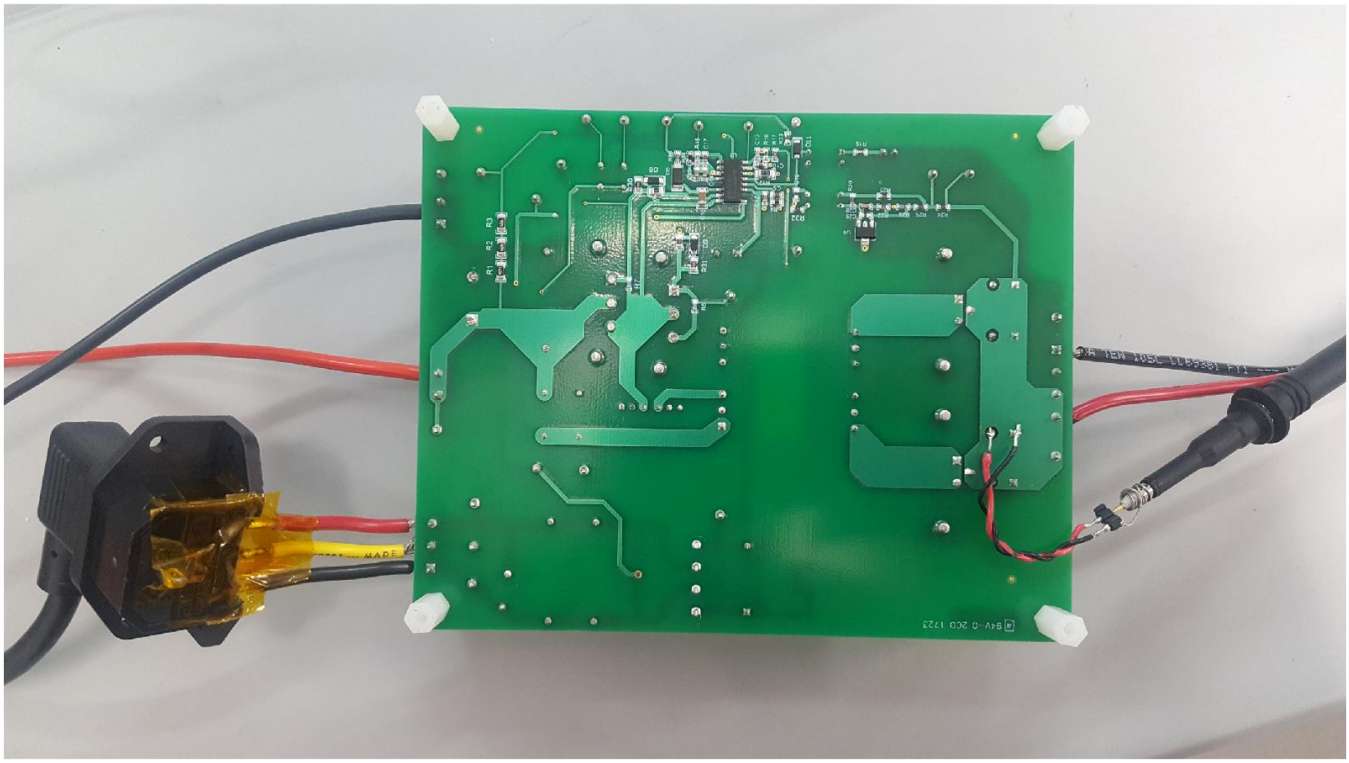

Figure 5. Tip and Barrel Probing

To illustrate the impact of proper probing technique on output ripple measurement, both techniques are used to measure output voltage ripple in Figure 5. Tip and barrel probing is used on channel 1 while traditional probing is used on channel 4. Figure 6 shows the peak-to-peak ripple is 200 mV less when using tip and barrel than when using traditional probe connections.

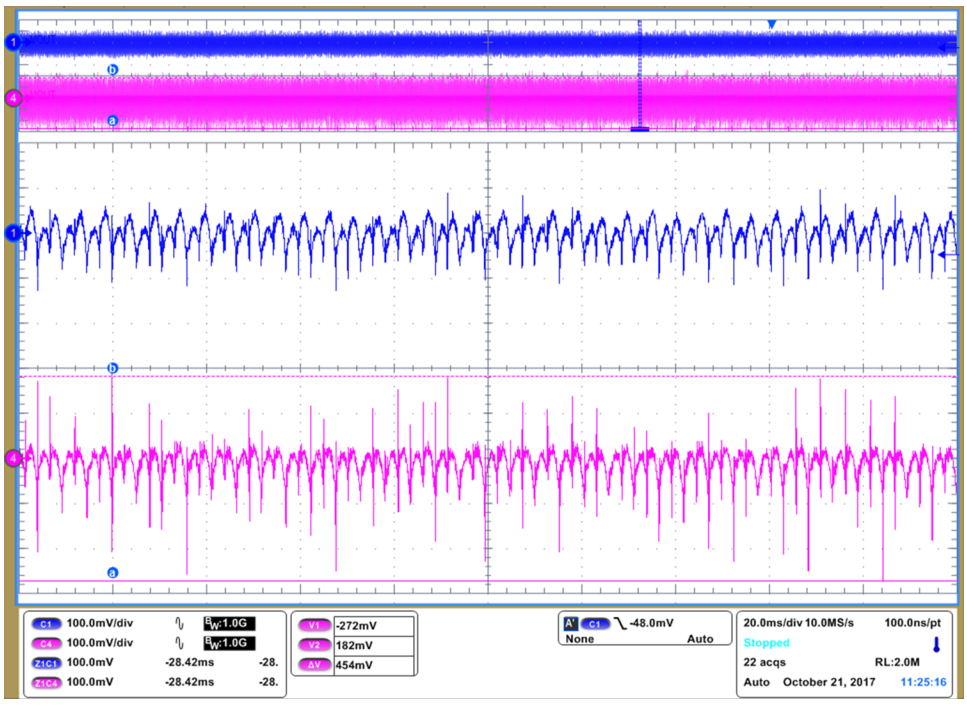

Figure 6. Output Ripple Comparison

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5 Output Voltage Ripple Results

The following measurements are taken on the UCC25630-1EVM-291, a 120-W LLC evaluation board. To test the AC ripple rejection of the design, a 390-V DC voltage with a 60-Hz, 25-V_{RMS} AC ripple component is applied to the input and the EVM is loaded to 10 A. The following images show the output ripple results of the LLC converter.

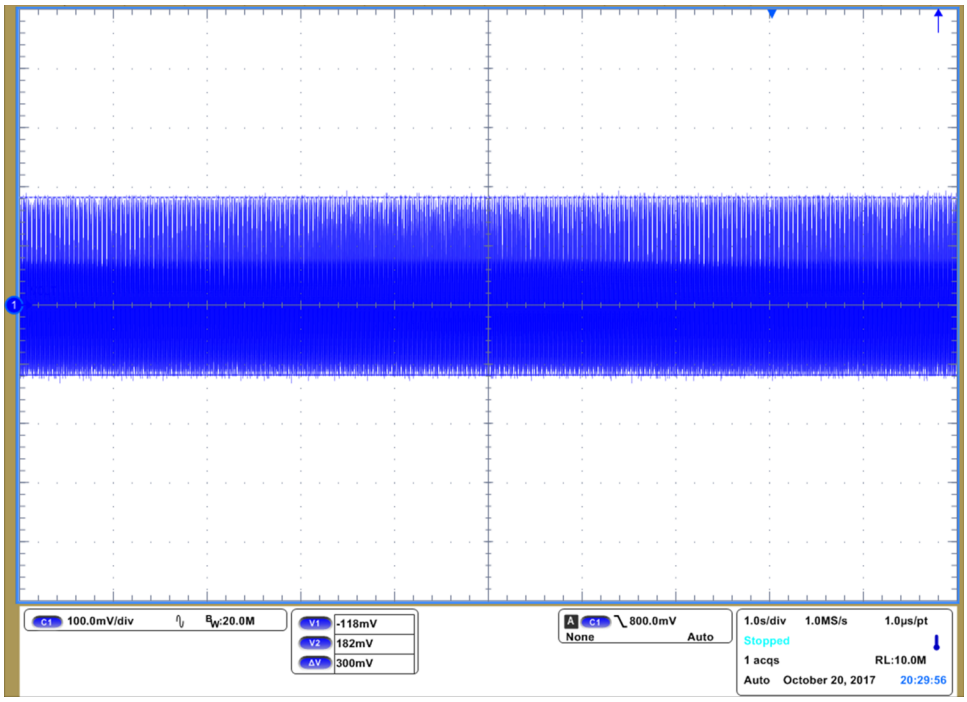

Figure 7. UCC25630-1EVM-296 Output Ripple

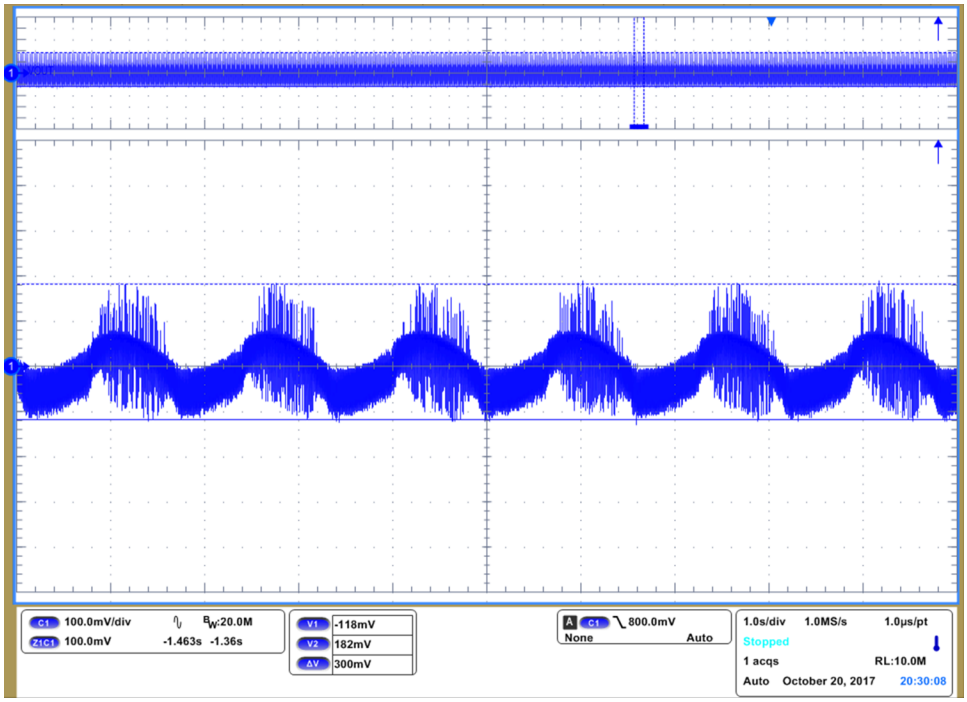

Figure 8. UCC25630-1EVM-296 Output Ripple Zoomed In

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The total output ripple voltage is 300 mV peak to peak, which is 2.5% of the total output voltage. As shown, a 60-Hz component is not present in the output ripple voltage; only the ripple caused by the LLC switching stage is present.

6 Conclusion

AC ripple is an undesirable characteristic of AC/DC systems that can result in excess output voltage ripple of the downstream isolated DC/DC converter and can pose problems for applications with a strict ripple requirement for power supplies. AC ripple is present in PFC stages because the PFC input current is manipulated to follow the line voltage for a high power factor, meaning the input power to the PFC stage varies with the line voltage. This AC ripple component is a function of the bulk PFC output capacitance. HHC offers superior AC ripple rejection by directly controlling the total input power delivered to the secondary every switching cycle. Superior AC ripple rejection allows the designer to meet strict output voltage requirements or reduce the PFC output capacitance to reduce BOM cost and board size.

7 References

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- Texas Instruments, *UCC256301 Enhanced LLC Resonant Controller with High Voltage Gate Driver Data Sheet*
- Texas Instruments, *Predicting Output Capacitor Ripple in a CCM Boost PFC Circuit* , TI E2E™ Community

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