Application Report
SLUA809–February 2017

Unified Ground Connection Recommendation on TPS53K-Integrated FET-Converter Devices

Xiao Xu

ABSTRACT

This document provides the unified ground connection recommendation for TPS53K-integrated FET-converter devices.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Since 2010, TI has introduced several generations of TPS53K-integrated FET converters with current rating ranging from 1.5 A to 40 A. This particular family of devices targets the enterprise computing applications; therefore, the devices share the same competitive performance goals in terms of efficiency, thermal, and transient response. Many design considerations simplify the system design and layout as well as reduce overall bill of materials (BOM).

Table 1 summarizes the TPS53K converter devices in terms of their applications.

Table 1. TPS53K Device Details

PART NUMBER	CURRENT RATING	VIN RANGE (V)	VOUT RANGE	PACKAGE SIZE AND STYLE	GROUND PINS
TPS53310	3 A	2.9 V to 6 V	0.6 V to 4.2 V	3 × 3 QFN-16	AGND, PGND
TPS53311	3 A	2.9 V to 6 V	0.6 V to 4.2 V	3 × 3 QFN-16	AGND, PGND
TPS53316	5 A	2.9 V to 6 V	0.6 V to 5.5 V	3 × 3 QFN-16	AGND, PGND
TPS53321	5 A	2.9 V to 6 V	0.6 V to 4.2 V	3 × 3 QFN-16	AGND, PGND
TPS53511	1.5 A	4.5 V to 18 V	0.75 V to 5 V	3 × 3 QFN-16	GND, PGND
TPS53312	3 A	4.5 V to 18 V	0.75 V to 5 V	3 × 3 QFN-16	GND, PGND
TPS53313	6 A	4.5 V to 16 V	0.6 V to 10 V	4 × 4 QFN-24	GND1, GND2, PGND
TPS53314	6 A	4.5 V to 25 V	0.6 V to 5.5 V	5 × 7 QFN-40	GND1, GND2, PGND
TPS53315	12 A	3 V to 15 V	0.6 V to 5.5 V	5 × 7 QFN-40	GND1, GND2, PGND
TPS53318	8 A	1.5 V to 22 V	0.6 V to 5.5 V	5 × 6 QFN-22	NA
TPS53319	14 A	1.5 V to 22 V	0.6 V to 5.5 V	5 × 6 QFN-22	NA
TPS53353	20 A	1.5 V to 15 V	0.6 V to 5.5 V	5 × 6 QFN-22	NA
TPS53355	30 A	1.5 V to 15 V	0.6 V to 5.5 V	5 × 6 QFN-22	NA
TPS53513	8 A	1.5 V to 18 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS53515	12 A	1.5 V to 18 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS53915	12 A	1.5 V to 18 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS548A20	15 A	1.5 V to 20 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS549A20	15 A	1.5 V to 20 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS548B22	25 A	1.5 V to 18 V	0.6 V to 5.5 V	5 × 7 QFN-40	AGND, DRGND, PGND
TPS548D22	40 A	1.5 V to 16 V	0.6 V to 5.5 V	5 × 7 QFN-40	AGND, DRGND, PGND
TPS549D22	40 A	1.5 V to 16 V	0.6 V to 5.5 V	5 × 7 QFN-40	AGND, DRGND, PGND
TPS548D21	40 A	1.5 V to 16 V	0.6 V to 5.5 V	5 × 7 QFN-40	AGND, DRGND, PGND

In the integrated converter designs, where controller, gate driver, and half bridge (HB) FETs are uniquely integrated and fit into a small semiconductor device package, ground treatment is a very sensitive matter. To understand how different grounds are defined, connected, and used in an integrated circuit (IC), the environment should give insight how to create the ground layout in a system or printed circuit board (PCB) environment. Unfortunately, no two ICs are ever laid out the same way. There are many different approaches IC designs can employ in regards to ground layout, similar to that of system or PCB board. In the case of TPS53K device family, the ground treatment was created in a similar working fashion, which results in a uniformed ground layout recommendation possible.

Figure 1 illustrates conceptually how the grounds (including thermal pad – red rectangle) of the internal IC are allocated, distributed, and connected.

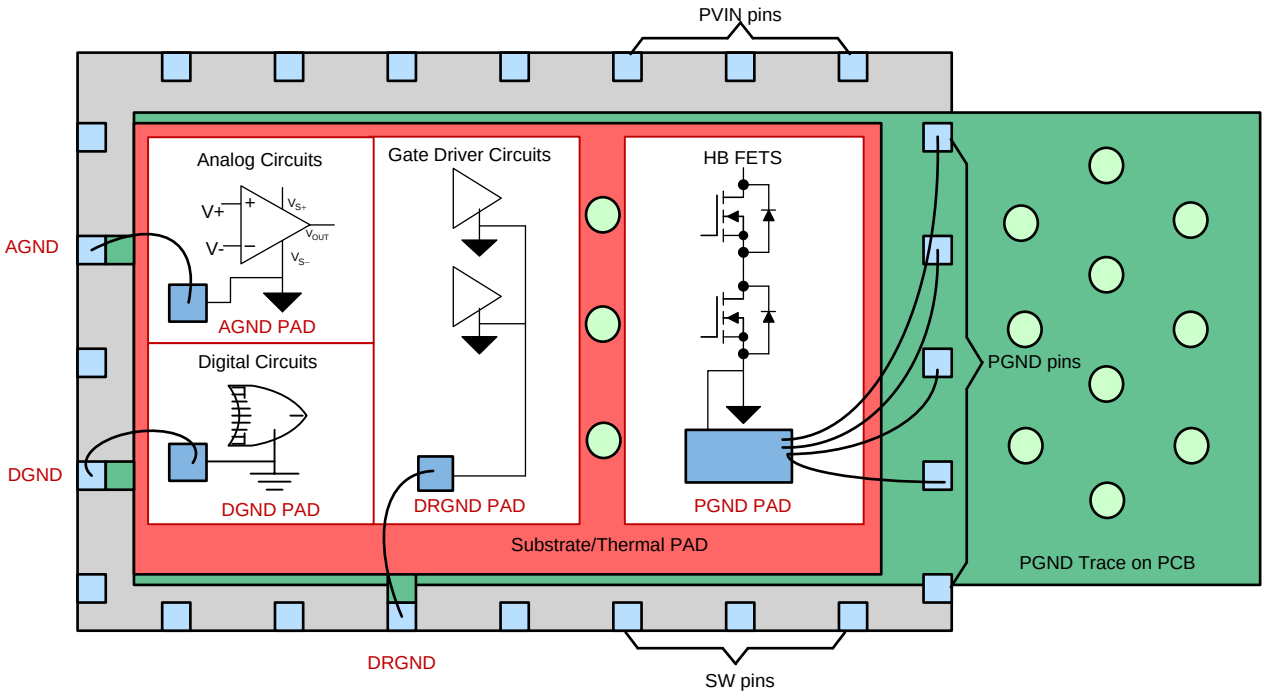

Figure 1. Ground Arrangement Diagram of TPS53K-Integrated FET Converter

Generally speaking in each integrated-FET converter design, there are a few essential circuit elements or blocks. As shown in Figure 1, the entire IC is broken down into analog circuit, digital circuit, gate drivers, and HB FETs. In most cases there is a dedicated ground assignment for each of the major circuit blocks. For example, analog ground (AGND) is used to serve the analog circuits, digital ground (DGND) to digital circuits, driver ground (DRGND) to gate drivers, and PGND to HB FETs. In the ideal situation where pin count is sufficient, all of the ground assignments can be brought outside of the IC through dedicated GND pins. In situations where pin count is of concern, the arrangement can be made at the IC layout to combine and merge the ground assignments.

For quad flat no-leads (QFN) packaged devices, there is also a thermal pad sitting on the bottom of the package (see Figure 2). The silicon die (analog circuit, digital circuit, gate driver, and HB FETs) is attached onto the thermal pad using thermally conductive adhesive. Figure 3 shows a cross-sectioned view of a typical QFN package. The exposed thermal pad is made of electrically conductive material, and when soldered on the PCB, the material makes a good electrical and thermal connection with the PCB.

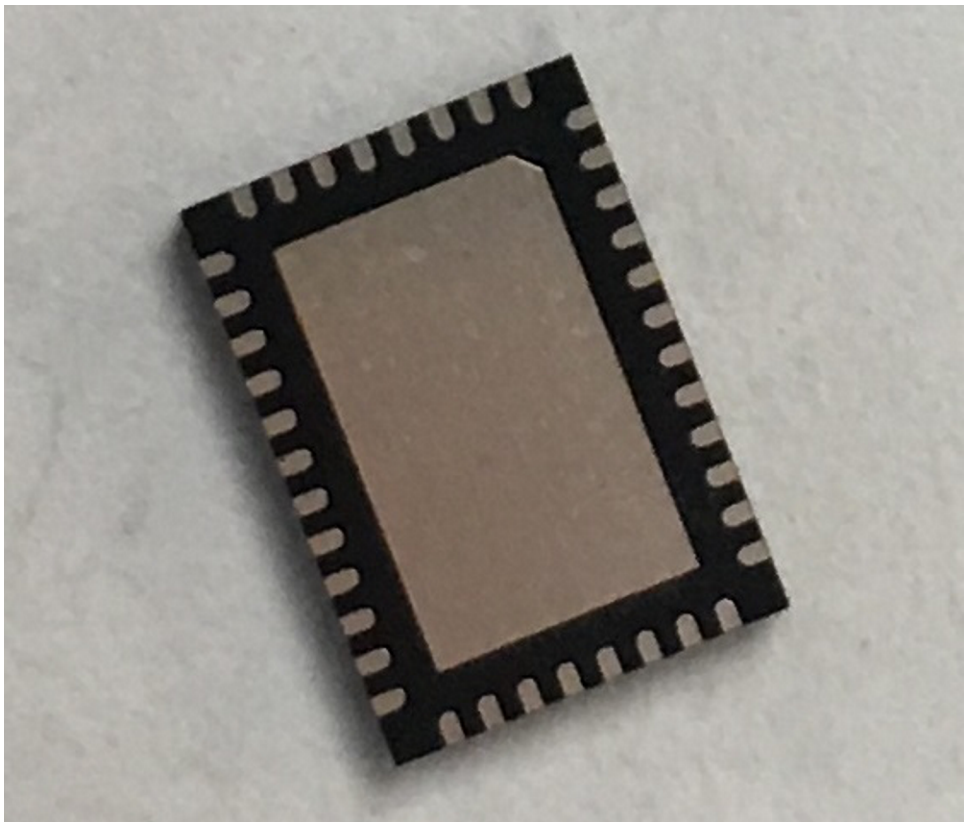

Figure 2. Thermal Pad of Upside Down 40-pin 5-mm × 7-mm QFN

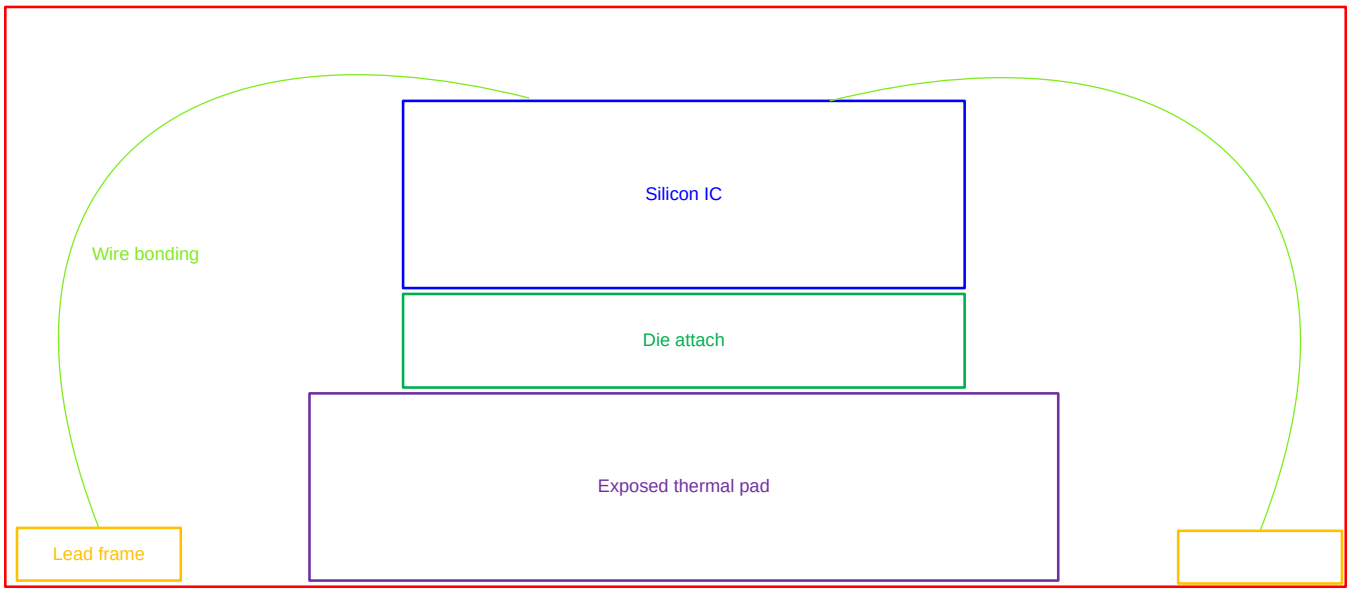

Figure 3. Section View of QFN Package

Once soldered down on the PCB, the thermal pad and the land pattern forms a strong connection electrically and thermally. It is strongly recommended that multiple thermal vias are placed on the land pattern. The vias should be made through hole and with an electrical connection to system or PCB general ground. The light green vias on the red thermal pad in Figure 1 are drawn to illustrate the above connection. The green land pattern with multiple vias is electrically connected to the system ground. All the ground assignments of the device are connected to the green ground land pattern underneath the device. The single point of ground connection is achieved by tying analog ground, digital ground, gate driver ground, and HB FETs ground together at the thermal pad land pattern, as illustrated in Figure 1.

For TPS53K-integrated FET converters, the uniformed ground connection recommendation is to take advantage of the thermal pad and tie all ground pin assignments to the thermal pad from underneath of the device (see green trace and copper fill in Figure 1).

2 References

1. Wikipedia, *Quad Flat No-leads package*, Article

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265