Application Report
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Design the UCC28704 With the UCC24636 (PSR and SR)

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ABSTRACT

Higher power conversion efficiency in a switch-mode power supply is usually obtained for use in a synchronous rectifier (SR) on a secondary-side controller. For example, to use the UCC24636, work with a primary-side regulated (PSR) controller such as the UCC28704. A primary-side regulated converter does not need an optocoupler to obtain the output voltage signal from the secondary-side controller to the primary-side, so this cost-saving process helps to gain higher reliability. A typical and simplified circuit diagram is illustrated in Figure 1 for a PSR flyback converter using the UCC28704 with the SR driver UCC24636.

When using the UCC28704 and the UCC24636 together, TI requires additional design considerations that are discussed in this application report. This report intends to help designs using the UCC28704 with the UCC24636, but similar considerations can be made for other PSR flyback controllers for use with the UCC24636.

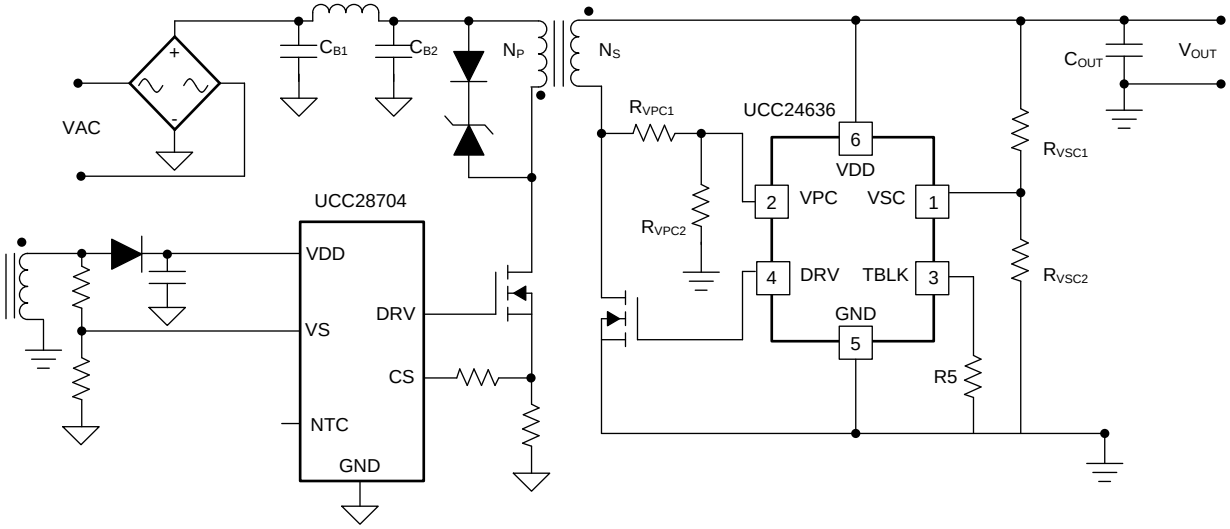

Figure 1. Functional Circuit Diagram

Contents

List of Figures

List of Tables

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1 Considerations When Designing the UCC28704 With the UCC24636

Redraw the graph shown in Figure 2 and see the Auxiliary Waveform Details graphic of the Applications and Implementation chapter of the UCC28704 High-Efficiency Off-Line CV and CC Flyback Controller with Primary-Side Regulation (PSR) Data Sheet. The total time partition and time requirement set up the minimum de-mag time, $t_{DMAG\ (min)}$. Possible variations and tolerances must be added into the minimum de-mag time. The bench test shows that it is required to set up $t_{DMAG\ (min)} > 2.2$ µs along with a proper body diode conduction time of t_{BW} of the SR MOSFET, that is, *bump* time is to be designed with a value of $t_{BW} \geq 750$ ns. The 750 ns time for t_{BW} is necessary to adapt the UCC28704 internal filter time. If these particular time requirements are not being met, PSR converter output voltage V_o knee point sensing results become erratic. The converter output V_o may then present irregular-shape ripples. Figure 3 shows an example of what typical irregular-shape ripples look like. An irregular-shape ripple from higher magnitude may result if DMAG (min) is further reduced. The highest V_o ripple observed with an irregular shape with peak-to-peak value can be over 400 mV on a 5V-output design on bench tests. The irregular ripples occur in the AM range of the UCC28704 where the switching frequency is fixed at 25 kHz with variable peak current. The irregular-shape ripple magnitude can be reduced to an acceptable level or eliminated by properly designing both minimum de-mag time, $t_{DMAG\ (min)}$, and bump time, t_{BW}.

Both analysis and bench tests show minimum de-mag time, $t_{DMAG\ (min)} > 2.2$ µs, is required along with bump time $t_{BW} \geq 750$ ns. However, $t_{DMAG\ (min)}$ may need to be designed with a typical value of 2.4 to 2.5 µs to have enough margin to cover parameter variations due to tolerance concerns.

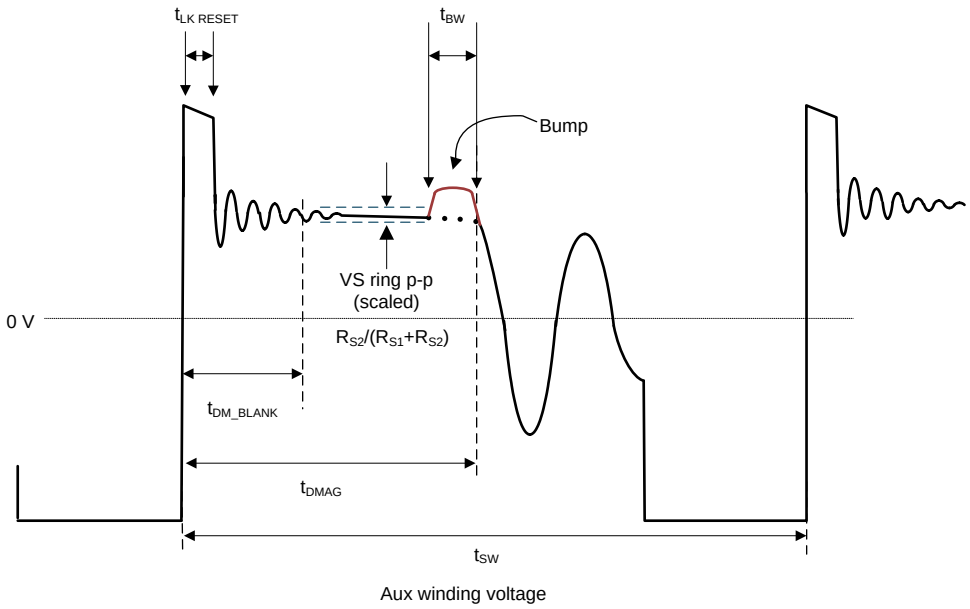

Figure 2. De-mag Time Partition and Body Diode Conduction Bump

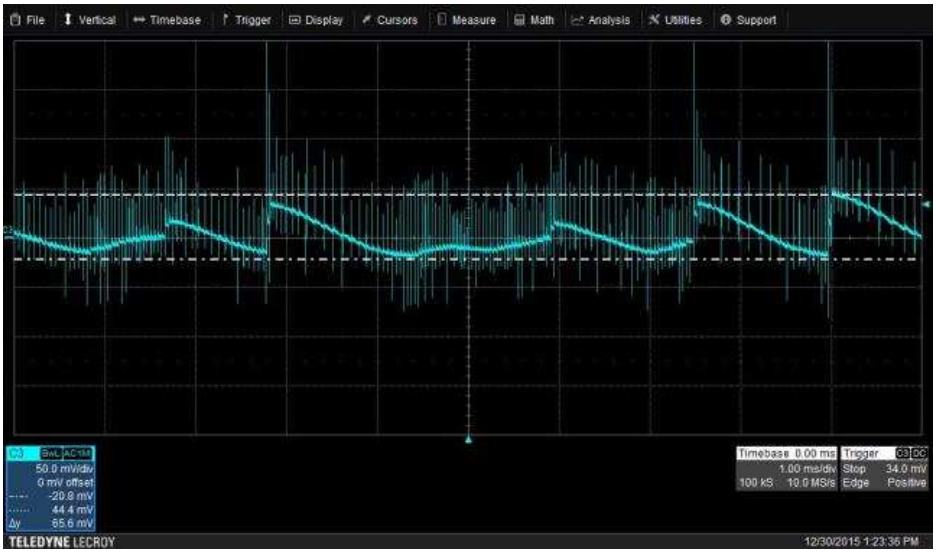

Figure 3. Output Voltage Ripple Irregular Waveforms

2 How to Design the Required Minimum De-mag Time

The required minimum de-mag time, $t_{DMAG\ (min)}$, can be designed by properly setting up the transformer inductance. As in a flyback converter with discontinuous conduction mode (DCM) operation, the transformer inductance design is associated with the switching frequency. The required de-mag time can be designed by setting up the maximum switching frequency from approximately 50 kHz but not exceeding 55 kHz at any time. This process ensures a design with the required minimum de-mag time, $t_{DMAG\ (min)}$, from approximately 2.4 to 2.5 µs.

The following criteria must be met for the UCC28704 when designing with the UCC24636:

(a) Operational maximum switching frequency of f_{sw} < 55 kHz, which achieves minimum de-mag time of $t_{DMAG\ (min)}$ ≥ 2.4 µs.

(b) SR MOSFET body diode minimum conduction (bump) time of t_{BW} (min) ≥ 750 ns.

When using the UCC24636 with other controllers, this criteria is still applicable. The frequency limit in item (a) can usually be extended to a higher value for other PSR controllers, such as the UCC2870x, UCC2871x, UCC2872x, and UCC28730. When using the UCC24636 with these controllers, due to different internal parameters, these devices can meet $t_{DMAG\ (min)}$ ≥ 2.4 µs with higher maximum switching frequency.

Item (b) applies to designs with the secondary-side using an SR MOSFET but not with a Schottky diode in parallel connection. A Schottky diode in parallel connection to the SR MOSFET can be used to operate with a switching frequency > 55 kHz without causing the V_o irregular ripple.

3 How to Design the Required Bump Time When Using the UCC24636

The *bump time* is the time from the initial MOSFET body diode turnon to when the transformer secondary winding current is reduced to zero after the SR MOSFET turns off as shown in Figure 4 with Bump-1 or Bump-2. The voltage drop difference from MOSFET Rds (on) to the MOSFET body diode reflects the primary causes of the bump on the auxiliary winding voltage output as shown in Figure 2. When the SR MOSFET turns off early, a longer time bump occurs in Bump-1 (a to c) in Figure 4. Similarly, when SR MOSFET turns off late, a shorter time bump is obtained as shown in Bump-2 (b to c).

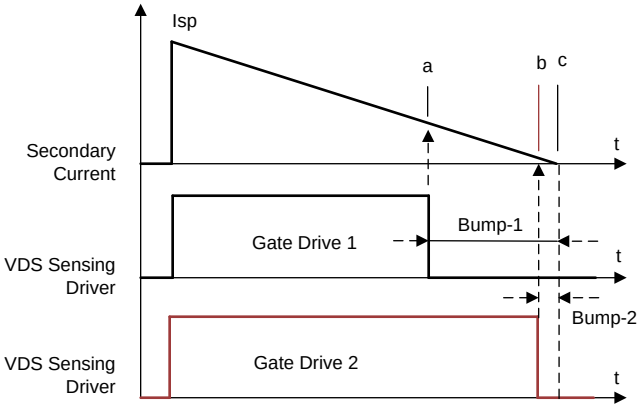

Figure 4. Bump Time Setup With the UCC24636

The SR gate drive time is programmable with the UCC24636 using four resistors: RVPC1, RVPC2, RVSC1 and RVSC2, as shown in Figure 1. The minimum bump time, t_{BW} (min), becomes programmable to achieve the minimum 750 ns requirement. The UCC24636 data sheet provides an example of how to design these four resistors for a 15W ac-dc converter with 5V-3A output. Universal AC Input to 5V/3A Output Reference Design DOE6 and COC V5 Tier 2 Compliant is available for evaluation for using the UCC28704 and the UCC24636. The same steps apply to other power level converters such as a 10W, 5V-2A converter.

After obtaining initial values for t_{BW} (min), the values may require tuning on the bench to get the final design target of 750 ns for the bump time of t_{BW} (min). RVSC1 should be used for the bump adjustment as it helps change the bump time while not having other effects. Usually RVSC1 tuning is enough to achieve the required bump time of t_{BW} (min). The bump time of t_{BW} (min) and the minimum de-mag time are tuned and measured at high line input voltage and with minimum load when the bump appears.

4 Effect of the Schottky Diode in Parallel With the SR MOSFET

Figure 5 provides the High Efficiency Universal AC Input to 5V 2A Adapter Reference Design of its SR circuit portion. This PMP11600 reference design is for high-efficiency universal ac input to 5V-2A output PSR flyback converter using the UCC24636 to drive SR MOSFET, Q1, on the secondary-side, and to work with the UCC28704 PSR flyback controller on the primary-side. A Schottky diode, D9, is connected in parallel with Q1 from its drain pin to its source pin. In removing D9, irregular output voltage ripple will occur. To eliminate the irregular ripple, this design must meet the two design criteria discussed in Section 2.

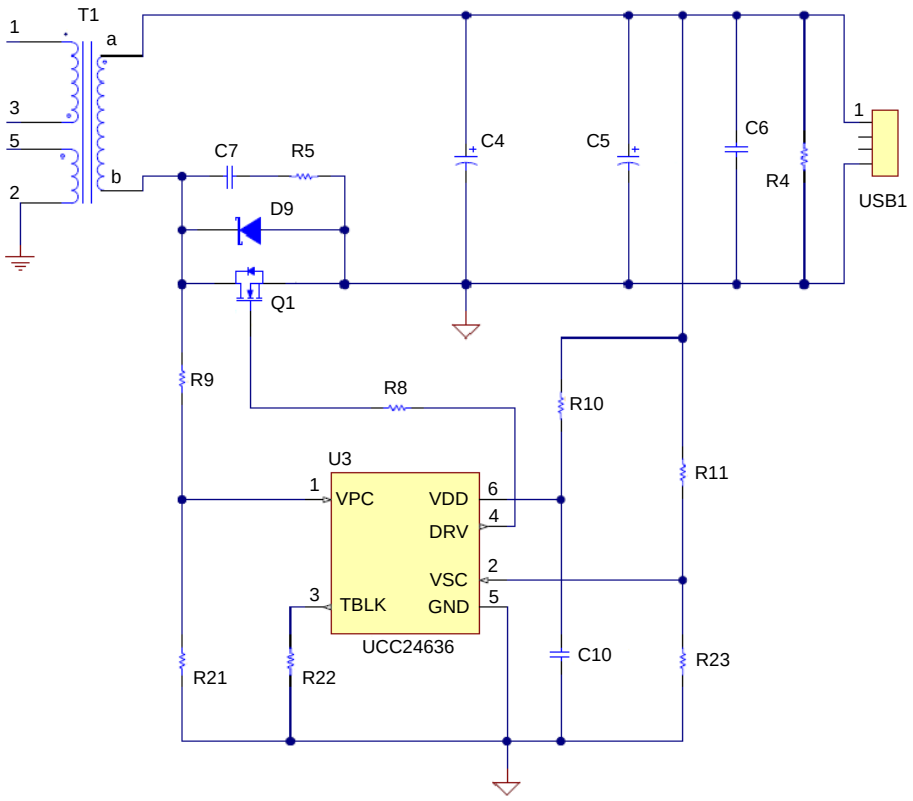

Figure 5. PMP11600 Part of Circuit Showing SR With a Schottky in Parallel

As a Schottky diode forward voltage drop is much lower than that of a MOSFET body diode, one concern is the amount of additional power loss if the Schottky diode is removed. Efficiency tests were conducted on the PMP11600 with the Schottky diode and without the Schottky diode.

The efficiency test results with and without the Schottky diode are illustrated in Figure 6. Table 1 provides the average efficiency difference comparison. Based on the test data, the Schottky diode helps to increase the average efficiency of 0.66% at low line (115V ac) and 0.48% at high line (230V ac). The test results indicate the Schottky diode has small efficiency improvement but is associated with a cost increase. When efficiency performance is adequate and meets the specifications, removing this Schottky diode from a design helps to achieve cost-savings and reduce component count.

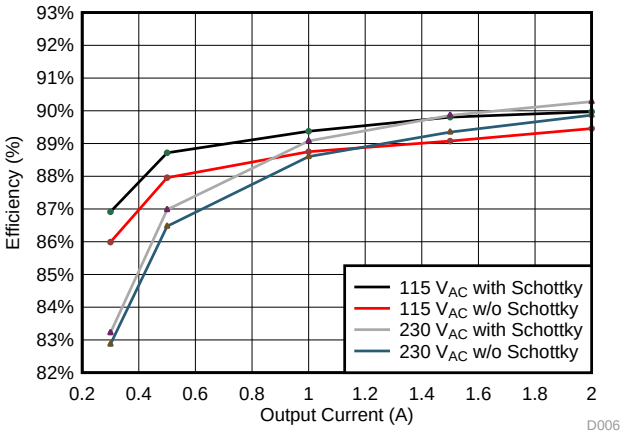

Figure 6. PMP11600 5V2A Converter Efficiency Test Result

Table 1. Efficiency Comparison

Vin	Schottky	Efficiency	
		Average	Increase
115 V_{ac}	With	89.47%	0.66%
	Without	88.81%	
230 V_{ac}	With	89.05%	0.48%
	Without	88.57%	

5 Summary

This application report describes how to design the UCC28704 with the UCC24636 without a Schottky diode in parallel with the SR MOSFET on the secondary-side in a PSR flyback converter. Based on the analysis and bench tests, two design criteria are required to observe and to eliminate the irregular-ripple output voltage or reduce the ripple magnitude to an acceptable level:

1. Design maximum operational switching frequency no greater than 55 kHz to achieve a minimum de-mag time of $t_{DMAG\ (min)} \geq 2.4\ \mu s$.
2. Design the SR MOSFET body diode conduction, or bump time, of tBW (min) ≥ 750 ns.

Both conditions are required to be true through bench tune-up with high-line input voltage and with MOSFET body diode conduction bump time present at a minimum-load operation of a converter.

The design criteria described in this report applies to cases where a Schottky diode is not used in parallel with the SR MOSFET, and the criteria is particularly applicable for the designs with the UCC28704 and the UCC24636. When a Schottky diode is used in parallel connection with the SR MOSFET, the maximum switching frequency can be extended to the range specified in the data sheet.

In addition to the effect of the switching frequency from the paralleled Schottky diode, the Schottky diode presents efficiency influence. The bench test shows the efficiency from this Schottky diode typically exists in a sub 1% range. Therefore, when the efficiency requirement can be met and when the switching frequency is acceptable, the Schottky diode can be removed from a design to achieve cost-savings and component count reduction.

6 References

1. Texas Instruments, UCC28704 High-Efficiency Off-Line Constant-Voltage and Constant-Current Flyback Controller With Primary-Side Regulation (PSR) Data Sheet
2. Texas Instruments, UCC24636 Synchronous Rectifier (SR) Controller With Ultra-Low Standby Current Data Sheet
3. Texas Instruments, PMP11600 High Efficiency Universal AC Input to 5V 2A Adapter Reference Design
4. Texas Instruments, PMP15002 Universal AC Input to 5V/3A Output Reference Design DOE 6 and COC V5 Tier 2 Compliant

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