Application Report

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bq77905 Using Multiple FETs

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BMS: Monitoring and Protection

ABSTRACT

The basic implementation of the bq77905 3-5S Low Power Protector for lithium ion batteries uses single charge and discharge FETs for current control. This document shows circuit implementation examples of driving multiple charge and discharge FETs when using the bq77905. The schematic examples and test results will help the battery electronics designer when designing a pack with multiple FETs for charge and discharge.

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1 Introduction

The bq77905 3-5S low power protector is an easy to use component for lithium ion battery circuits. The common schematic uses series FETs where the current for both charge and discharge flows through single charge and discharge FETs in series. See Figure 1. R_{DSG} and R_{CHG} are sized for appropriate switching speeds of the transistors, and in some cases additional circuitry may be used in the charge path to accommodate system voltages. Refer to the datasheet for additional description.

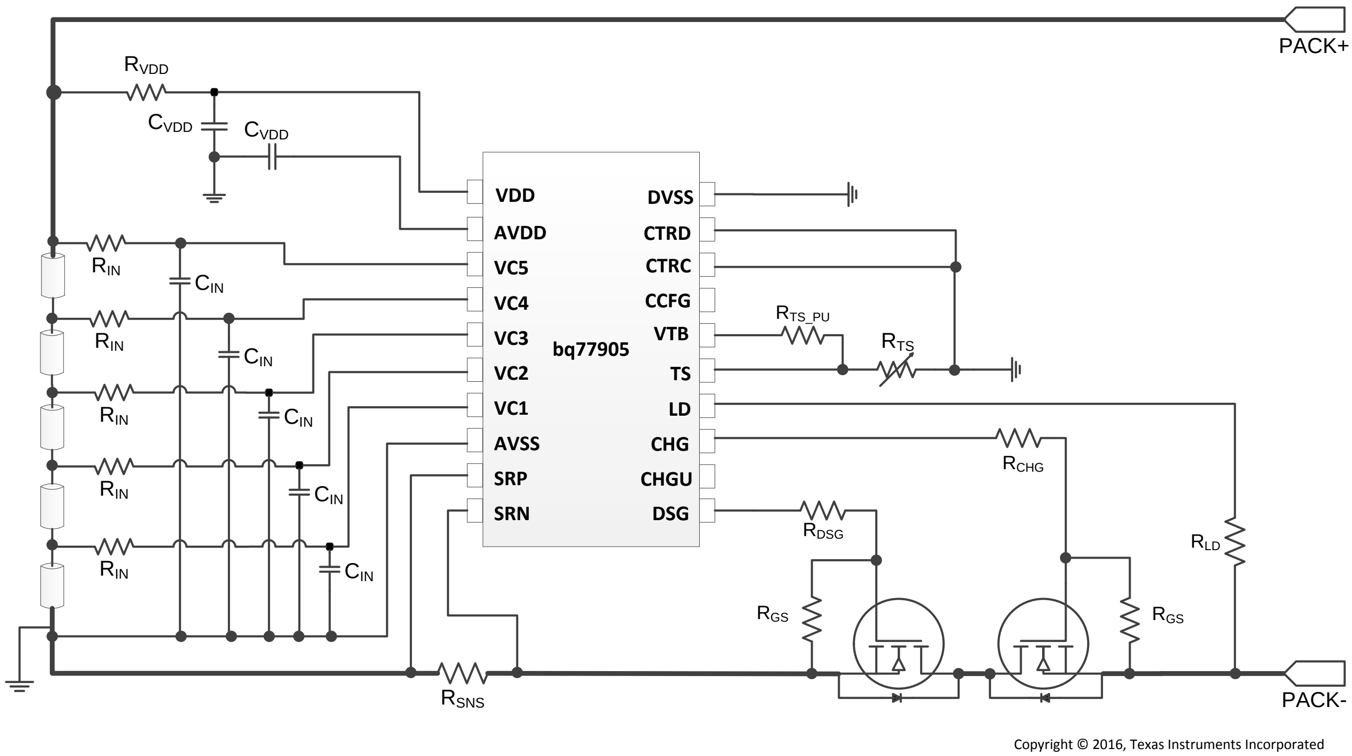

Figure 1. Common Implementation

2 Multiple FETs

In some cases, it may be desirable to use multiple FETs in parallel for both the charge and discharge FETs. This may be either for increased current handling or to spread heat over a wider area. Consult industry references or your FET manufacturer for recommendations on paralleling FETs. It is generally recommended to keep the circuit symmetrical and the FETs at the same temperature for equal current sharing. With parallel FETs, the driver sees a larger load. The bq77905 has drivers with low internal resistance and can accommodate the larger total gate load, refer to the datasheet feature description and electrical characteristics for details. When driving the parallel FETs, it is generally desirable to keep the signal to the gates the same while maintaining some isolation between the gates to avoid oscillation. Ferrite beads or a small portion of the total resistance is often used for gate isolation. Figure 2 shows a circuit implementation with 4 parallel MOSFETs. In the DSG drive circuit the R_{DSG} is split between a common resistance R8 and smaller individual gate resistors R14, R19, R21, and R23. The CHG circuit is more complex since it limits the gate voltage to the FETs during transients and blocks the current into the CHG pin during a discharge protection with load. The R_{CHG} for turn on is provided by the common R9 and the individual R15, R20, R22 and R24. For CHG turn off the drive resistance is dominated by R13 in parallel with R17 until PACK- falls below GND, then the remaining turn off is through R17.

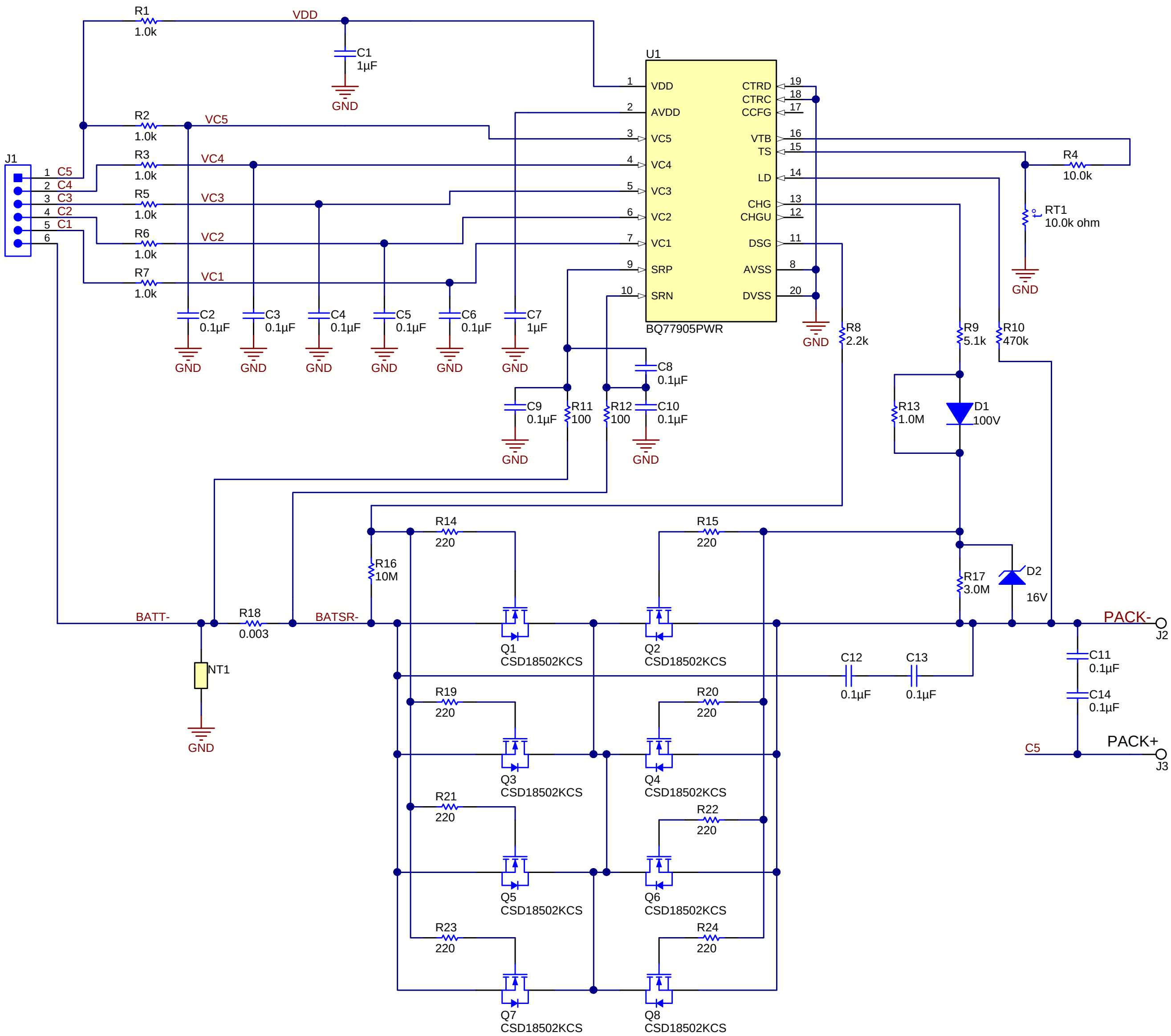

Figure 2. Schematic With Multiple FETs

When PACK+ is shorted to PACK-, a high current flows from the battery limited by the capability of the cells and the resistances of the circuit, interconnect and short. When the current exceeds the short circuit threshold for the protection delay, both DSG and CHG are turned off. Figure 3 shows the turn off of the discharge FET from a short circuit protection event with the Figure 2 circuit. When DSG is turned off, the R_{DSG} resistances allow the discharge FET gates to fall slowly so the current drops from over 100 A to 0 slow enough to avoid a large transient from the cell inductance and current transition. Although CHG turns off, the high resistance of the turnoff path and the FET's gate capacitance keep the charge gates high during the short time shown in the figure.

NOTE: Waveform captures in this document show charge current as positive.

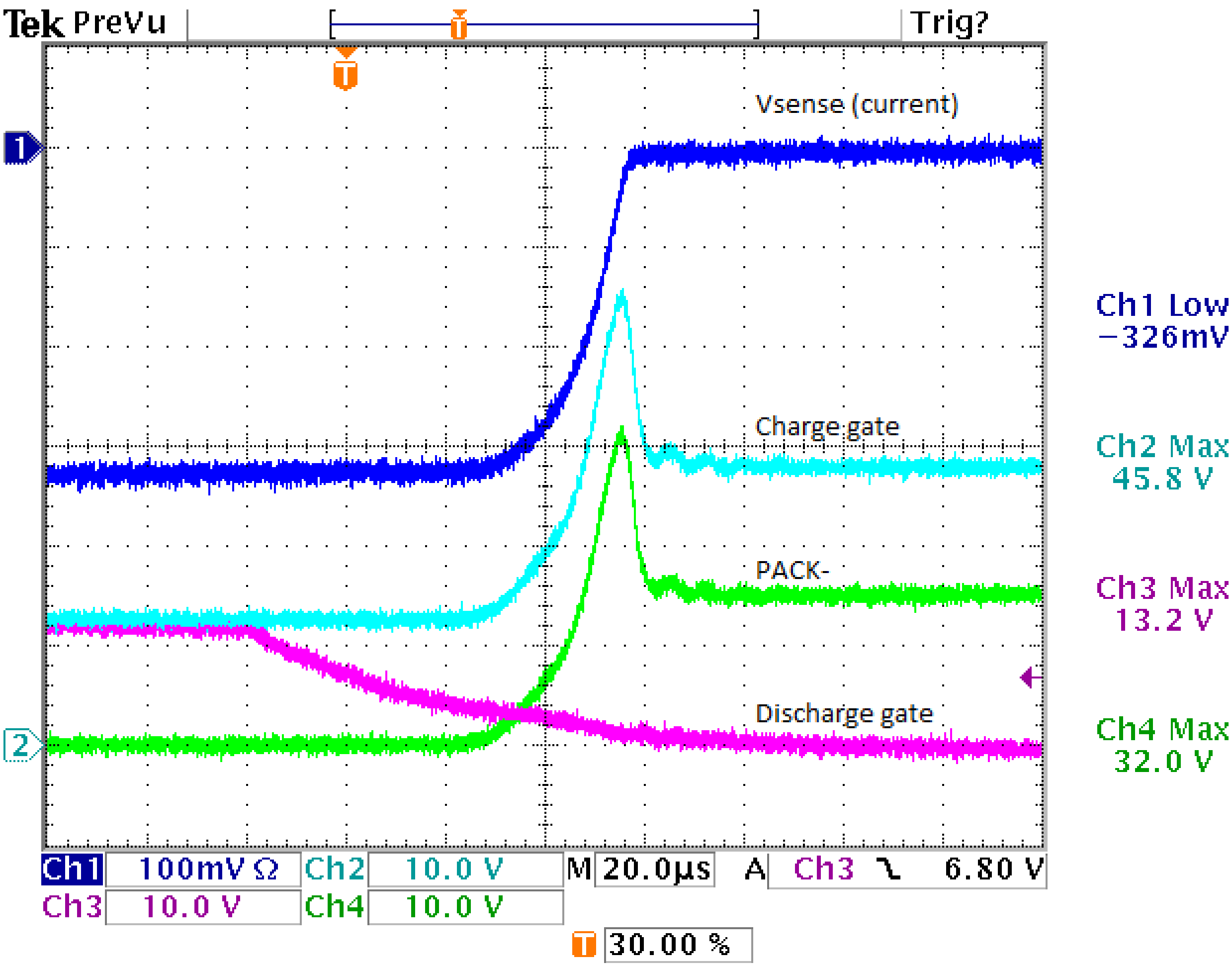

Figure 3. Short Circuit With Multiple FETs

During an undervoltage protection turn off as shown in Figure 4, the discharge FET gates again fall slowly but the transient on PACK- is lower due to the smaller current and higher resistance of the load. The bq77905 keeps CHG on during the undervoltage event, but it is not apparent since the charge gates rise again in the short term due to the gate capacitance.

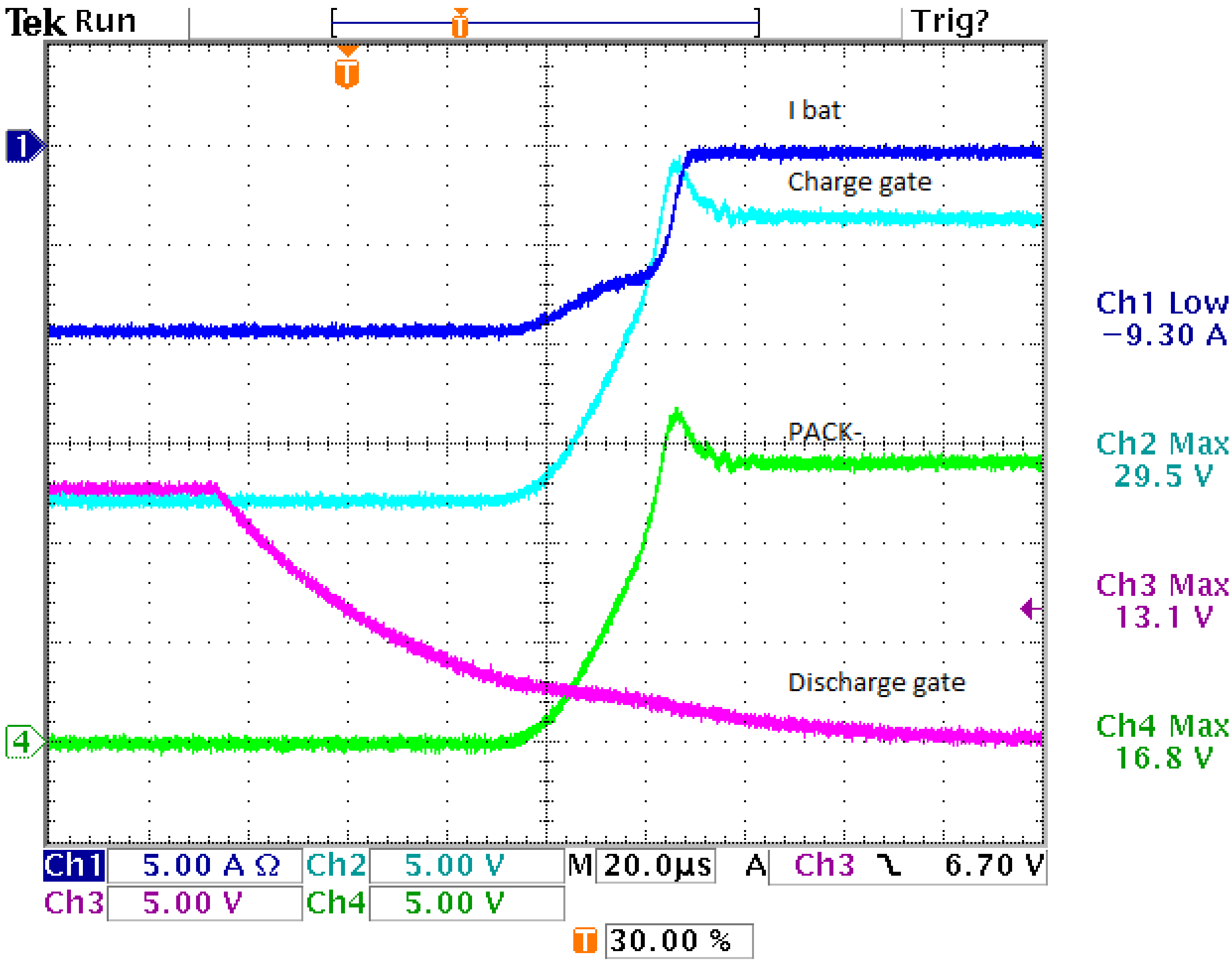

Figure 4. Undervoltage With Multiple FETs

When the charge output is turned off from a protection event such as overtemperature during charge as shown in Figure 5, the high resistance of the turn-off path provides a slow turn off of the FET. The typical R_{GS_CHG} is large to avoid the CHG output voltage from preventing load removal when a bq77905 with the load removal for UV recovery option is used and to reduce constant current into the resistor when CHG is on. The turn-off time can be faster with a smaller R_{GS_CHG} resistance when the load removal for UV recovery option is not used. For systems where the charge current is small, the delay time to the drop in current and the slow transition time may be acceptable, but for higher charge currents a different technique may be desired.

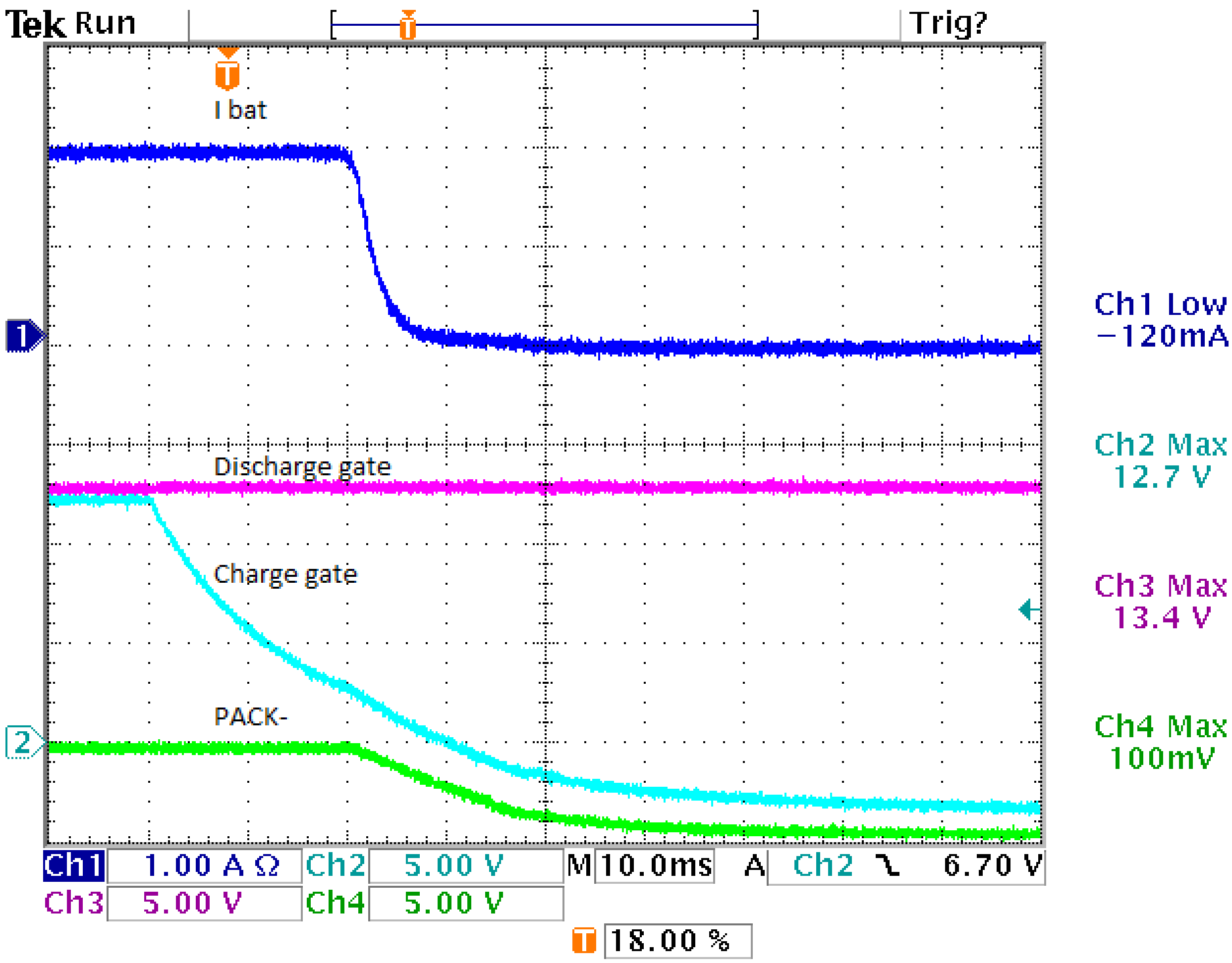

Figure 5. Overtemperature Charge With Multiple FETs

3 Increasing the Charge Turn Off Speed

When using multiple FETs, the R_{GS_CHG} resistance which turns off the charge FETs may allow a long turn-off time and result in FET heating or failure. It may be desirable to add a circuit to speed up the turn off of the charge FETs. With high impedance drivers and fast switching, adding a PNP transistor to pull down the FET gate as shown in figure 31 of SNVA008 is a common technique. Since R_{GS_CHG} is large in the bq77905 circuit, voltage control of a P-channel FET is more appropriate as shown in Figure 6. In this circuit the R_{GS_CHG} is split between R17 and R25. D3 turns on the FET gates when CHG is high, Q9 pulls down the gates when CHG is turned off and R17 pulls Q9's gate down. It is important that the V_{GSTH} of Q9 is lower magnitude than V_{GSTH} of the charge FETs so that Q9 is still conducting as the charge FETs turn off. The charge FET gate voltage pull down continues by Q9 until it turns off, then by R25.

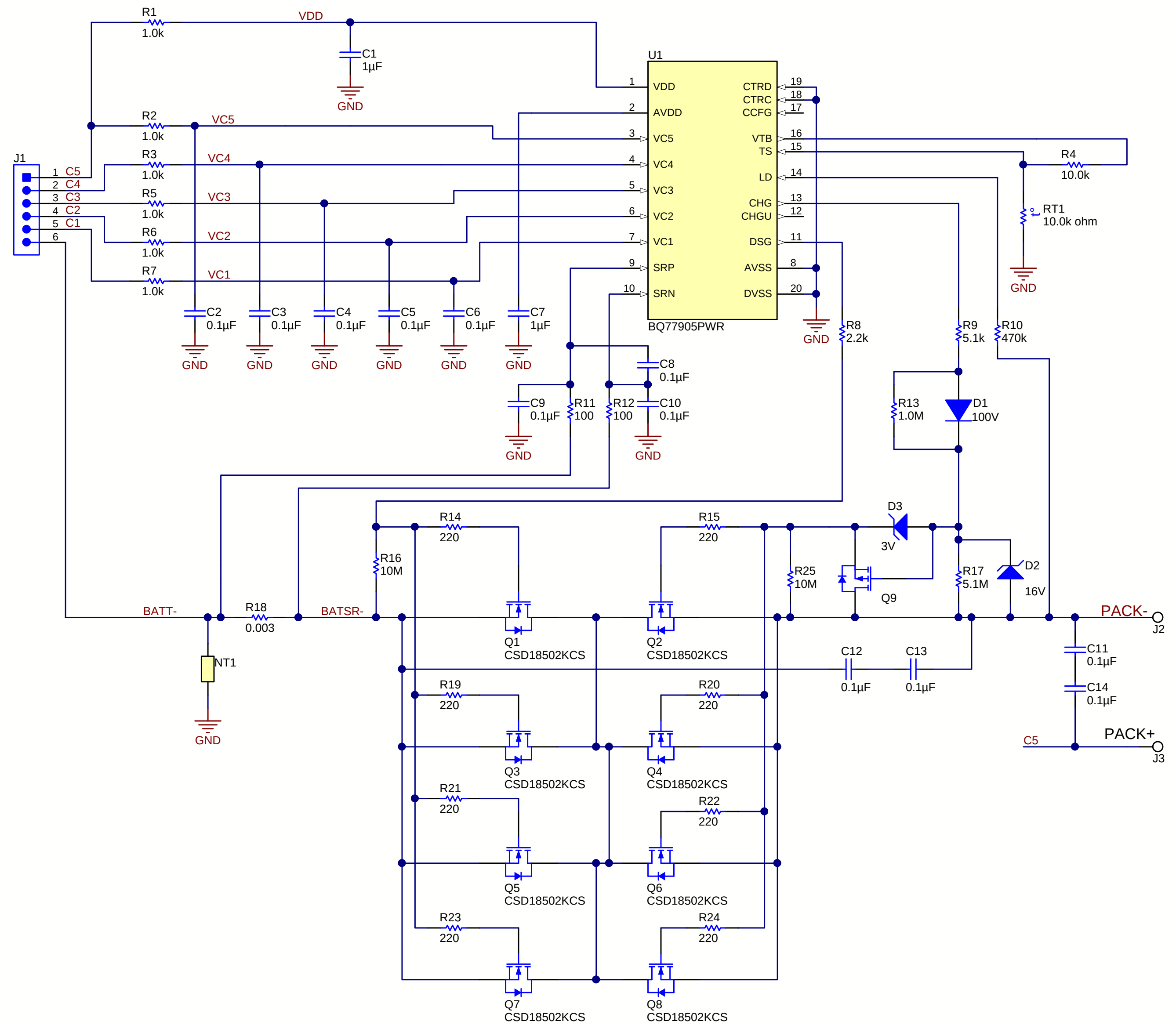

Figure 6. Schematic With Faster Charge Disable

Figure 7 shows the improved charge turn-off time of the circuit in Figure 6. The circuit was tested with a FDN340P FET for Q9 although other FETs such as CSD25483F4 may be appropriate depending on the power FET selected. Other circuits to speed up the switching may be desired depending on the application.

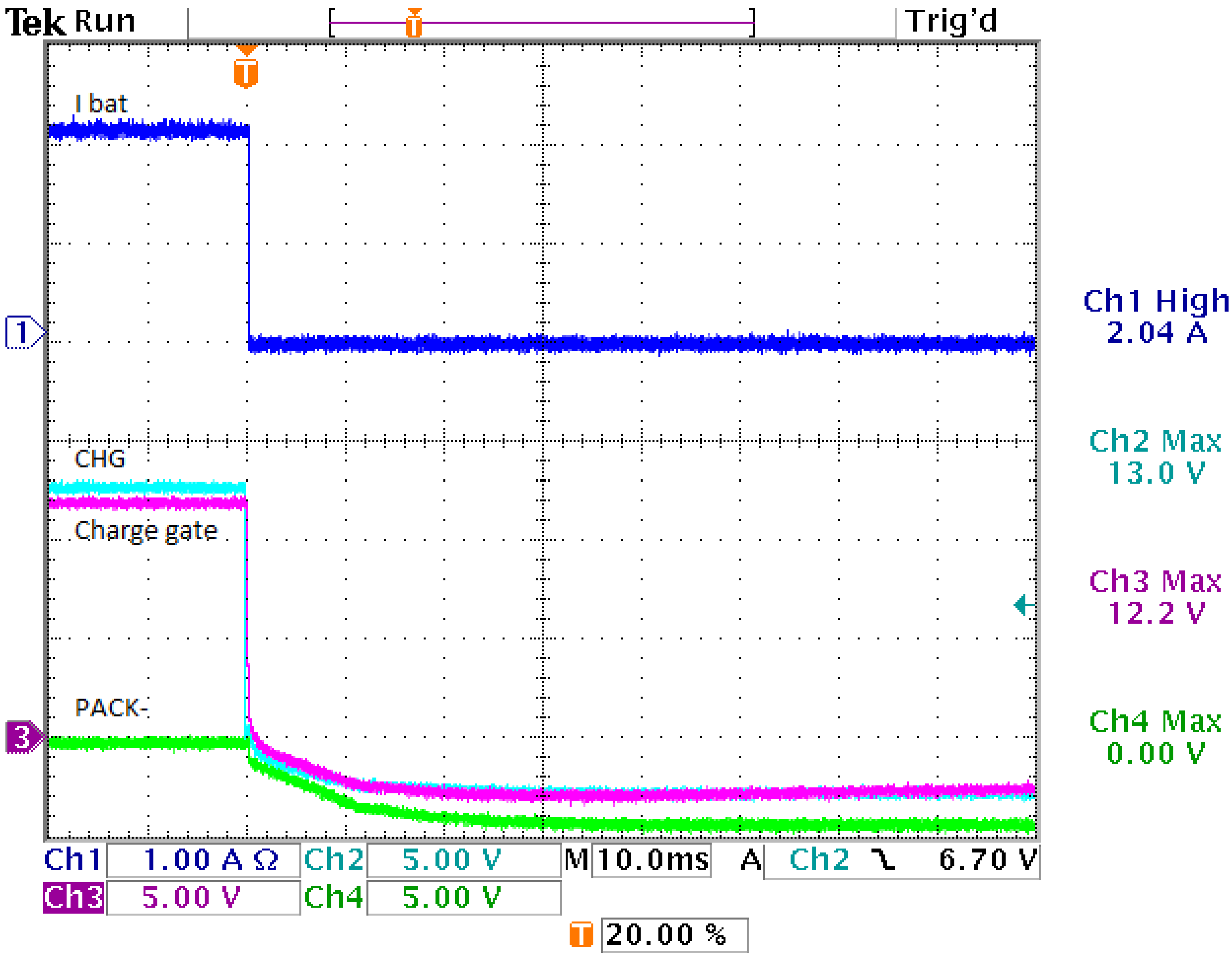

Figure 7. Overtemperature Charge With Faster Charge Disable

4 References

For additional information, refer to the documents below available at www.ti.com.

- *bq77904 / bq77905: 3-5S Low Power Protector* data sheet (SLUSCM3)
- *bq77905 EVM User's Guide* (SLVUAN2)
- *AN-558 Introduction to Power MOSFETs and Their Applications* (SNVA008)

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