Application Report
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Not All Jitter is Created Equal: Understanding Jitter in Switching Power Supplies

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ABSTRACT

This application report offers a tutorial discussion on jitter in switching DC-DC converters. Not all power supply designs are equally susceptible to jitter, nor are they equally affected by jitter. Modes of switching jitter are defined and explained for several popular control architectures, which are then analyzed for sources of jitter. An example contrasting the amount of jitter and effect on output voltage caused by this jitter is included, using a closed-loop time domain simulation.

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Introduction

A common issue faced by designers of DC-DC switching power supplies is switching jitter. At steady state, a switching converter is expected to produce a very consistent pulse train, but often when prototypes are evaluated, the designer will see some noticeable inconsistency in the on-time, off-time, or frequency of the switching their converter produces, even for a constant DC resistive load.

This application note explores the architecture of common power DC-DC converters to explain the reason jitter occurs, why it affects different designs differently, and the system level effects it causes.

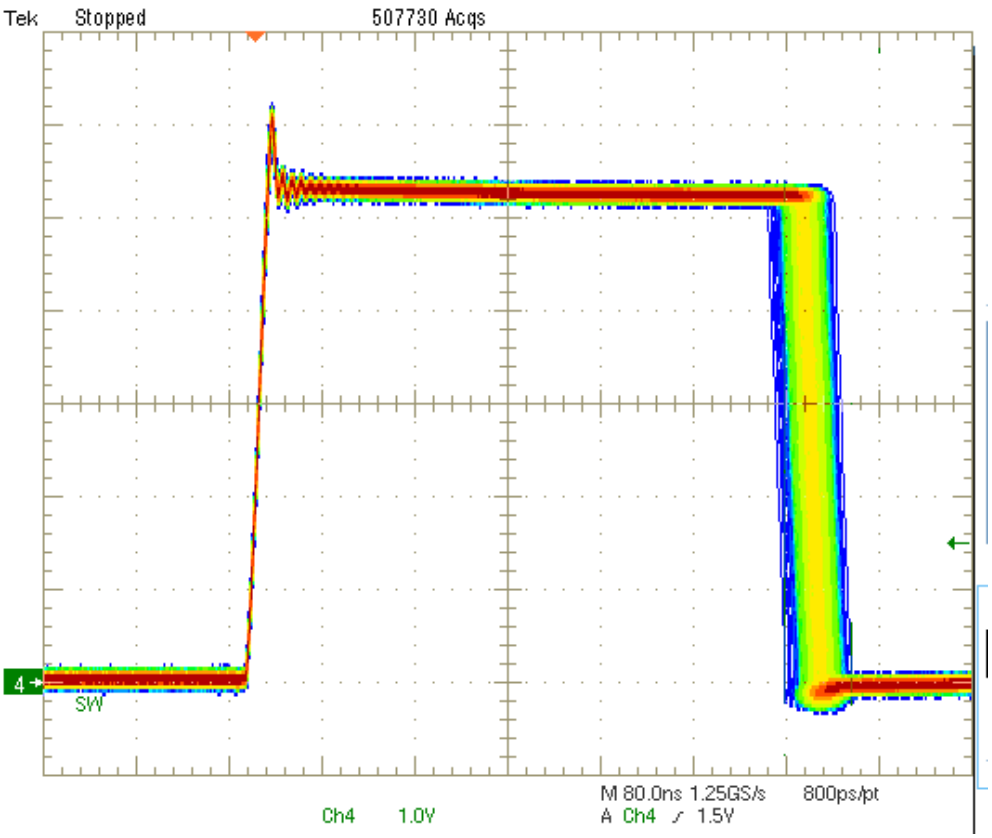

Figure 1 - Typical Switching Jitter

Background

Switched-mode DC/DC converters are composed of a few fundamental pieces – a power source, a power switch, and an averaging filter. A control loop *decides* when to toggle the power switch, as necessary to maintain a regulated output whether at steady-state, or in the presence of changing conditions. This decision is made at the *modulator*, which is controls the amount of time the power switch conducts (on-time), and the amount of time it does not (off-time). This control is often represented as pulse train, which represents the output of the modulator. By convention, when the pulse train waveform is high, the power switch is on, and likewise

As soon as a converter has reached steady-state, ideally, its switching waveform should remain completely uniform. Figure 2 shows an ideal pulse train waveform, with constant on-time, constant off-time, constant duty cycle, and hence constant frequency.

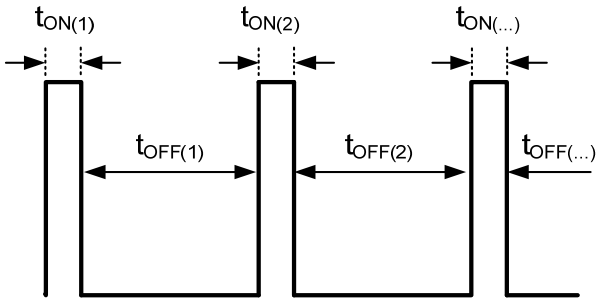

Figure 2 - Ideal Modulator Output Pulse Train

In practice, however, no converter topology or control scheme is capable of producing 100% ideal switching. Such a scheme would require infinite noise margin. Real DC/DC converters always include some variability in the on-times and off-times they produce, regardless of the stability of their control loop. This variability is referred to as jitter.

There are three general types of jitter:

- **On-Time Jitter** - Variability in the power switch on-time. See Figure 3.
- **Off-Time Jitter** - Variability in the power switch off-time. See Figure 4.
- **Frequency Jitter** – Variability in the switching frequency. See Figure 5.

Clock-based linear control schemes such as voltage mode control (VMC) and current mode control (CMC), are primarily susceptible to on-time jitter only, where nonlinear constant on-time (COT) and pulse frequency modulation (PFM) schemes are primarily susceptible to off-time jitter only. Frequency jitter is often created intentionally in a converter, as a way of spreading switching noise across multiple frequencies. This technique is known as *frequency spread spectrum*.

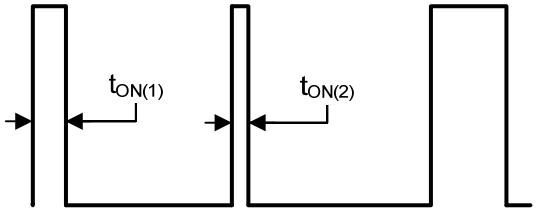

Figure 3 - On-Time Jitter

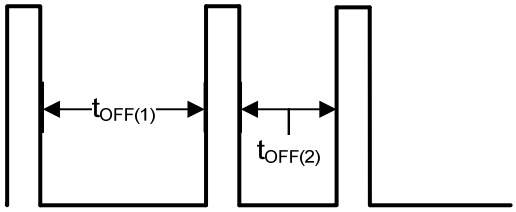

Figure 4 - Off-Time Jitter

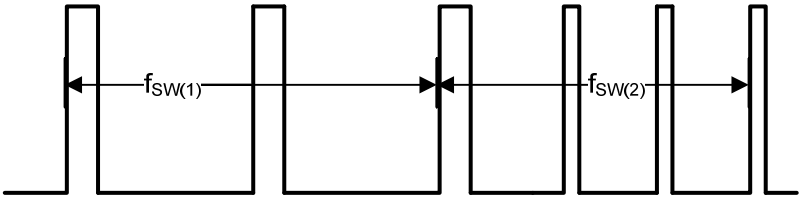

Figure 5 - Frequency Jitter

Understanding Causes of Jitter for Common Control Schemes

Modulator Noise Margin

The central cause of jitter in switching DC/DC converters is a concept known as *noise margin*. All switching DC/DC converters exist in a noisy environment, but not all control schemes are equally affected by noise.

A good starting place in any analysis of jitter is the *decision point*. Every converter control scheme works by making a comparison of current conditions to desired conditions, then measuring its response to bring the current conditions closer to those desired. The final stage of this comparison, the one which actually controls the action of the power switches based on control information, is referred to as the *modulator*, which is often implemented as a simple comparator. The decision point is moment at which the modulator output toggles, and jitter is any inconsistency in this *decision*. Because the *decision* occurs at the modulator, any architectural cause of jitter must be present at the modulator inputs.

An important factor in determining how much variability in output results from a given amount of noise is the *gain* of the modulator – that is, how greatly a given amount variability in its input signals causes its output decisions to change.

Schemes which use small amplitude signals, or very similar signals at the inputs of their modulator are therefore more susceptible to jitter. This is because a small amount of noise can cause a larger difference in the pulse train produced versus a control scheme which uses larger amplitude signals. This effect is shown for the case of voltage mode control, current mode control, and DCAP™ control schemes in the next sections.

Voltage Mode Control

Figure 6 shows a block diagram of voltage mode control with trailing edge modulation. This is the control scheme used by several of TI's most popular converters such as TPS40055, TPS40304, TPS56221, and TPS54550, among many others.

As in any trailing edge modulation scheme, the output latch is set by an oscillator clock, closing the power switch (high-side FET); the control loop operation determines when switch opens, or the falling edge of the pulse train signal (turn-on of the low-side FET for a synchronous converter). For voltage mode control, a compensated error amplifier compares the output voltage to a voltage reference to generate Vc, or the control signal.

The control signal is then compared at the modulator to a voltage ramp that runs at the oscillator frequency. When the control signal, Vc, intersects the voltage ramp, the output of the modulator is toggled high, resetting the latch and turning off the power switch.

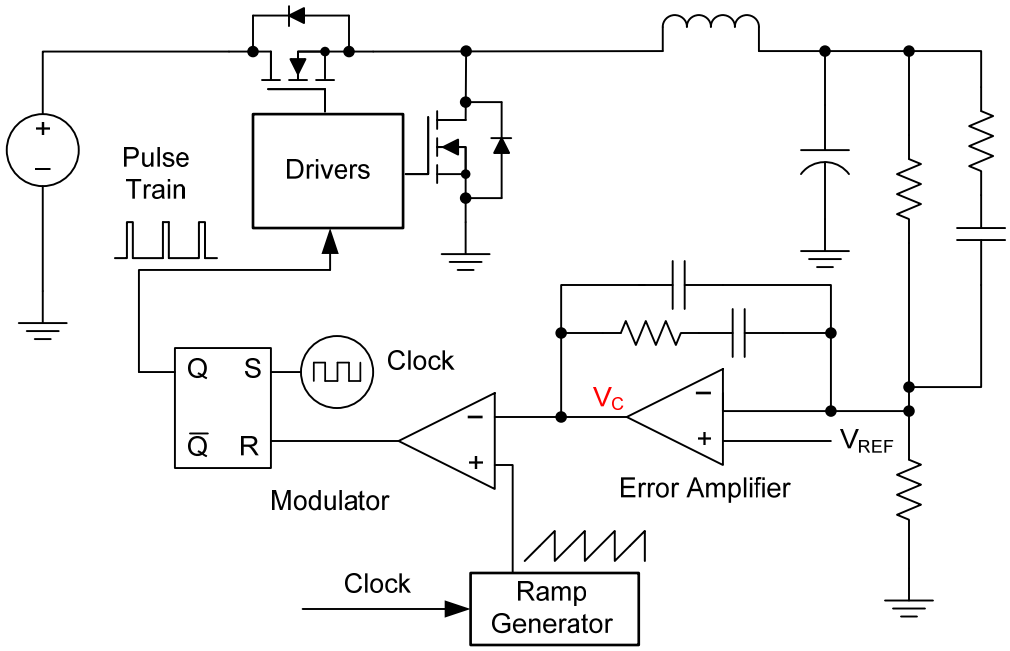

Figure 6 - Voltage Mode Synchronous Buck Converter

Figure 7 and Figure 8 show the real and ideal modulator waveforms for a voltage mode converter. Because the rising edge of the pulse train is initiated by a constant frequency clock, it can be seen that there is little opportunity for noise to corrupt its output on the rising edge, and little opportunity for noise to affect the frequency of operation (outside of affecting the clock signal).

For this reason, jitter in voltage mode converters is dominated by to on-time jitter alone, with almost no variation in frequency.

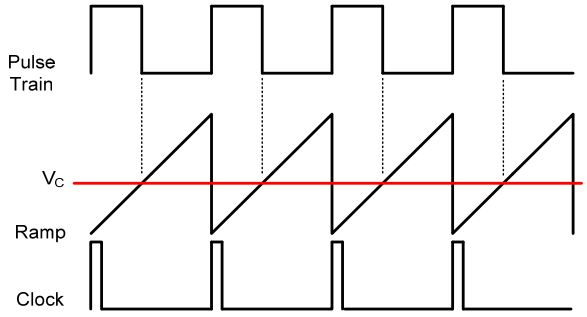

Figure 7 - Ideal Modulator Waveforms

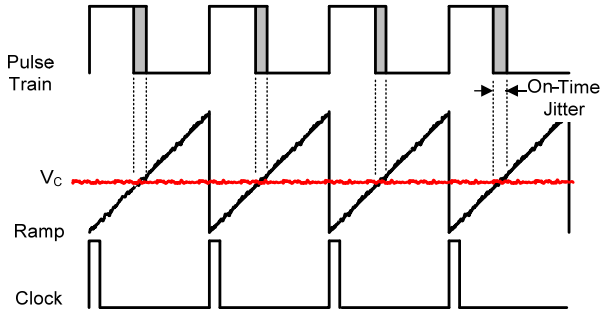

Figure 8 - Real Modulator Waveforms

One can see, however, that noise can cause some variability at decision point, which dictates the falling edge, and pulse width. In reality, neither the control signal, nor the ramp signal is completely free of noise. As the control signal and ramp approach each other, they eventually enter a region where even a small amount of noise this enough to trigger the modulator to transition.

Because the exact decision point is defined as the intersection point of two non-ideal signals, there will be some probabilistic variation in the exact decision point, and hence in the pulse train signal produced. Hence, as the decision point approaches, the noise margin decreases, until finally the decision to turn off the power switch is made.

One common variant of the voltage mode control scheme implements input feed-forward by making the ramp amplitude proportional to the input voltage. This allows the system to respond quickly to input transients. This scheme also, however, decreases the slope of the ramp signal at low input voltages, hence making these conditions more susceptible to jitter.

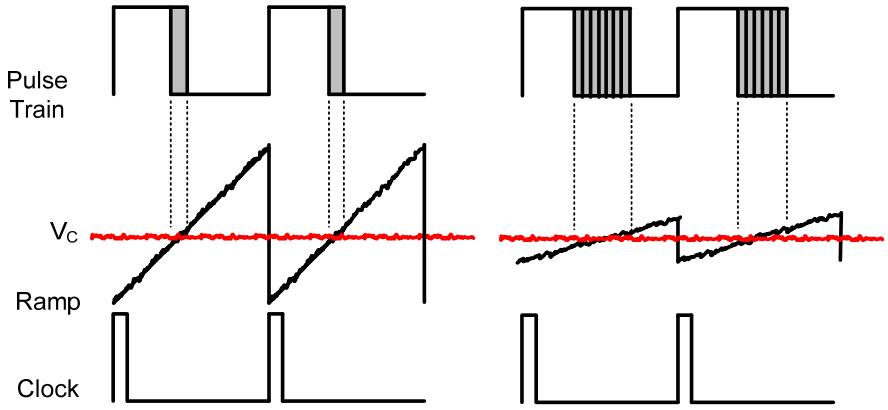

Figure 9 - VM Modulator Noise Margin vs. Ramp Slope

For a standard off-the-shelf voltage mode controller, the ramp signal is generated internally, and is not dependent on external components. Voltage mode controllers are designed such that the amplitude of their ramp signal is relatively large (between 1 V and 2 V), which is very large compared to the amount of noise on either the control or ramp signals. Hence, the voltage mode control scheme is usually quite immune to jitter when designed properly. A typical voltage mode converter may only have 20 ns of jitter at steady state.

Peak Current Mode Control

Another popular trailing edge modulation control scheme is peak current mode control, as shown in Figure 10. Peak current mode control is a popular scheme for modules and integrated FET converters, due to simplified control loop stabilization. This scheme is employed by many TI converters such as TPS54620, and TPS54418.

In a peak current mode control converter, the control signal is used to limit the peak current the converter supplies, while an outer voltage loop adjusts the control signal to maintain a regulated output. A clock turns on the power switch, and the modulator compares the switch current to the control signal, terminating the pulse when the switch current reaches the control signal. Most modern peak current mode controllers will also apply slope compensation. Slope compensation is added to the sensed current signal to eliminate the possibility of sub-harmonic oscillation when the commanded duty cycle is greater than 50%. This property of peak current mode control is discussed thoroughly in SLUA101.

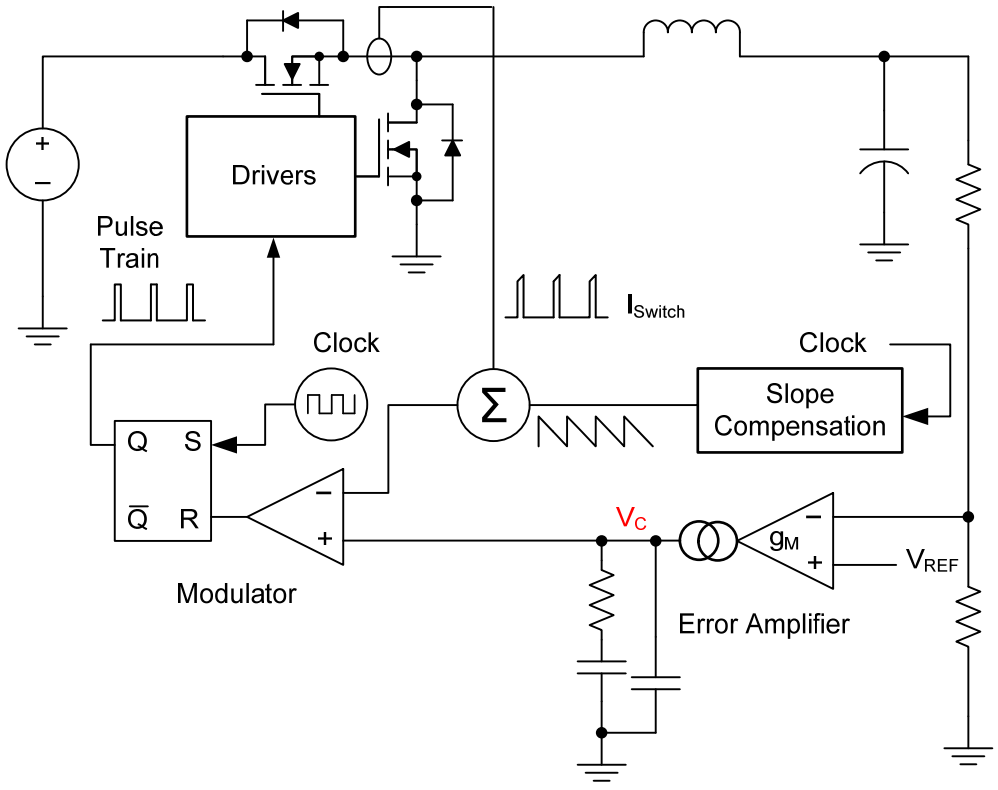

Figure 10 - Peak Current Mode Control

Figure 11 and Figure 12 show the modulator waveforms for a peak current mode control converter. As noted before, any architectural source of jitter must be present at the inputs to the modulator. Again, because the turn-on of the power switch is initiated by a constant frequency clock, there is little opportunity for noise to interfere with the rising edge of the pulse train signal, or its frequency. The turn-off is controlled by the modulator which compares the switch current and the slope compensated control signal, and hence is susceptible to the noise margin of this intersection.

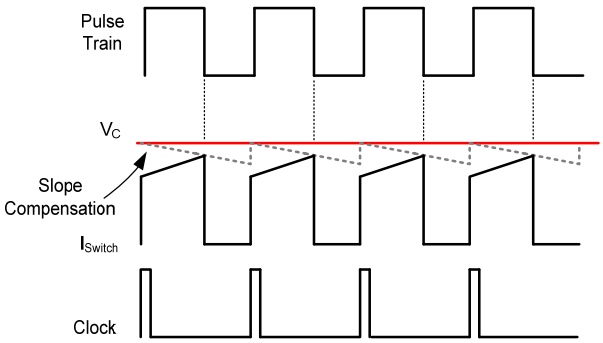

Figure 11 - Peak Current Mode Control Ideal Modulator Waveforms

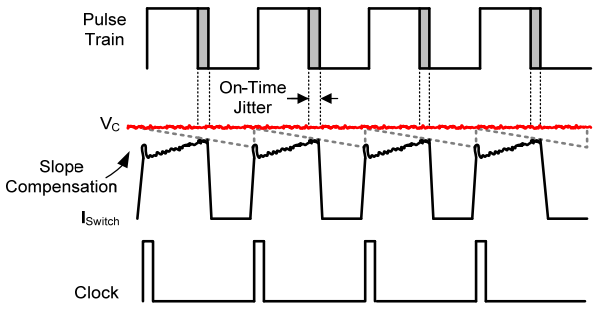

Figure 12 - Peak Current Mode Control Real Modulator Waveforms

The most immediately obvious non-ideality of the real modulator waveforms shown in Figure 12 is the sensed switch current. In most circumstances, the sensed rising edge of the switch current is not as *clean* as the waveform shown in Figure 11. There will always be some finite rise time to the switch current, as well as some overshoot at the *corner* formed when the switch is fully on, and the valley current; this overshoot can even intersect the control signal in some cases. In practice, these effects are dealt with using a *blanking time* – a short time after the clock edge, where the modulator is prevented from terminating the switch pulse, even if its inputs dictate it should do so. This is meant to ensure that these non-ideal effects have time to settle prior to the real decision point.

A main source of decreased noise margin in peak current mode control is the dependence on the output inductor value. Figure 13 shows how the noise margin of the peak current mode converter is directly dependent on the slope of the switch current, which of course is dependent of the output inductor value. Hence, a peak current mode converter design using a large inductor would be more susceptible to jitter because this would decrease the slope of the switch current, compared to a converter with a small inductor value.

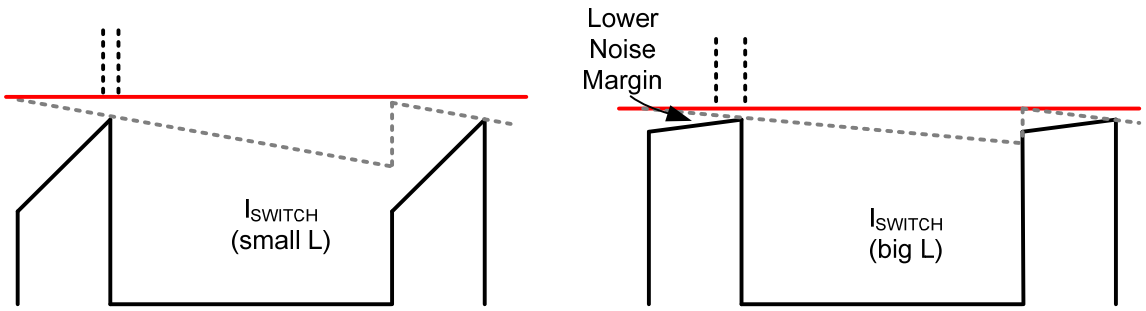

Figure 13 - Peak Current Mode Control Inductor Slope Dependence

Constant On-Time DCAP™ Control

A popular control scheme developed by Texas Instruments for designs requiring fast transient response with relatively few output capacitors is Texas Instruments' DCAP™ control. Most commonly, DCAP is paired with an adaptive constant on-time control scheme. By itself, DCAP control refers to a control technique using the effective series resistance (ESR) of the output capacitance as a current-sense element. This enables DCAP control to have superior transient response. The very popular TPS53355 converter employs DCAP mode control.

Most commonly DCAP is used with adaptive constant-on-time control. In this scheme, the desired switching frequency is known, and the ideal on-time of the power switch is determined by an on-time generation circuit. For buck converters, the ideal on-time for each cycle is given as $t_{ON} = V_{OUT} / (V_{IN} \times f_{SW})$. The output voltage is divided to match a voltage reference. Whenever the divided output voltage intersects the reference voltage, the switch is turned on for exactly the determined on-time. Because the on-time is well-controlled by internal circuitry, on-time jitter is a negligible effect for this type of control. However, the off-time (time between t_{ON} pulses) is generated by comparing the output voltage ripple to the voltage reference. In most applications, it is desirable to minimize the amplitude of the output voltage ripple, so it can be seen that the decision point happens on a much smaller scale than that of voltage or current mode control.

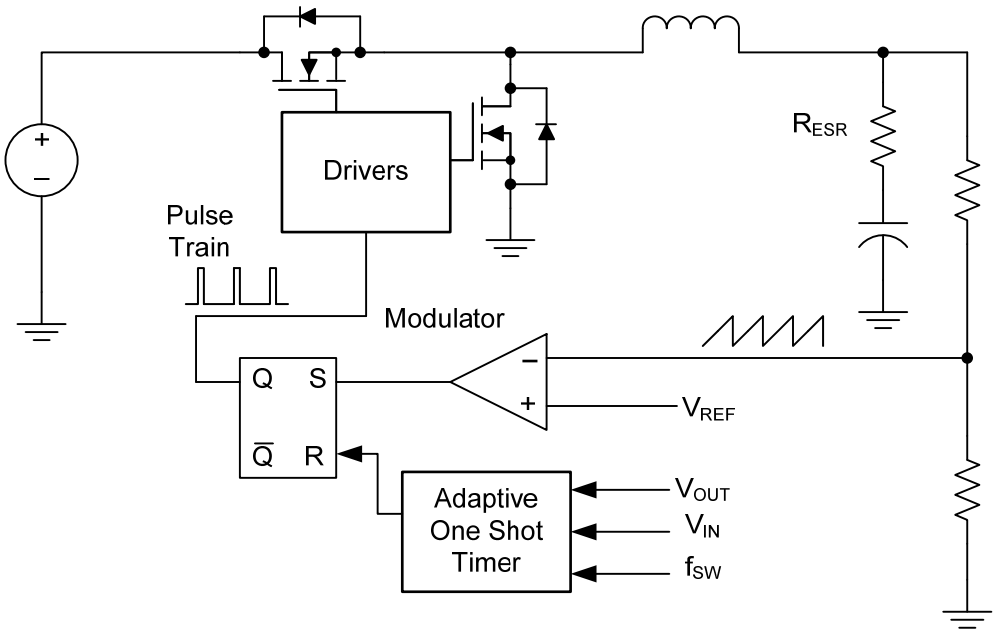

Figure 14 - DCAP Constant On-Time Control

In effect, the modulator noise margin of adaptive constant on-time DCAP control is determined by the output voltage ripple. Figure 15 and Figure 16 show the modulator waveforms for this type of control. It can be seen that as the output ripple amplitude is minimized, the noise margin at the modulator shrinks accordingly. This is the reason DCAP converters generally specify a minimum output ripple requirement, and are seen as more susceptible to jitter.

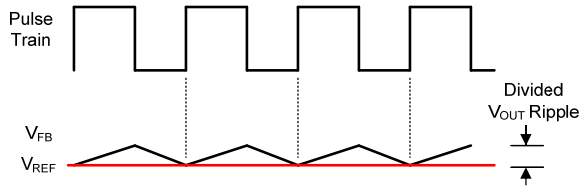

Figure 15 - DCAP Ideal Modulator Waveforms

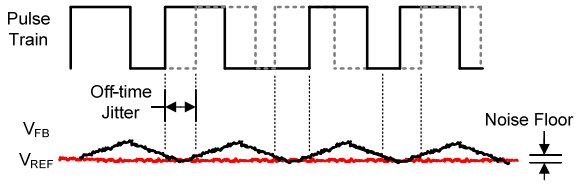

Figure 16 - DCAP Real Modulator Waveforms

Most typically, a minimum of 15 mV ripple at the modulator is necessary to keep a *reasonable* amount of jitter, though this limit is subjective. This ripple is generated using high ESR output capacitance. Compare this to a ramp amplitude between 1 V and 2 V for the voltage mode controller, and it is easy to see why jitter is more noticeable in DCAP designs. Figure 17 shows the effect of minimizing the output voltage ripple on the jitter performance of a constant on-time DCAP control converter.

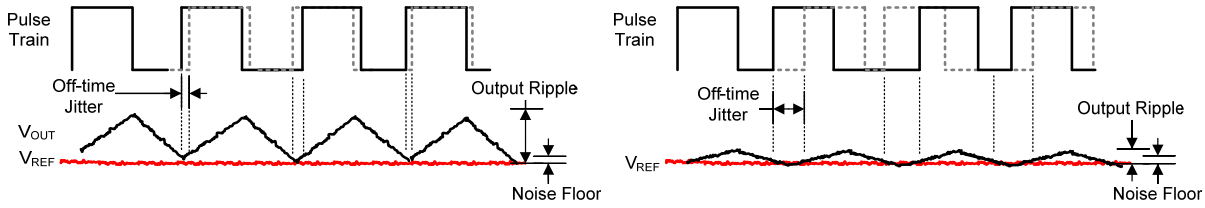

Figure 17 - DCAP Output Ripple Dependence

DCAP Control with Emulated Ramp Generation (including DCAP2 and DCAP3)

Many low output voltage designs cannot tolerate large output ripple due to increasingly tight AC output specifications. Designs may require the fast transient response offered by DCAP control, but not be able to tolerate the high output ripple required for stability. One method that can be used to support DCAP control with near zero output ripple is *emulated ramp generation*. This can be implemented externally, via an R-C network across the output inductor which is then coupled into the feedback node. This process is described in SLVS453.

Many newer TI converters such as TPS544C20 and TPS53915, which use DCAP2 and DCAP3 control, have this ripple injection network integrated into the controller which allows them to support low-ESR ceramic output capacitor banks without the need any external components.

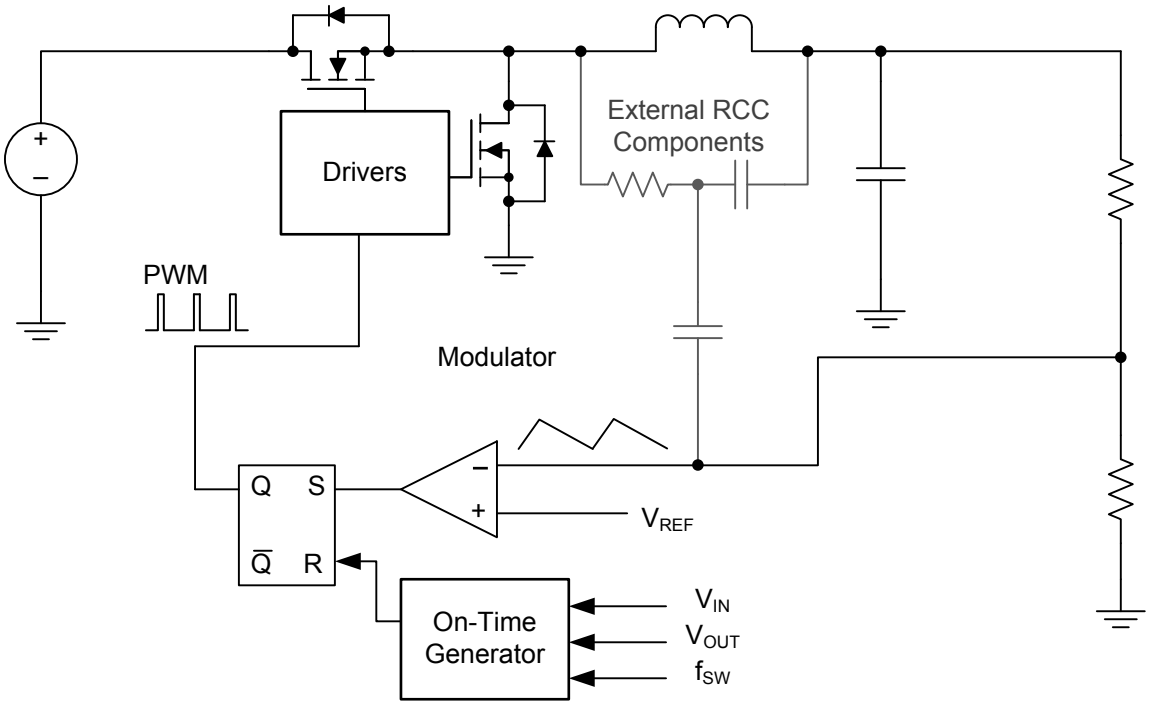

Figure 18 - DCAP Control with External RC Ramp

Figure 18 shows the block diagram of a traditional DCAP control design with external ripple injection components. These components allow the ripple at the output capacitor to be extremely small without decreasing the noise margin at the modulator inputs by *synthesizing* or *emulating* a voltage ripple in phase with switching that does not actually exist across the output capacitors.

The major innovation of DCAP2 control is the ability to include these ripple generation components internally to the controller circuit for low-ESR output capacitor support without the need for external components. Because the selection of these component values affects transient response and control loop phase margin, DCAP3 devices also include options to optimize/change these component values for optimum performance at the system level.

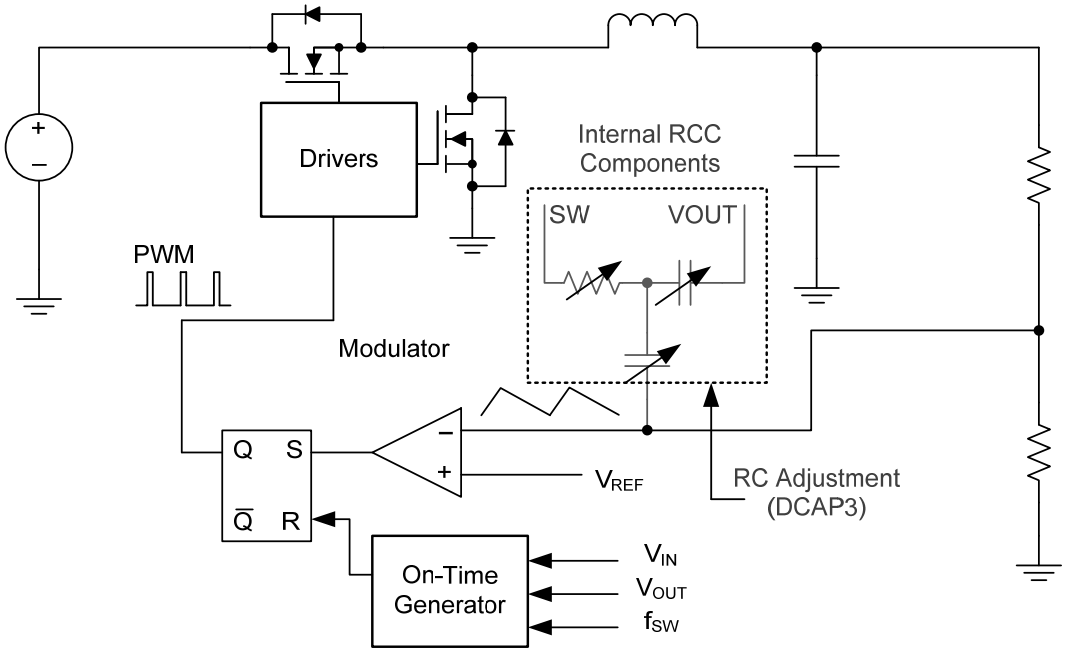

Figure 19 – DCAP2 and DCAP3 Control with Internal RC Ramp

It is important to note that even though these schemes include emulated ripple injection, the amplitude of the emulated ramp remains relatively small for purposes of fast transient response. This means that although stable switching can be achieved without an output ripple requirement, the switching jitter in DCAP designs remains generally larger compared to linear schemes like voltage and current mode control.

Non-Architectural Causes of Jitter

Jitter can also be caused or exacerbated by power supply implementation issues such as control loop stability and PCB layout. For this reason, it is very important to follow manufacturer recommendations for power controllers, and adhere to good power supply design principles.

Common non-architectural causes of jitter include:

- Sub-harmonic oscillation due to marginal stability – If the control loop is not properly stabilized, the control signals (and output voltage) may begin to oscillate, which can appear either as random jitter, or bi-modal jitter (long-pulse-short-pulse operation).
- High gain compensation design – Care should be taken to design error amplifier compensation such that it does not amplify high frequency noise excessively. Compensator designs with high mid-band gain can be susceptible to jitter.
- PCB layout – Switching power supplies have several nets which carry switching currents and voltages. Power supply designers must be careful to design circuit boards such that magnetic and capacitive coupling between these signals and sensitive control signals is minimized.

Effect of Jitter on Output Voltage Ripple

Conventional power supply design wisdom holds that increased amounts of switching jitter would certainly cause the amplitude of the output voltage ripple it produces to increase – but this statement is actually not true for all types of jitter. In fact, even though constant-on-time type schemes such as DCAP, and DCAP2/DCAP3 have increased jitter, this jitter does not translate to substantially larger output ripple.

This effect can be demonstrated via closed loop time-domain simulation. The next section shows a comparison of a voltage mode converter and a DCAP converter, with high frequency noise is injected at the modulator inputs to cause switching jitter.

Simulating Jitter

A major challenge that arises when one attempts to simulate jitter in a time domain simulation is that common SPICE programs do not have arbitrary noise source generators built into them. This is because noise analysis is typically done in the frequency domain.

For the purposes of this demonstration, in which the objective is to evaluate time domain jitter, this issue has been circumvented by using MATLAB to generate a series of *Additive White Gaussian Noise* (AWGN) points, which were then exported into a piecewise linear (PWL) source at high resolution and combined with a gain stage to allow easy noise amplitude control. The end result is a circuit block which can be easily inserted in series with the modulator inputs of each converter model to show their response to high frequency noise. This simplified model of noise is enough to create switching jitter and demonstrate its effect on the output ripple. Note that in reality noise is present in varying degrees at every point in the circuit, not only at the critical nodes chosen for demonstration in this example.

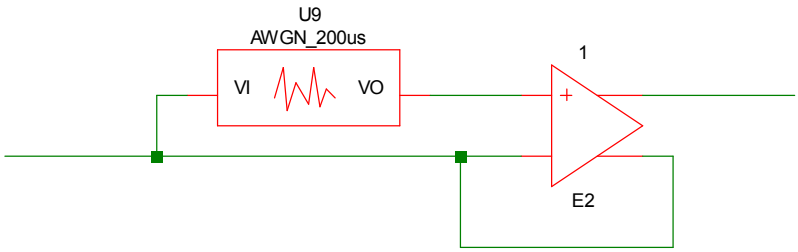

Figure 20 - AWGN Noise Source

For these simulation experiments, the AWGN source is inserted directly at the modulator input. That is, in series with Vc (or COMP) for the voltage mode converter, and with feedback (FB or VSNS) for the DCAP converter. Varying the gain of E2 in Figure 20 changes the amplitude of the noise injected.

Jitter Results: Voltage Mode Converter vs. DCAP Converter

Table 1 and Table 2 summarize the simulated output ripple peak-to-peak voltage, simulating with a voltage mode control converter and a constant on-time DCAP converter with identical power stages, under identical conditions. The example used is a 12-V to 1-V buck converter at 500 kHz. The schematic used for each converter, and time domain waveforms produced are shown in the Appendix A of this document. Because the simulated noise is random, each value is reported as a window ± 3σ (± three standard deviations from the mean).

Table 1. Constant On-Time DCAP Mode Converter

±3σ Noise Injected (mV)	±3σ OFF-Time Jitter (ns)	Peak-to-Peak Output Ripple (mV)
0.00	2.57	24.62
0.53	54.33	25.09
1.07	107.84	25.52
1.60	162.12	25.90
2.12	220.38	26.45
2.63	290.45	27.26
3.14	345.36	27.69

Table 2. Voltage Mode Converter

±3σ Noise Injected (mV)	±3σ ON-Time Jitter (ns)	Peak-to-Peak Output Ripple (mV)
0.00	3.01	24.59
29.25	53.99	33.18
58.71	103.27	42.57
93.41	158.33	54.03
133.21	226.87	68.93
178.57	287.43	80.93
218.88	344.76	96.65

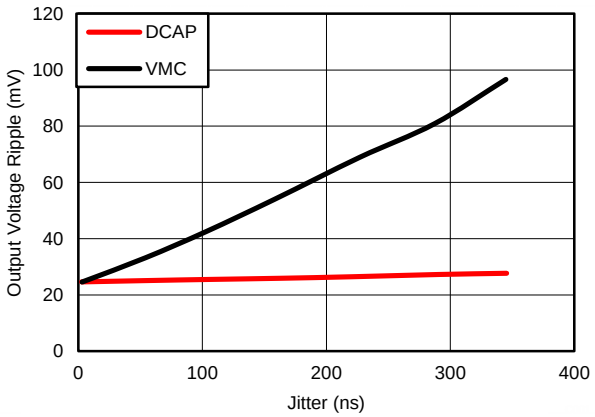

Figure 21 - Simulation Result: Output Ripple vs. Jitter

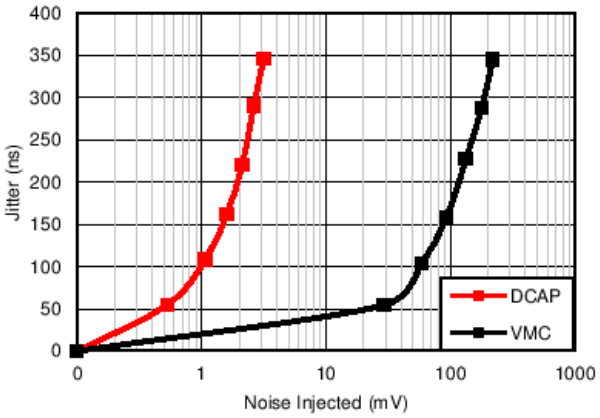

Figure 22 - Simulation Result: Jitter vs. Injected Noise

Discussion and Explanation of Results

These results raise two main questions:

Why does the same amplitude noise cause higher amounts of jitter for the constant on-time DCAP converter compared to the fixed frequency voltage mode converter?

Figure 22 shows that the amplitude of noise required to produce the same amount of jitter was much lower for the constant on-time DCAP mode converter compared to the voltage mode converter. This is a result of the fact that the constant on-time DCAP mode converter has lower modulator noise margin. Referring to Figure 23, the voltage mode converter has its control signal compared to a ramp with approximately 1.4 V, a typical value for a 12-V input bus voltage mode buck converter. For the constant on-time DCAP mode converter, effectively, the output voltage is the ramp signal, and V_{REF} is the control signal – so its ramp signal is nominally only 25 mV. It can be seen that for a given amount of noise, the voltage mode converter has a much higher signal-to-noise ratio (SNR).

For example, consider the effect of a 1-mV amplitude noise signal on both converters. This noise signal is only a 0.07% fraction of the ramp signal for the voltage mode converter, while it represents a 4% fraction of the ramp signal in the constant-on-time DCAP mode converter.

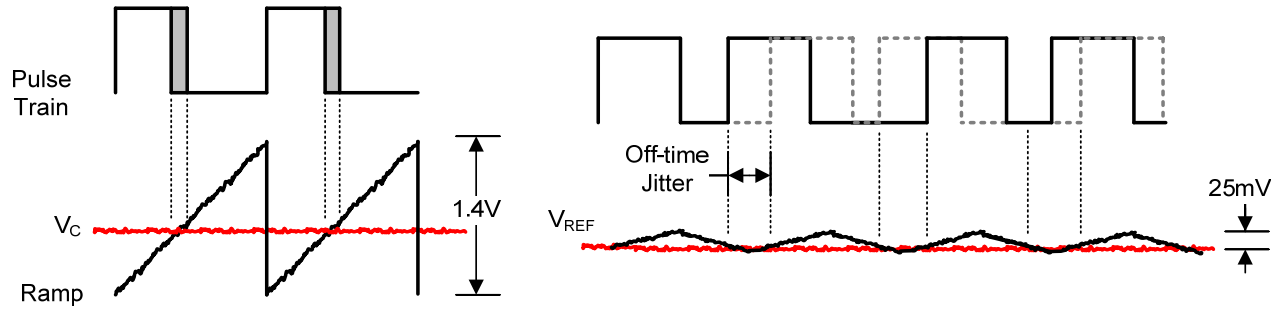

Figure 23 - Noise Margin Comparison: Voltage Mode vs. DCAP

Why does the output ripple increase more for the voltage mode converter than it does for the constant on-time DCAP converter, when they have the same amount of jitter?

Figure 21 shows that for the same amount of jitter, the constant-on-time DCAP mode converter had much less output ripple compared to the voltage mode converter. Figure 24 and Figure 25 This is caused by a combination of two effects:

(1) the nature of fixed frequency control, and

(2) the relative speed of each control loop

Firstly, by definition, the fixed frequency voltage mode converter remains at a fixed frequency, even when a jittering pulse delivers too much energy to the output. Even though, the previous pulse has delivered more energy to the output than required, a pulse continues to occur at the beginning of the next switching period, which causes the output to overshoot further. For the constant on-time DCAP mode converter, there is no fixed frequency requirement. When two pulses occur too close to each-other due to jitter, some overshoot is observed, but the next pulse does not occur until the output voltage falls back to the reference point. Hence the constant on-time DCAP mode converter is able to correct for jitter on a cycle-by-cycle basis, where the fixed frequency converter is not.

Second, the effective control loop bandwidth of the fixed frequency voltage mode converter is lower than that of the constant on-time DCAP converter. Ideally, the fixed frequency converter would simply skip the next pulses whenever a jitter pulse caused the output to overshoot, but in order for this to occur, the control signal must slew from its nominal value to outside the ramp signal, which takes time, and requires a relatively large transient. For the constant on-time DCAP converter, the output voltage *is* the control signal, so when it overshoots, the control loop is able to respond without needing to slew compensation components.

A similar discussion would hold for the case of an undershoot caused by jittering pulses in each converter.

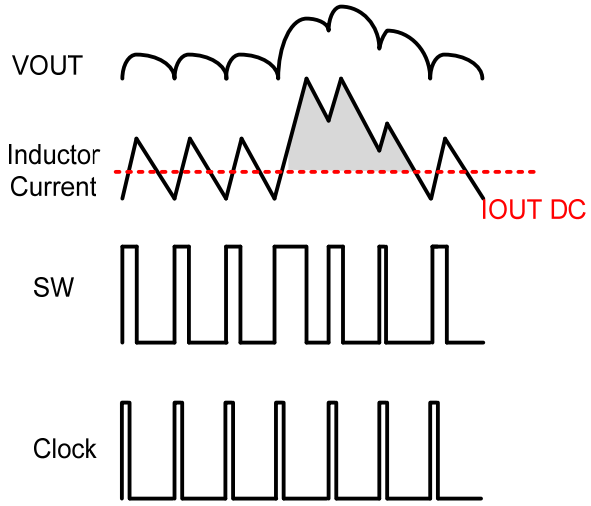

Figure 24 - Jitter Response (Voltage Mode)

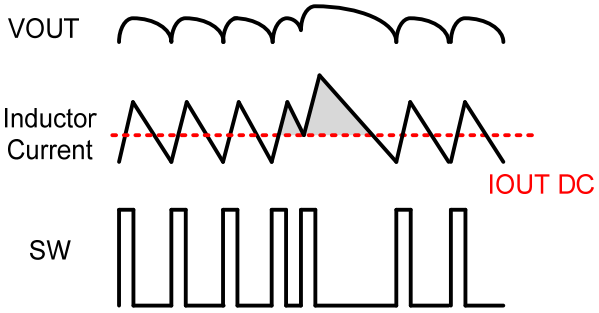

Figure 25 - Jitter Response (DCAP)

Conclusion

Some amount of jitter is unavoidable in any DC-DC power supply design. Jitter is caused by noise that is present at the modulator which controls the operation of the power switches used to convert power.

Because different control architectures such as voltage mode control, current mode control and constant on-time DCAP, use different methods to control switching, these schemes have different jitter signatures. Fixed frequency, clock-based schemes like voltage mode control and current mode control are mainly susceptible to on-time jitter only, where constant on-time schemes like Texas Instruments DCAP are susceptible to off-time jitter only.

Control schemes which have higher signal-to-noise ratio are less susceptible to jitter. For this reason, it is not uncommon to see voltage mode converters with on-time jitter with only 20 ns, where a typical constant on-time DCAP converter might have 100 ns of off-time jitter. However, jitter does not affect all converters equally. For an equivalent amount of jitter, fixed-frequency converters show more output voltage deviation than constant on-time converters.

Appendix A. Simulation Schematics

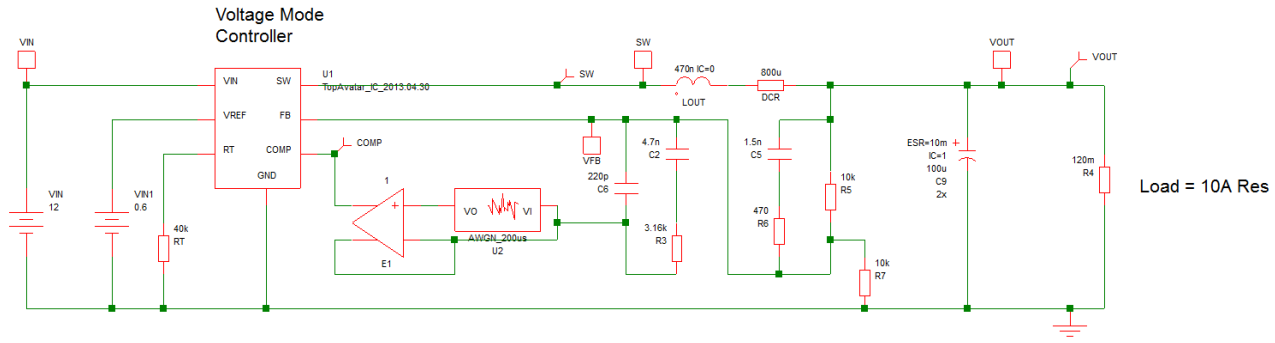

Figure 26 - Voltage Mode Converter Schematic

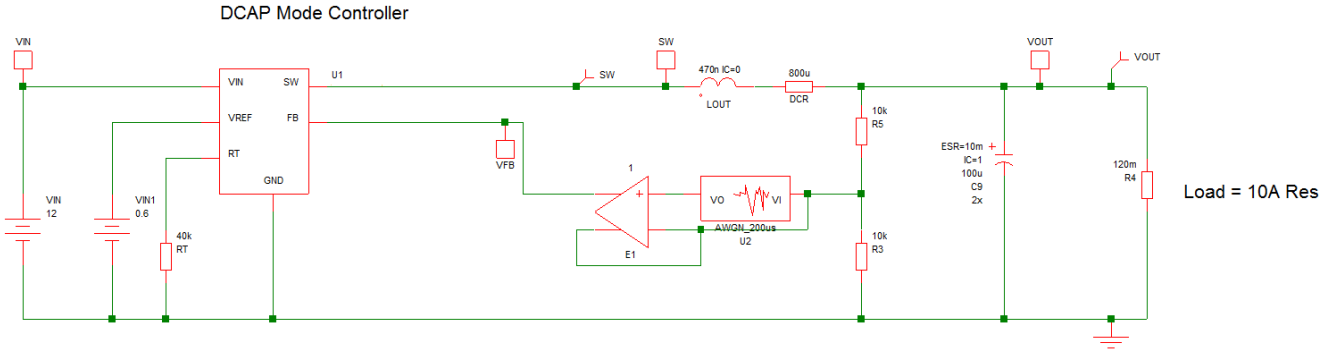

Figure 27 - DCAP Converter Schematic

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