



Rapid Transient Response With UCC28633 Primary-Side-Regulation (PSR) Flyback and UCC24650 Wake-Up Monitor

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ABSTRACT

PSR flyback controllers make use of primary-side information to indirectly sense the output voltage for regulation. This capability allows elimination of the conventional secondary-side error amplifier (typically TL431) and feedback opto-coupler – saving cost and standby power. However, because the output voltage can only be sampled during a switching cycle, there is always a trade-off with PSR between very-low switching frequency to achieve low standby power and the need to keep switching frequency high to maintain a fast transient response. This application note demonstrates how the UCC28633 PSR controller can be combined with the UCC24650 secondary-side fast wake-up monitor to achieve low standby power and fast transient response.

Topic	Page
1 Introduction	2
2 Transient Response versus Standby Power	3
3 UCC28633 External Wake Input at VSENSE Pin	4
4 Practical Demonstration Using UCC28630-EVM572	6
5 Test Results	8
6 Summary and Conclusions	12
7 References	12
8 Export Control Notice	12

1 Introduction

PSR is ideally suited to flyback converters, where secondary-side output voltage is readily available for sensing across the transformer low-voltage bias winding, scaled by the bias-to-secondary turns ratio. Such schemes require connection of the primary-referenced bias winding to a voltage-sense pin of the PWM controller, for measurement of the reflected output voltage during the flyback interval, as shown in Figure 1. Sampling of the reflected output voltage is synchronized to the flyback-interval portion of the PWM switching cycle, as shown in Figure 2.

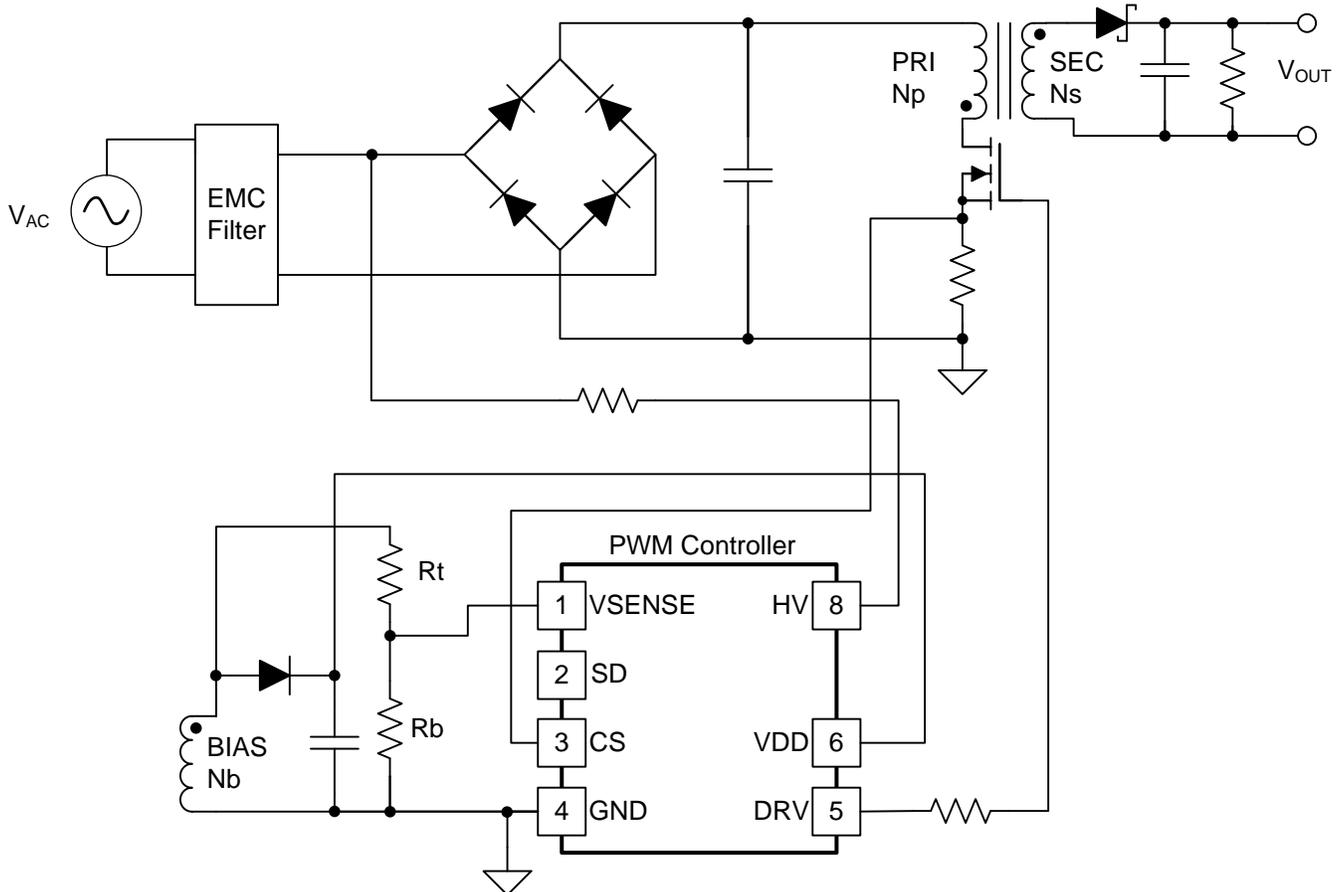


Figure 1. Typical PSR Flyback Power Stage and Controller

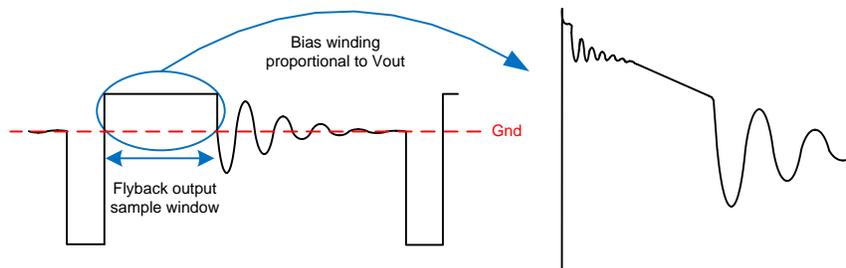


Figure 2. Indirect Output Voltage Sense through Flyback Bias Winding

2 Transient Response versus Standby Power

As shown in Figure 2, the sampling of the reflected output voltage on the bias or sense winding must be synchronized to the Flyback interval of a PWM switching cycle. In between switching cycles, the primary-side controller is effectively “blind” to any deviations in the output voltage. This differs from conventional secondary-side error-amplifier plus opto-feedback schemes, where the secondary-side error amplifier continuously monitors the output voltage.

To achieve very low standby power targets, such as ≤ 30 mW, the PWM switching frequency of PSR controllers is commonly decreased as load power decreases. As the load power approaches zero, the PWM frequency can decrease well below 1 kHz; for example, the UCC28633 PSR controller has a minimum switching frequency F_{\min} of just 200 Hz. This very-low minimum frequency allows for power supply designs that can achieve very-low standby power.

However, as noted previously, in between switching cycles, the PSR controller is “blind” to any changes in output voltage. So, if the power supply is running at or near zero-load standby level, and a large load transient is applied, the response of the primary controller will be very dependent on the relative timing between the application of the load step, and the next timed PWM cycle. If the primary controller is operating at an F_{\min} of 200 Hz for example, then the worst-case delay is up to 5 ms before the next switching cycle; during this interval, the drop in system output voltage is entirely a function of the load current and the amount of output hold-up capacitance (see Figure 4).

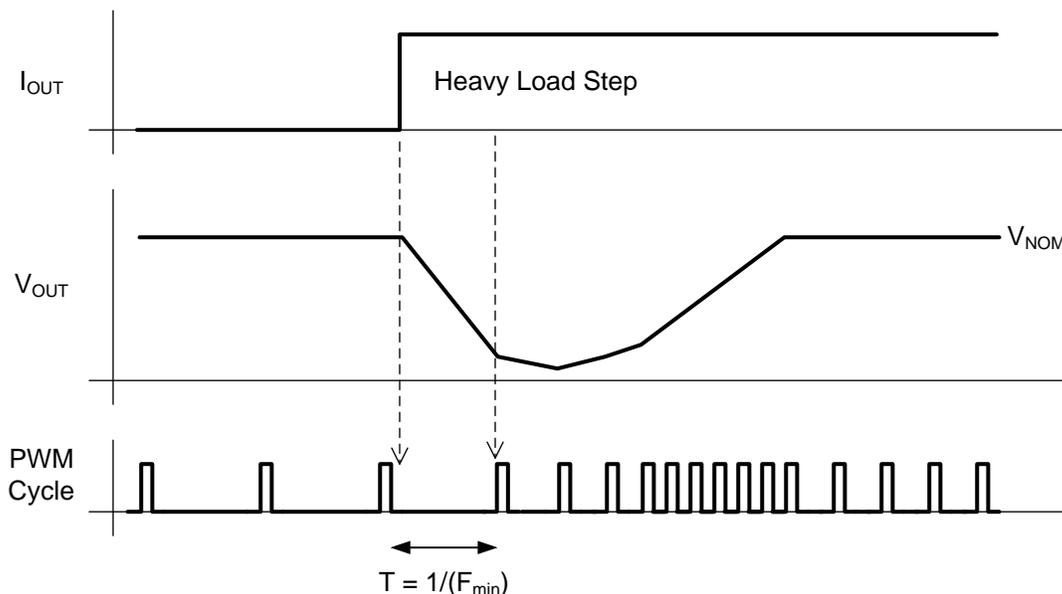


Figure 3. Output Transient Drop at F_{\min} – When Load Step Occurs just After PWM Cycle

By making use of the UCC28633 PSR controller and the UCC24650 secondary-side voltage monitor and wake-up IC, the user can design a PSR flyback power supply that can achieve good transient response and low standby power.

As shown in Figure 4, the main output rectifier diode must be positioned at the return side of the secondary winding, so that the GND-referenced UCC24650 WAKE function can be deployed. In effect, the WAKE pin shorts out the rectifier diode for a short interval to draw some current from the output capacitor through the transformer secondary winding. This sets up a low-level pulse of current that then rings resonantly in the power circuit, magnetizing inductance and parasitic capacitance. This causes a similar ringing voltage waveform on all transformer windings, including the bias/sense winding, which interfaces to the VSENSE pin. If the initial pulse of current drawn by the secondary WAKE pin is sufficient, then the ringing voltage at the VSENSE pin is large enough to exceed the wake-up threshold.

The UCC28633 [data sheet Typical Application](#) section includes details of how to estimate the amplitude of the wake pulse ringing at the WAKE pin. In some cases, especially at higher-rated output power, the transformer magnetizing inductance is lower, while the total switch node capacitance tends to be higher. This reduces the transformer impedance and can also result in reduced wake pulse amplitude. In these cases, the UCC24650 WAKE pin output can be augmented with an external PNP circuit Q1, R1, and R2, as shown in Figure 5. In this case, when the WAKE pin pulls low, Q1 turns on, and draws more current through the secondary winding. TI recommends to have a current limiting resistor (R1) in series with either the collector or emitter. Effectively, R1 swamps the UCC24650 internal WAKE pin resistance, R_{WAKE} . The setup requires a pullup resistor (R2) from base to emitter to ensure that the WAKE pin is adequately pulled up or pulled down during normal switching activity to properly trigger the internal sample and hold on the VDD pin. The external PNP device Q1 must have at least the same voltage rating as the main rectifier diode.

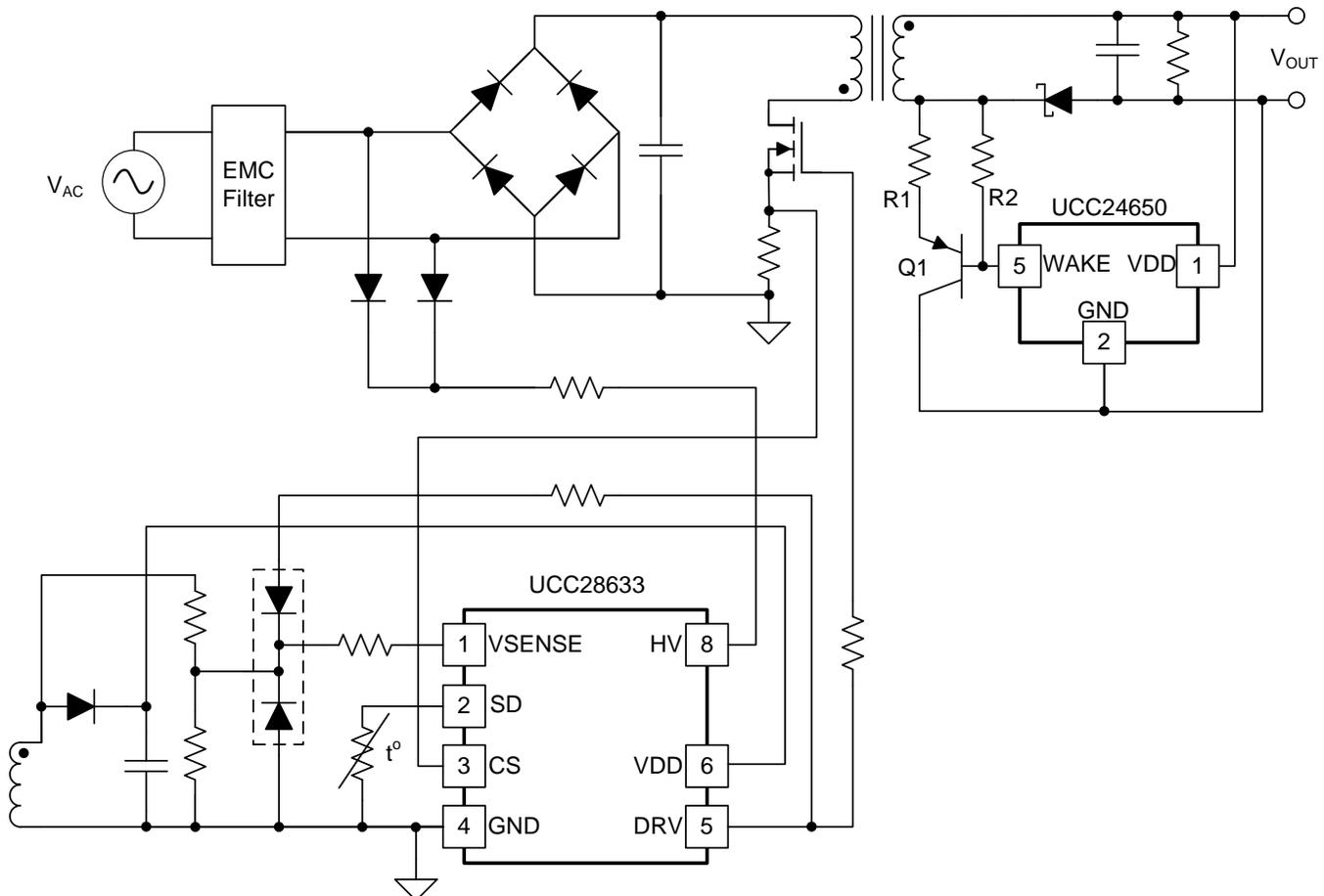


Figure 5. Addition of UCC24650 Secondary-Side Voltage Monitor and Wake-Up Circuit

4 Practical Demonstration Using UCC28630-EVM572

4.1 EVM572 Modifications

To demonstrate the UCC28633/UCC24650 capability, a standard 65-W average/130-W peak UCC28630 EVM module (UCC28630-EVM572) was modified to accommodate the secondary-side UCC24650.

The board was modified to accommodate the secondary side wake-up IC UCC24650. The following list shows the required changes, and [Figure 6](#) shows the modifications to the standard EVM572 schematic.

Required changes to EVM572 to support fast wake-up chipset:

- Replace the pre-inserted UCC28630D with UCC28633D.
- Remove output rectifier Diode D7 (and associated heatsink).
- Insert shorting wire links from the D7 anode terminals to the D7 cathode terminal.
- Cut the bottom-side trace going from transformer pins 10 and 11 to the output RET net.
- Connect diode D7 between transformer pins 10 and 11 and the output RET net. The cathode terminal should connect to the transformer pins, and the anode terminals should connect to the RET net. See [Figure 6](#) mark-up for details.
- Connect UCC24650 device to RET and +VOUT nets as shown in the schematic mark-up.
- Connect PNP transistor (choose minimum 100-V rated V_{ce} , suggest FMMTA92 or similar) plus resistors as shown in schematic mark-up, between the WAKE pin of UCC24650, output RET, and D7 cathode.

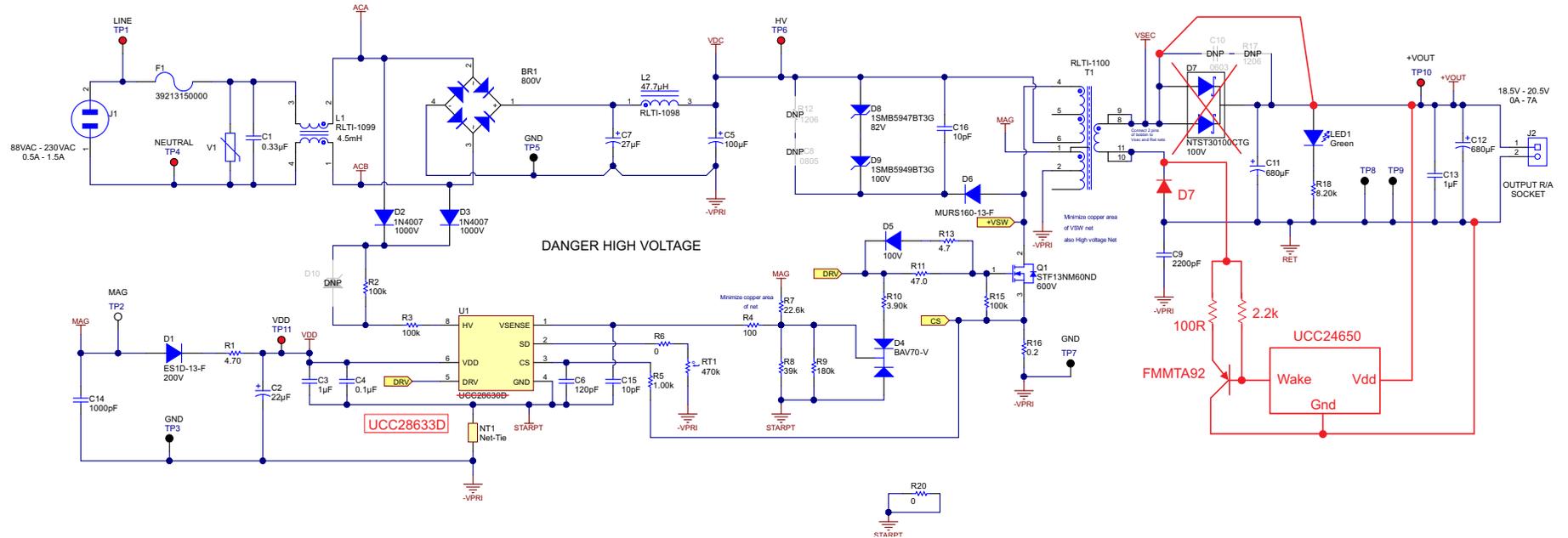


Figure 6. Modification of Standard EVM572 Schematic to Add UCC28633 PSR Controller and UCC24650 Secondary-Side Voltage Monitor and Wake-Up Circuit

5 Test Results

5.1 Standard EVM572

Before making any modifications, the standard EVM572 was tested for standby power and for no-load to full-load transients, with the results shown in Table 1 and Figure 7. The design is optimized for low standby power (to meet a specification of <70 mW), but this comes at the expense of very poor transient performance for heavy load steps that can occur from zero-load. Worst-case transient dips of 11.7 V were measured out of a 19.5-V set-point (60% dip).

Table 1. Measured Standby Power

No Load Power					
Vin (V)	F (Hz)	Pin (W) Measured	Pin (W) Max Specification	Vout (V)	Pass?
115	60	0.0524	0.070	19.65	PASS
230	50	0.0585	0.070	19.79	PASS

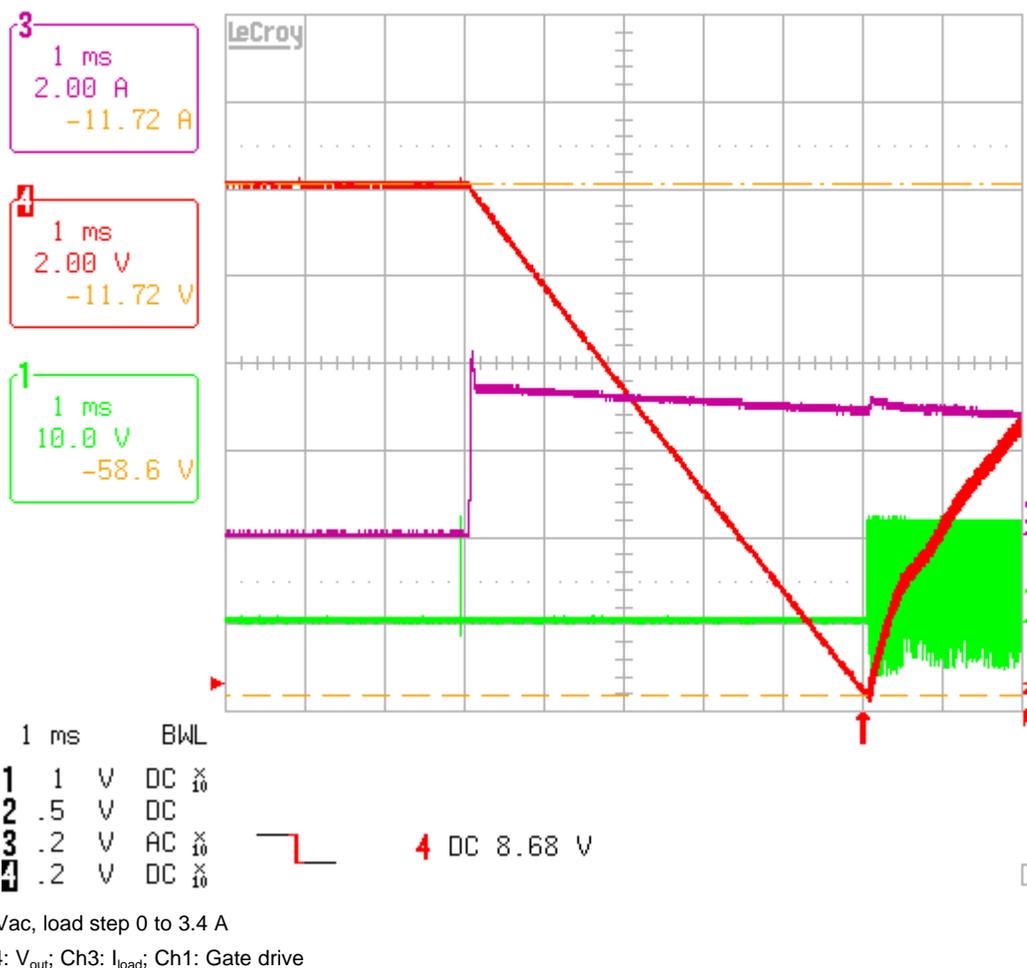


Figure 7. Zero-Load to Full-Load Transient Response on Standard EVM572

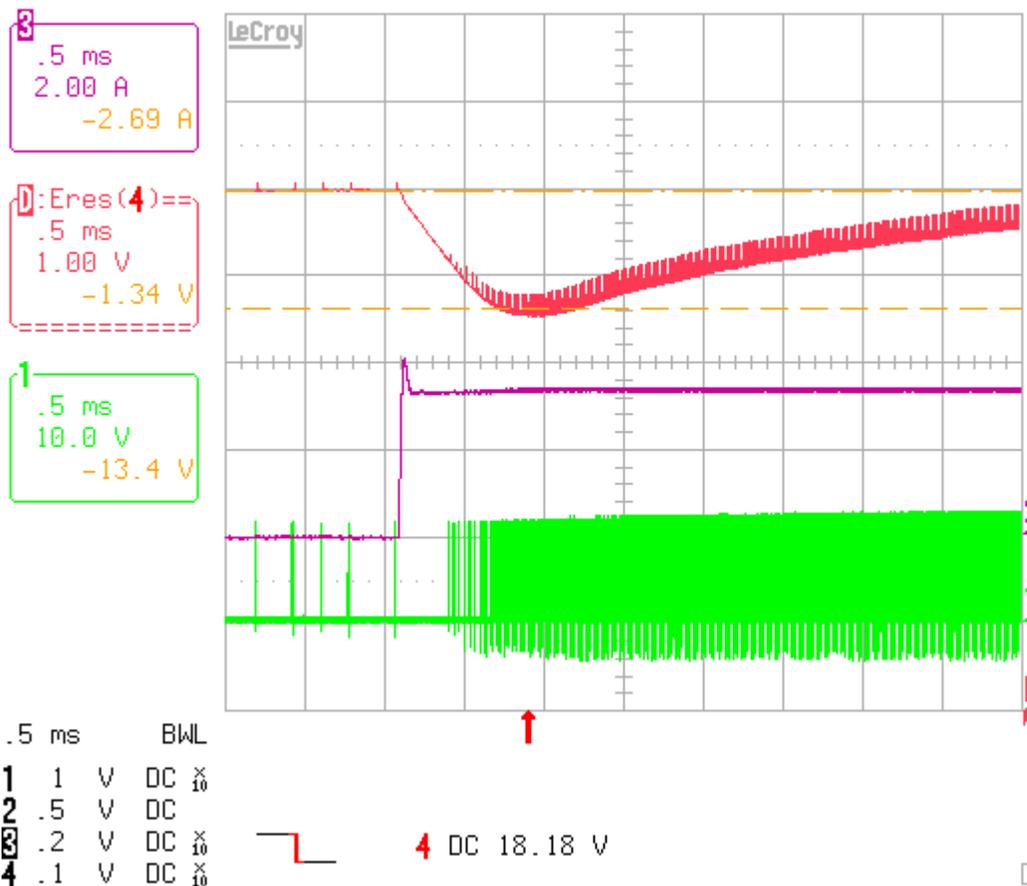
5.2 Standard EVM572 With Added Pre-Load

The standard EVM572 was modified slightly to add more pre-load to the output. This addition was achieved by adding some on-board load resistance across the output. To meet a similar timing response as the UCC24650 secondary-side wake IC, the pre-load was calculated such that the average PWM frequency in standby would be approximately 4 kHz; this gives the required time delay between PWM cycles such that a drop in V_{out} for a full-load step would be approximately 3% in between switching cycles—the same as the UCC24650 drop in V_{out} required to trigger a wake-up pulse. For the EVM572 power stage, the pre-load resistance required is approximately 1 k Ω .

The modified EVM was then tested for standby power and no-load to full-load transients, with the results shown in Table 2 and Figure 8. The design now achieves significantly better transient response – worst-case 1.34-V drop out of 19.5 V (or 6.9%), but this comes at the expense of significantly higher standby power.

Table 2. Measured Standby Power

No Load Power					
Vin (V)	F (Hz)	Pin (W) Measured	Pin (W) Max Specification	Vout (V)	Pass?
115	60	0.452	0.070	19.65	FAIL
230	50	0.441	0.070	19.79	FAIL



90 Vac, load step 0 to 3.4 A
 ChD: V_{out} ; Ch3: I_{load} ; Ch1: Gate drive

Figure 8. Zero-Load to Full-Load Transient Response on Modified EVM572 with 1-k Ω Pre-Load

5.3 Modified EVM572 With UCC24650

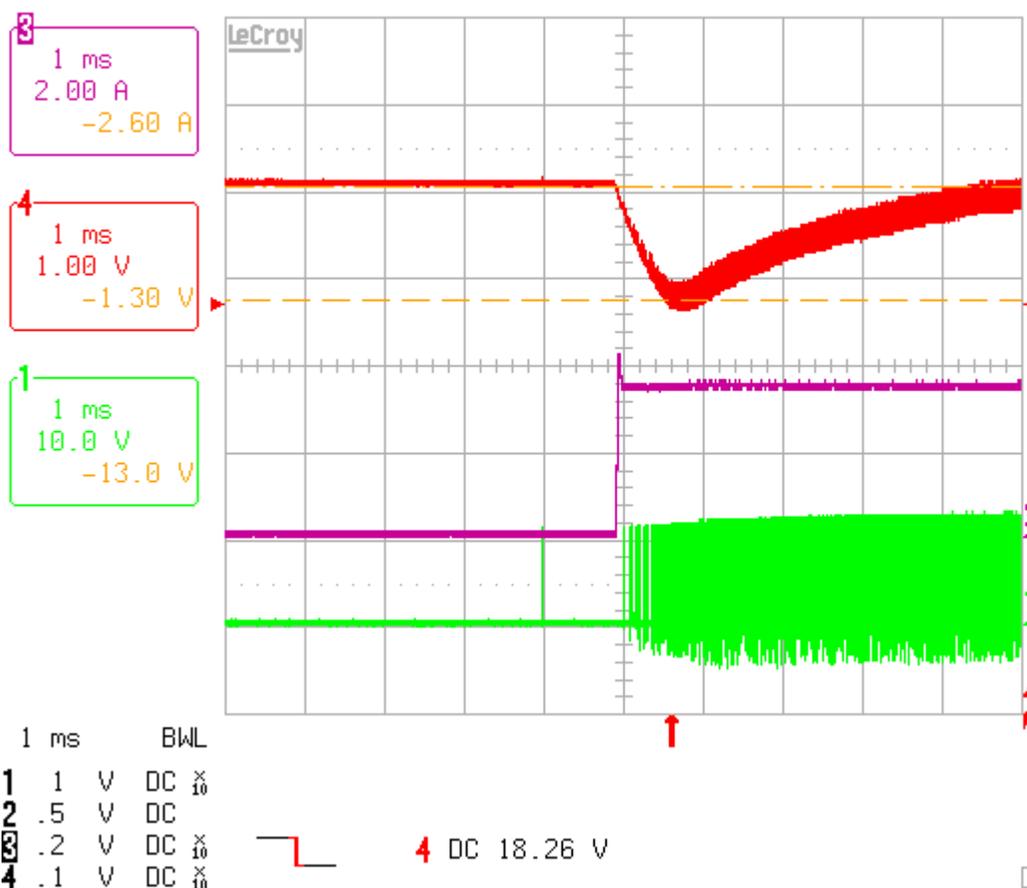
Finally, the EVM572 was modified to remove the previous extra resistive pre-load, and further modified to include the secondary-side monitor/wake-up IC UCC24650, as detailed in [Section 4.1](#) and [Figure 9](#). The system no-load standby power and transient response were measured.

Table 3. Measured Standby Power

No Load Power					
Vin (V)	F (Hz)	Pin (W) Measured	Pin (W) Max Specification	Vout (V)	Pass?
115	60	0.054	0.070	19.65	PASS
230	50	0.060	0.070	19.79	PASS

As can be seen, very low standby power performance was maintained (<2 mW increase from addition of the UCC24650, which can be compensated for by a slight increase in R18 in [Figure 6](#)).

The design achieves 60-mW standby for a power supply that is rated to 130-W peak. The standby power is <0.05% of peak power. Transient response is good, despite the low standby power; 1.3 V or 6.7% dip.

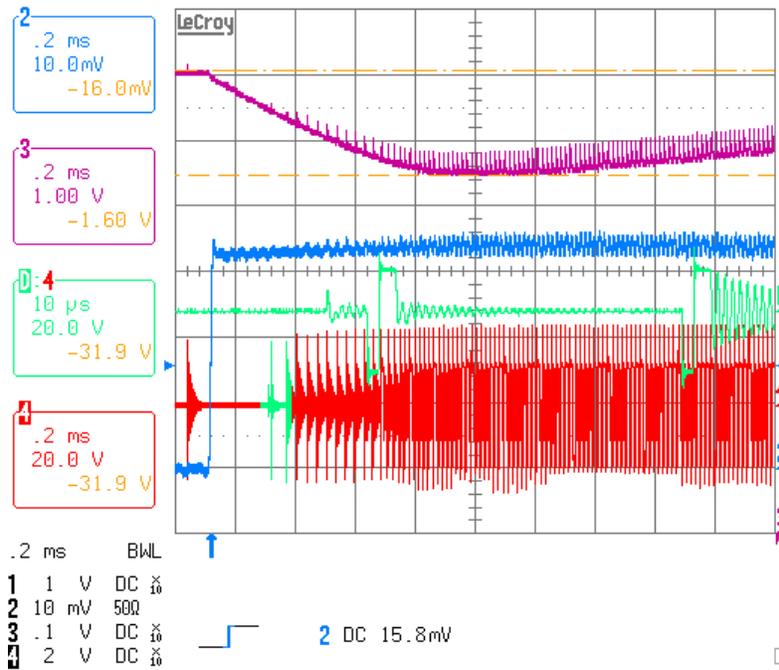


90 Vac, load step 0 to 3.4 A

Ch4: V_{out}; Ch3: I_{load}; Ch1: Gate drive

Figure 9. Zero-Load to Full-Load Transient Response on Modified EVM572 With UCC24650

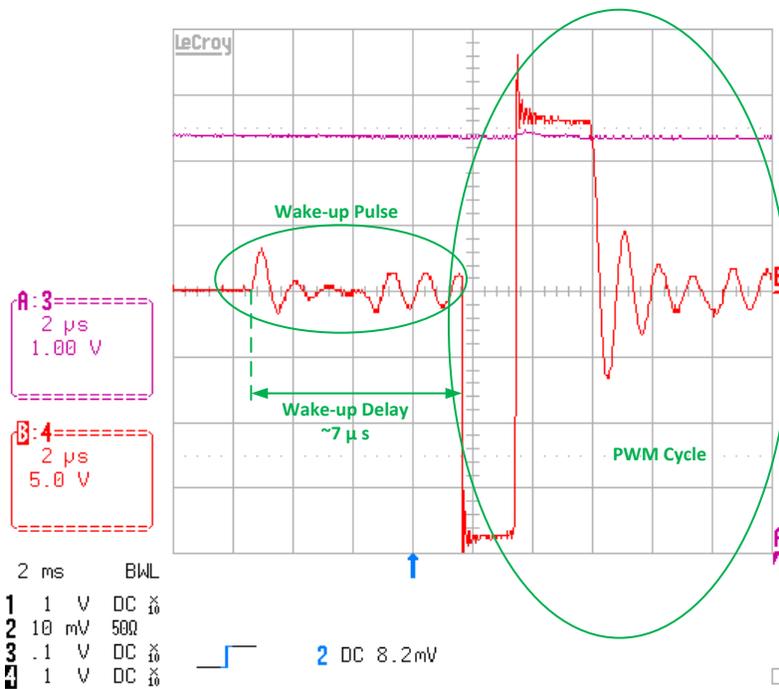
[Figure 10](#) and [Figure 11](#) show detailed plots of the waveform at the bias/sense winding and show a zoom-in of the ringing wake-up pulse waveform generated by the secondary-side wake-up IC, as measured on the primary-side bias/sense winding.



90 Vac, load step 0 to 3.4 A

Ch2: I_{out} ; Ch3: V_{out} ; Ch4: Bias wdg, ChD: Zoom C4

Figure 10. Detailed Waveforms during the Load Step Event



Zoom-in of wake pulse + response

ChA: V_{out} ; ChB: Bias wdg

Figure 11. Zoom-In of the Wake-Up Pulse and Ringing as Measured on the Primary-Referenced Bias/Sense Winding of the Transformer

6 Summary and Conclusions

Due to the trade-off between standby power and transient response for PSR, [Section 5.1](#) and [Section 5.2](#) show there is clear choice for most designs: optimize for low standby power or optimize for heavy-load transients that can occur when the power supply is operating at or near zero-load.

If the end-system has a sufficient minimum load, or if the end-system characteristics are such that heavy-load transients cannot occur when idling at or near zero-load, then the power supply can be designed for low standby power, without the poor transient response issue.

For applications where the end-system can demand very-heavy load steps from zero-load conditions, [Section 5.3](#) shows that by adding the UCC24650 secondary-side monitor and wake-up IC, a dramatic improvement in transient response can be achieved, while still achieving a very-low standby power design. The addition of the UCC24650 IC only adds a further 1 to 2 mW of extra dissipation at 19.5-V output. This extra dissipation could be subsumed into the regular PSR output pre-load to maintain the same standby performance as the system without UCC24650.

[Table 4](#) summarizes the relative performance of the EVM572 in terms of standby power and no-load to full-load transient deviation, under the three configurations tested.

Table 4. Performance Comparison

Configuration	P_{standby} (mW) Measured at 230 Vac	ΔV_{out} (V/%) for 0-A to 3.4-A Step
Standard EVM572	58.5	-11.7 V (-60%)
EVM572 + pre-load	441	-1.34 V (-6.9%)
EVM572 + UCC24650	60	-1.30 V (-6.7%)

7 References

- *UCC28630/1/2/3 High-Power Flyback Controller With Primary-Side-Regulation and Peak-Power Mode*, data sheet ([SLUSBW3](#))
- *UCC24650 Voltage Droop Monitor With Wake-Up Output*, data sheet ([SLUSBL6](#))

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