

# ***bq20z70/90 Gas Gauge Circuit Design***

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## **ABSTRACT**

Components in the bq20z70/90 chipset reference design are explained in this application report. Design analysis and suggested tradeoffs are provided, where appropriate.

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## **1 Introduction**

The bq20z90 Advanced Gas Gauge chipset has approximately 85 components in the reference design for a 2-thermistor, 4-cell application with 5 LEDs. The bq20z70, with no LEDs has approximately 78 components. For clarity, these chipsets are grouped into the following classifications: High-Current Path, Gas Gauge Circuit, AFE/Secondary-Current Protection, and Secondary-Voltage Protection.

The discussion is based on the 4-cell reference design for the bq20z90/bq29330/bq29412 chipset. The complete schematic is available on the last page of this document.

## 2 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, the sense resistor, and then returns to the PACK– terminal (see the reference design schematic at the end of this document). In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

### 2.1 Protection FETs

The N-channel charge and discharge FETs should be selected for a given application. Most portable battery applications are a good match for the FDS6690A or equivalent. The P-channel precharge FET can usually be implemented with a smaller, less expensive device depending on the desired amount of precharge current.

The Fairchild FDS6690A is an 11-A, 30-V device with  $R_{ds(on)}$  of 12.5 m $\Omega$  when the gate drive voltage is 10 V.

If a precharge FET is used, R38 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to  $(V_{charger} - V_{bat}) / R38$  and maximum power dissipation is  $(V_{charger} - V_{bat})^2 / R38$ .

The gates of all protection FETs are pulled to the source with a high-value resistor between gate and source to ensure that they are turned off if the gate drive is open.

Capacitors C27 and C28 help to protect the FETs during an ESD event. The use of two devices ensures normal operation if one of them becomes shorted. In order to have good ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C27 and C28 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

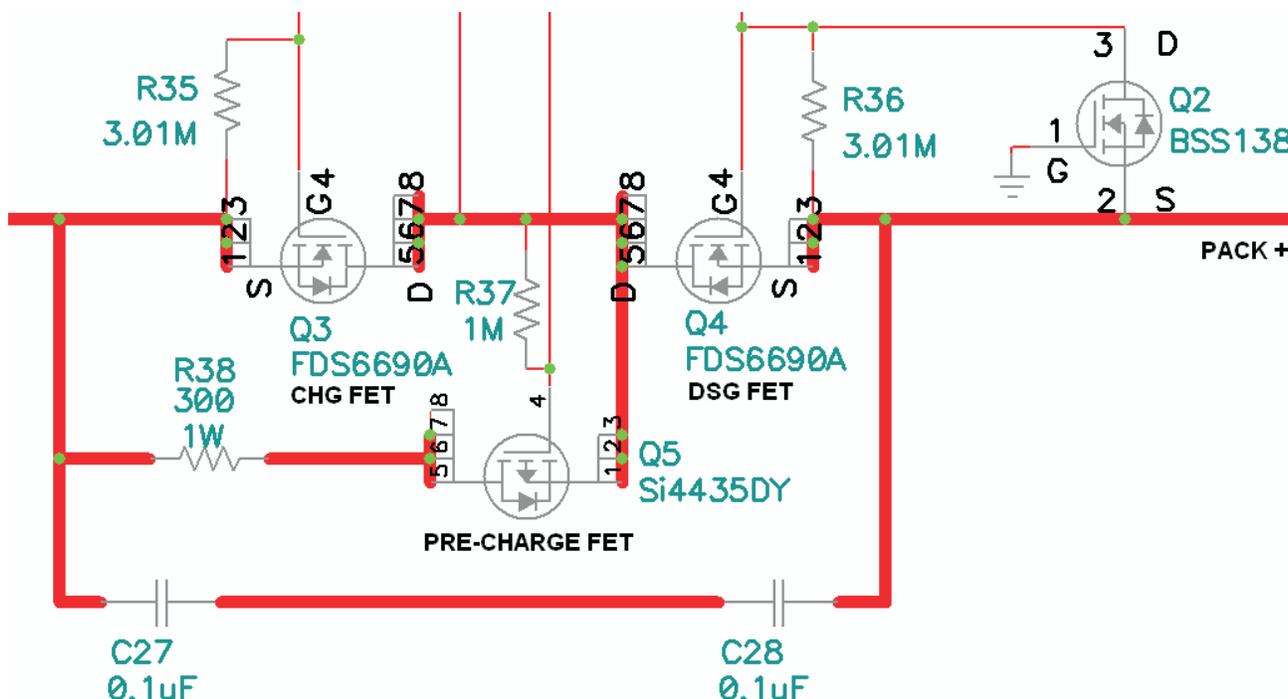


Figure 1. Protection FETs

## 2.2 Chemical Fuse

The chemical fuse (Sony Chemical, Uchihashi, etc) is ignited under command from either the bq29412 secondary voltage protection IC or from the SAFE pin of the gas gauge. Either of these events applies a positive voltage to the gate of Q1 in Figure 2, which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-channel FET. Ensure that the proper voltage, current, and  $R_{ds(on)}$  ratings are used for this device. The fuse control circuit is discussed in detail in the Gas Gauge Circuit section of this document under the heading *Safe Circuitry*.

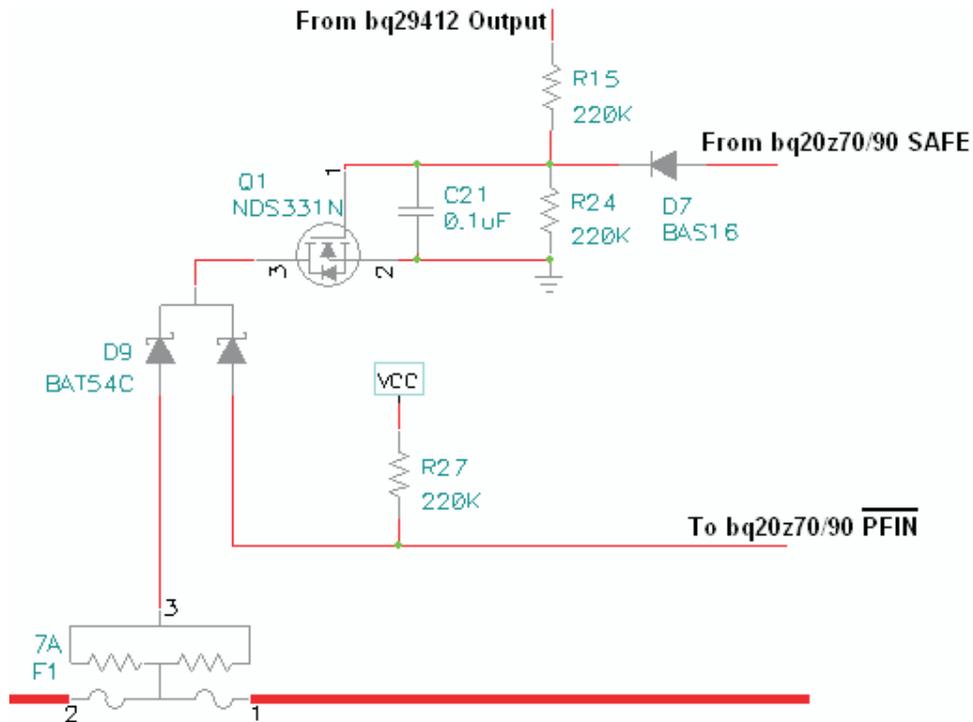


Figure 2. Chemical Fuse

## 2.3 Lithium-Ion Cell Connections

The important thing to remember about the cell connections is that high current flows through the top and bottom connections, and therefore the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. This is critical for gauging accuracy in the Impedance Track™ gauges. The location marked 4P in Figure 3 indicates the Kelvin connection of the most positive battery node. The connection marked 1N is equally important.

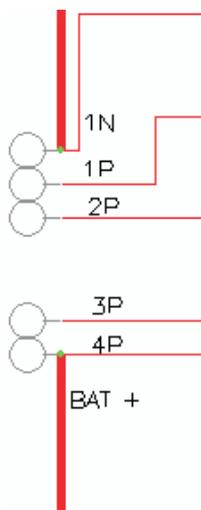


Figure 3. Lithium Ion Cell Connections

## 2.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. Not only the sense lines, but the single-point connection to the low-current ground system must be made here in a careful manner.

The sense resistor should have a temperature coefficient no greater than 75 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq29330. (See relevant tables in the data sheet). Select the smallest value possible in order to minimize the negative voltage generated on the bq29330 pin 8 (VC5) node during a short circuit. This pin has an absolute minimum of  $-0.3\text{ V}$ . For a pack with two parallel cylindrical cells,  $10\text{ m}\Omega$  is generally ideal. Parallel resistors can be used as long as good Kelvin sensing is ensured.

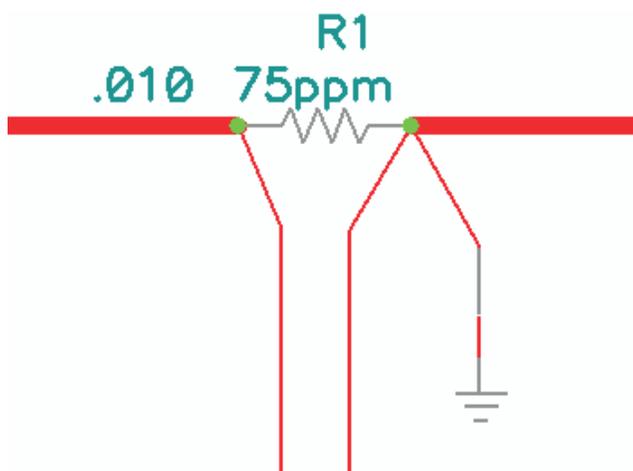


Figure 4. Sense Resistor

## 2.5 ESD Mitigation

A pair of series  $0.1\text{-}\mu\text{F}$  ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors should become shorted.

Optionally, a tranzorb such as the SMBJ2A can be placed across the terminals to further improve ESD immunity.

### 3 Gas Gauge Circuit

The Gas Gauge Circuit includes the bq20z70/bq20z90 and its peripheral components. These components are divided into the following groups: LEDs, Differential Low Pass Filter, Power Supply Decoupling/RBI/Master Reset, System Present, SMBus Communication, and SAFE circuit.

#### 3.1 LEDs

The LEDs do not need current-limiting resistors because the bq20z90 LED pins have programmable current sink to simplify the design. The display switch pulls the bq20z90 pin 14 to ground to generate an interrupt. It is pulled up to 2.5 V with a 220-k $\Omega$  resistor. However, if your packaging is arranged such that an ESD may hit the switch, you may want to insert a clamping diode, and/or RC damping here also.

The 3.3-V output of the bq29330 at the LEDOUT pin powers the LEDs. Note that a 4.7- $\mu$ F ceramic capacitor is required on the LED output for loop stability.

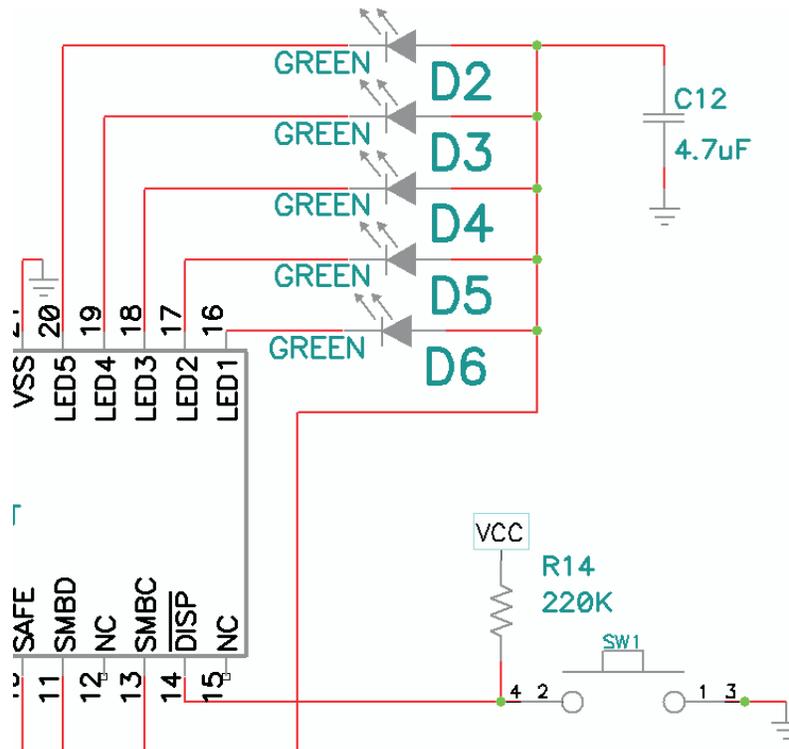


Figure 5. LEDs and Display Switch

#### 3.2 Differential Low Pass Filter

As shown in Figure 6, a differential filter should precede the current sense inputs of the gas gauge. This filter eliminates the effect of unwanted digital noise, which could cause offset in the measured current. Even the best differential amplifier has less common-mode rejection at high frequencies. Without a filter, the amplifier input stage may rectify a strong RF signal, which then may appear as a dc offset error.

Five percent tolerance of the components is adequate because capacitor C6 shunts C3/C7 and reduces AC common-mode arising from component mismatch. It is important to locate C6 as close as possible to the gas gauge pins. The other components also should be relatively close to the IC. The ground connection of C3 and C7 should be close to the IC.

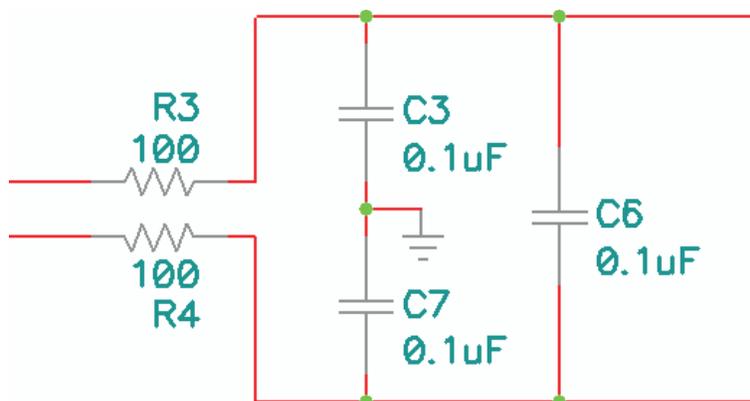


Figure 6. Differential Filter

### 3.3 Power Supply Decoupling, RBI, and Master Reset

Power supply decoupling is important for optimal operation of the bq20z70 and bq20z90 advanced gas gauges. As shown in Figure 7, a single 0.1- $\mu$ F ceramic decoupling capacitor from  $V_{CC}$  to  $V_{SS}$  must be placed adjacent to the IC pins.

The RBI pin is used to supply backup RAM voltage during brief transient power outages. The partial reset mechanism makes use of the RAM to restore the critical CPU registers following a temporary loss of power. A standard 0.1- $\mu$ F ceramic capacitor is connected from the RBI pin to ground as shown in Figure 7.

XRST (bq29330) and  $\sim$ MRST (bq20z70/90) are connected to allow the AFE to control the gas gauge reset state. The connection between these pins must be as short as possible in order to avoid any incoming noise. With the recommended orientation of the two ICs, direct interconnection does not cause a problem. If unwanted resets are found, one or more of the following solutions may be effective:

- Add a 0.1- $\mu$ F ceramic capacitor between MRST and ground.
- Provide a 1-k $\Omega$  pullup resistor to 2.5 V at MRST.
- Surround the entire circuit with a ground pattern.

Again, these steps are not normally required if the ICs are located close together. If a test pin is added at MRST, it should be provided with a 10-k $\Omega$  series resistor.

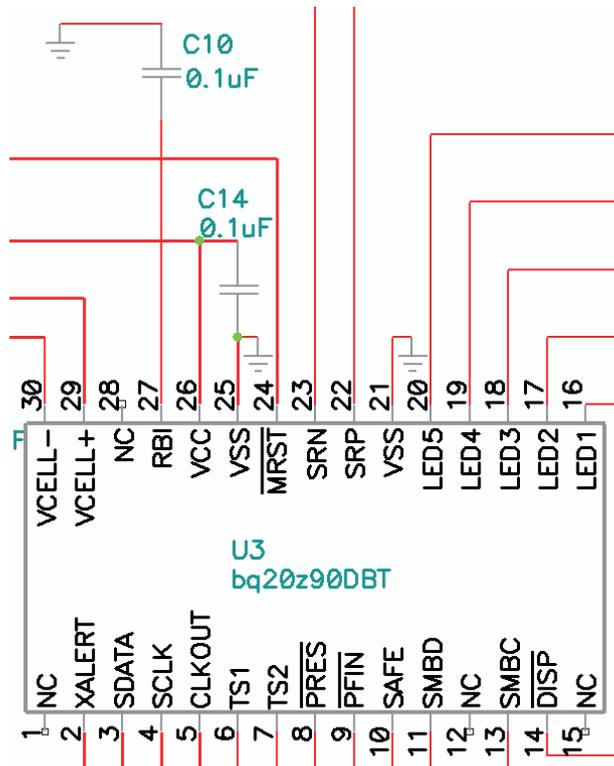
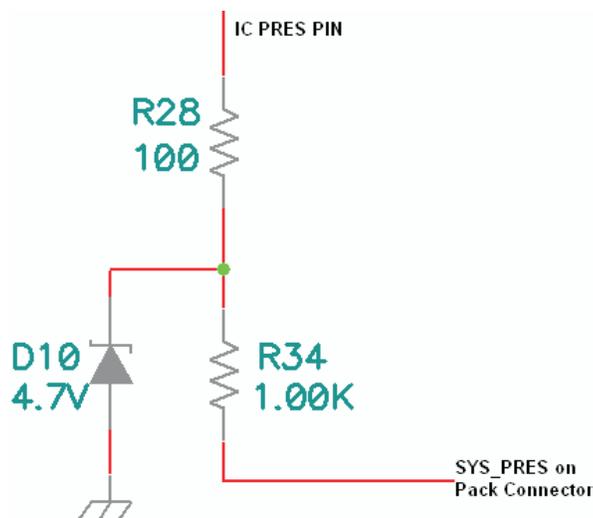


Figure 7. Power Supply Decoupling

### 3.4 System Present

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The  $\overline{\text{PRES}}$  pin of the bq20z70/bq20z90 is occasionally sampled to test for system present. To save power, an internal pullup is provided by the gas gauge during a brief 4- $\mu\text{s}$  sampling pulse once per second.

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. R34 and the 4.7-V Zener diode D10 protect against positive ESD pulses and an inadvertent short to PACK+. R28 limits the current that would flow out of the IC in parallel with the current through D10 for negative ESD pulses. Observe the voltage rating of D10 in order to maintain signal integrity and avoid electrical stress to the IC.



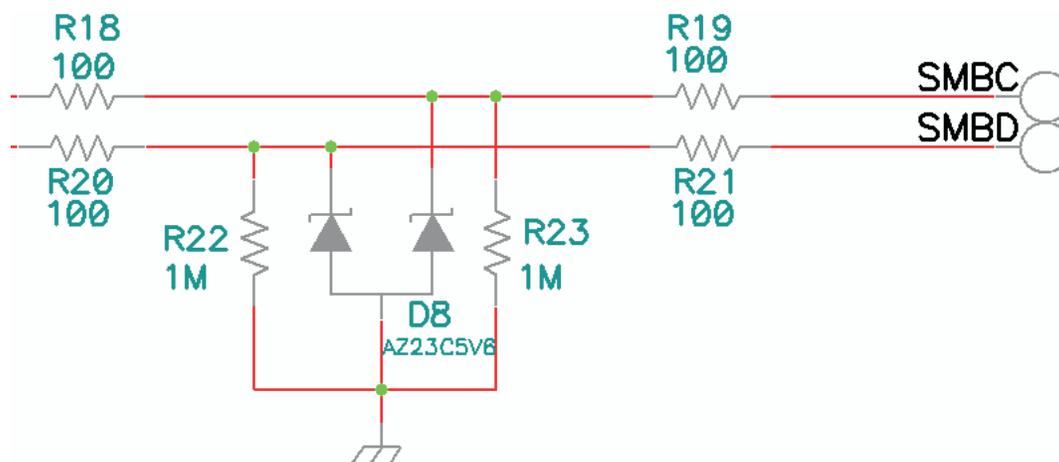
**Figure 8. System Present ESD and Short Protection**

### 3.5 SMBus Communication

As with the System Present pin, the SMBus clock and data signals interface to the outside world on the pack connector. Each signal employs an ESD protection scheme similar to that previously described for System Present (see Figure 9). It should be noted, however, that the 5.6-V Zener diode must have nominal capacitance below 100 pF in order to meet the SMBus specifications. The AZ23C5V6 is a recommended device. Also, the resistor on the pack side is only 100  $\Omega$  to maintain signal integrity. Note that the Zener diode will not survive a long-term short to a high voltage. If it is desirable to provide increased protection with a larger input resistor and/or Zener diode; carefully investigate the signal quality of the SMBus signals under worst-case communication conditions.

Resistors R22 and R23 provide pulldown for the communication lines. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto offset calibration and then goes into sleep mode to conserve power.

ESD protection operates the same as with the System Present network previously described. For the SMB clock signal, R19 and part of D8 provide clamping for positive ESD pulses, while R18 limits the current coming out of the IC (in parallel with the current through D8) for negative ESD pulses.



**Figure 9. ESD Protection for SMB Communication**

### 3.6 SAFE Circuitry

The SAFE output of the bq20z70/90 is designed to ignite the chemical fuse if one of the various safety criteria is violated. The PFIN input is used to monitor the state of the secondary-voltage protection IC. Q1 ignites the chemical fuse when its gate is high. R15, R24, and D7 form a logical OR gate, which enables the Q1 gate if either the SAFE signal or the output of the bq29412 device go to the high state. The 7-V output of the bq29412 is divided in half by R15 and R24, which provides adequate gate drive for Q1 while guarding against excessive back current into the bq29412 from D7 if the SAFE signal is high.

The use of C21 is generally good practice, especially for RFI immunity, but may be removed if desired because the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that may come from the SAFE output during the cell connection process.

The combination of D7, C21, and the gate capacitance form a peak detector with R15 and R24 as a discharge path. It is important to note that this network rectifies strong RF signals and produces a positive DC level on the gate of the FET. This potential issue can be avoided by ensuring that the trace on the anode side of D7 is kept short or is shielded by ground on both sides.

When the fuse is commanded to ignite, the right side of D9 becomes forward-biased, which notifies the gas gauge of the situation. In this manner, the output of Q1 can be recorded for future fault analysis. The left side of D9 blocks any unwanted current through the FET body diode in the case of a reverse-connected charger.

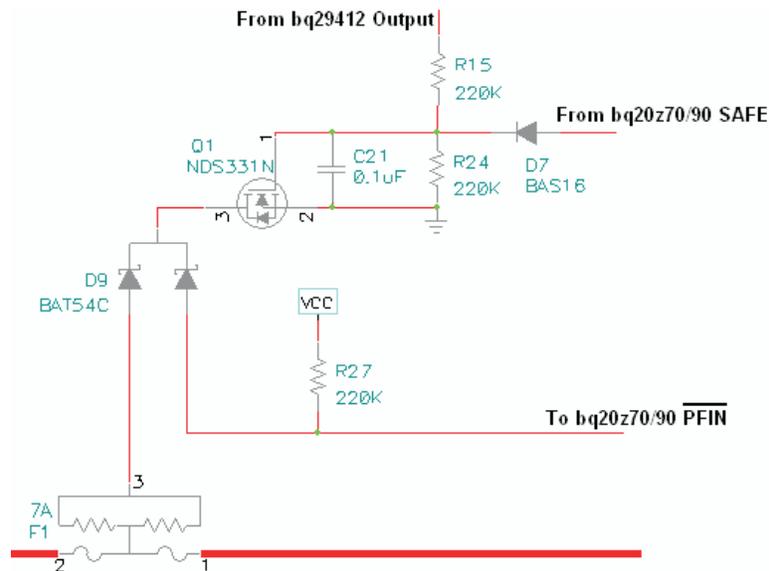
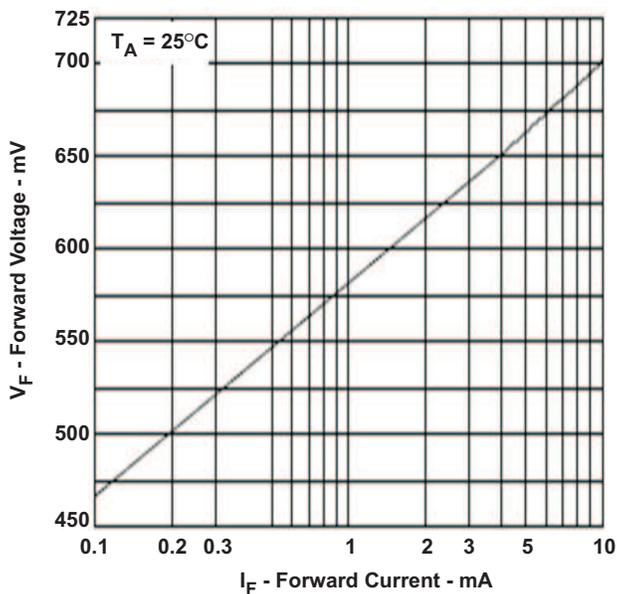


Figure 10. SAFE Circuit

For proper safety protection, it is extremely important to be certain that the fuse ignites when commanded. If alternate components are selected, an analysis such as the following must be made.

The fuse drive can be modeled as a high (~2.5 V) output from the SAFE pin, driving current through a signal diode (BAS16) into a load of approximately 110 k $\Omega$ . The minimum voltage at the SAFE pin is a function of the 2.5-V LDO in the bq29330 AFE, which has a guaranteed minimum of 2.41 V from -40°C to 110°C. With the 110-k $\Omega$  load, the output current is 23 mA. At this current, the drop from V<sub>CC</sub> to the SAFE pin is specified to be less than 1.5 mV over temperature.



**Figure 11. BAS16 Diode Forward Voltage Drop**

Figure 11 is the forward voltage drop as a function of forward current from the diode data sheet. Extrapolating down to 23 mA shows diode forward voltage to be ~400 mV at 25°C. With a 50°C change in temperature, the diode drop could be as much as  $400 \text{ mV} + 1.6 \text{ mV} \times 50^\circ\text{C} = 480 \text{ mV}$  at -25°C.

Worst-case minimum voltage at the gate of the NDS331N is given as:

$$+25^\circ\text{C} \quad V_{gs} = 2.41 \text{ V} - 0.0015 \text{ V} - 0.400 \text{ V} = 2.0085 \text{ V}$$

$$+75^\circ\text{C} \quad V_{gs} = 2.41 \text{ V} - 0.0015 \text{ V} - 0.320 \text{ V} = 2.0885 \text{ V}$$

$$-25^\circ\text{C} \quad V_{gs} = 2.41 \text{ V} - 0.0015 \text{ V} - 0.480 \text{ V} = 1.9285 \text{ V}$$

In this case, the temperature effects of the diode and the FET work together to advantage. The worst-case gate-source voltage allows approximately 3 A to flow in the drain at all expected battery temperatures (see Figure 12). Therefore, it can be concluded that there is ample margin to ensure ignition of the chemical fuse.

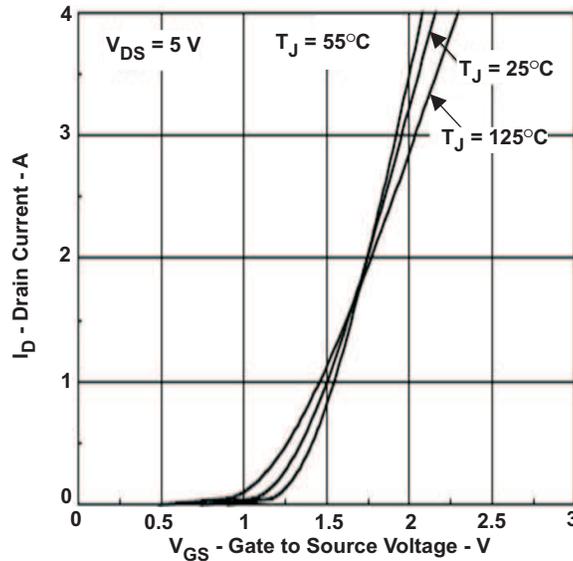


Figure 12. NDS331N FET Turnon Characteristic

## 4 AFE/Secondary-Current Protection

The bq29330 analog front end (AFE) provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, voltage translation, and the low dropout 2.5-V and 3.3-V regulators for the gas gauge and LEDs. The following discussion examines Cell and Battery Inputs, Pack, VCC, PMS Inputs and FET Control, Regulator Outputs, Temperature Output, and Cell Voltage Output.

### 4.1 Cell and Battery Inputs

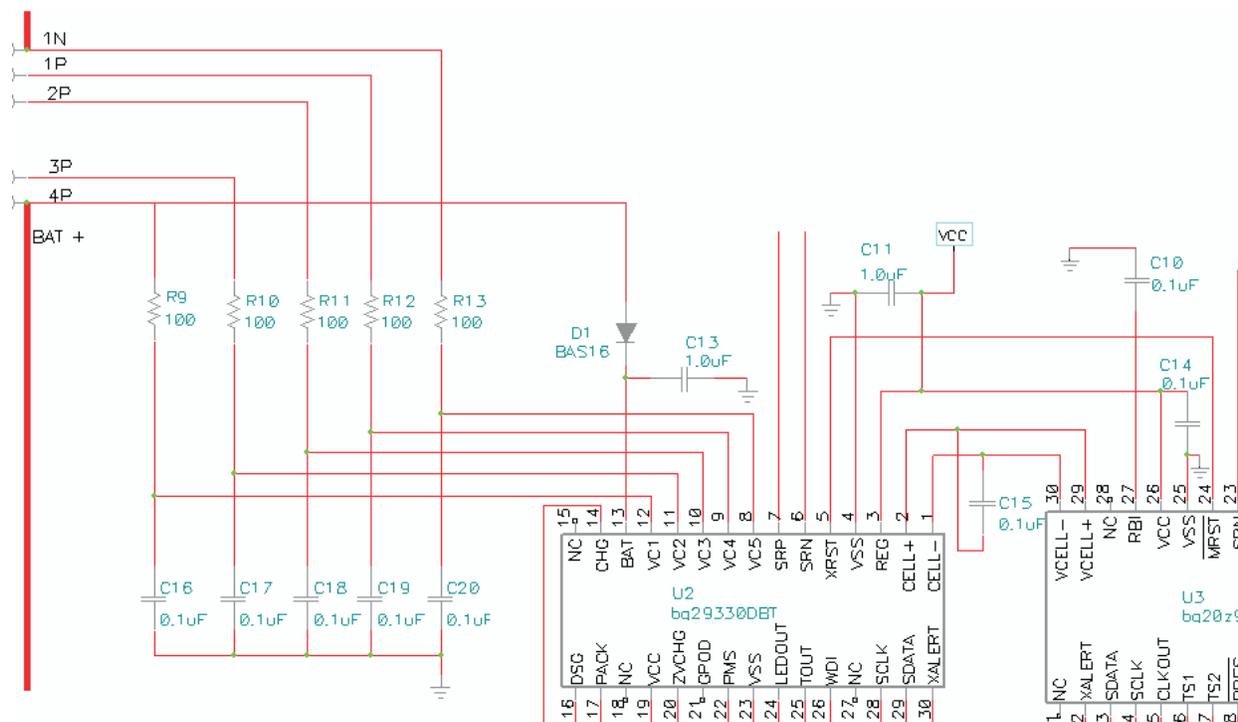
Each cell input is conditioned with a simple RC filter with a time constant of at least 10  $\mu$ s. This filter provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some tradeoff for cell balancing versus safety protection.

Internal FETs in the bq29330 provide about a 400- $\Omega$  resistance, which can be used to bypass charge current in individual cells that may be overcharged with respect to the others. (Of course, this is not done during the low duty cycle voltage measurement phase) If the filter is built with 1-k $\Omega$  resistors and 0.01- $\mu$ F capacitors, the cell-balancing feature is not effective because the total bypass resistance across a cell is 1000 + 1000 + 400 = 2400  $\Omega$ ; therefore, the bypassing current is too small. As the reference design indicates, TI recommends 100- $\Omega$  resistors and 0.1- $\mu$ F capacitors. Values between 200  $\Omega$  and 470  $\Omega$  can provide limited cell-balancing functionality.

The BAT input uses a diode (D1) and 1- $\mu$ F ceramic capacitor (C13) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

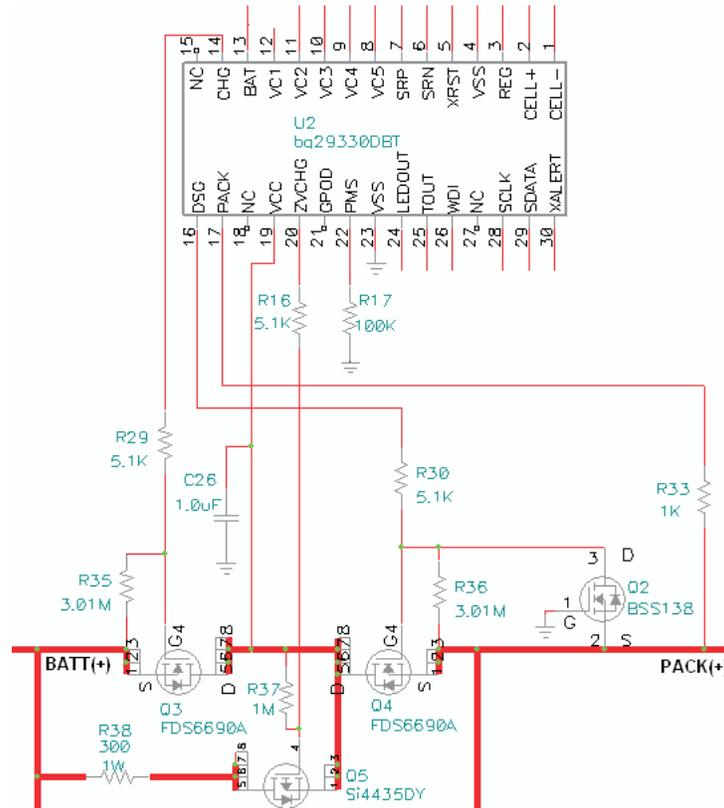
Also, as described previously in the High Current Path section, the top and bottom nodes of the cells must be sensed at the battery connections with a Kelvin connection to prevent voltage sensing errors caused by a drop in the high-current PCB copper.

Some designers prefer to specify the 100- $\Omega$  cell input resistors as the fusible type, for protection in the event of a short inside U2. This is one of those tradeoffs where the benefit may or may not be valuable and may depend on corporate policy.


**Figure 13. Cell and BAT Inputs**

#### 4.2 PACK, VCC, PMS Inputs, and FET Control

The PACK and VCC inputs provide power to the AFE from the charger. The PACK input also provides a method to measure and detect the presence of a charger. The PACK input uses a 1-k $\Omega$  resistor, whereas the VCC input uses a 1- $\mu$ F ceramic capacitor (C26) to decouple it from the PACK+ input. This guards against input transients and prevents misoperation of the gate driver during short-circuit events. Ensure that the voltage rating of C26 is adequate to withstand the full-system voltage.



**Figure 14. PACK, VCC, PMS Inputs, and FET Control**

The N-channel charge and discharge FETs are controlled with 5-k $\Omega$  series gate resistors, which provide a switching time constant of a few microseconds. The 3-M $\Omega$  resistors ensure that the FETs are off in the event of an open connection to the FET drivers. The precharge FET, if used, is a P-channel device.

Q2 is provided to protect the discharge FET (Q4) in the event of a reverse-connected charger. Without Q2, Q4 can be driven into its linear region and suffer severe damage if the PACK+ input becomes slightly negative. Q2 turns on in that case to protect Q4 by shorting its gate to source. To use the simple ground gate circuit, the FET must have a low gate turnon threshold. If it is desired to use a more standard device, such as the 2N7000, the gate should be biased up to 3.3 V with a high-value resistor.

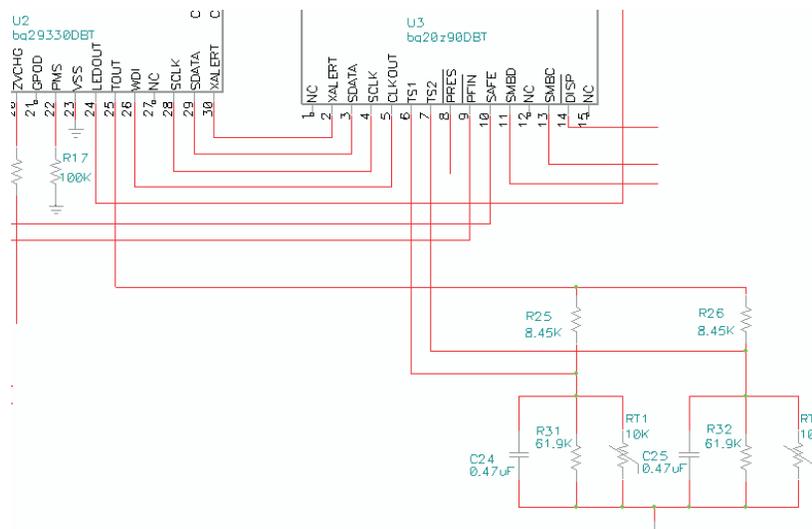
The PMS pin, depending on the desired precharge operating mode, should be tied to ground or PACK through a 100-k $\Omega$  resistor.

### 4.3 Regulator Outputs

Two low dropout regulators within the bq29330 require capacitive compensation on their outputs. The 2.5V REG output should have a 1- $\mu$ F ceramic capacitor placed close to the IC terminal. The LED output requires a ceramic capacitor, even if no LEDs are used in the application. Use a 2.2- $\mu$ F capacitor for a no-LED design and a 4.7- $\mu$ F capacitor if LEDs are used.

### 4.4 Temperature Output

TOUT (pin 25) provides thermistor drive under program control. The reference design includes two 10-k $\Omega$  thermistors, RT1 and RT2. The 1% resistors are optimized for the recommended Semitec NTC103AT, or equivalent thermistor. Because these thermistors are normally external to the board, the ceramic capacitors are provided for ESD protection and measurement smoothing.


**Figure 15. Thermistor Drive**

#### 4.5 Cell Voltage Output

The differential CELL+ and CELL– outputs require a 0.1- $\mu$ F ceramic capacitor to stabilize the output amplifier in the bq29330 and provide the required filtering for the switched capacitor input of the gas gauge A/D converter.

### 5 Secondary-Voltage Protection

The bq29412 provides secondary-overvoltage protection and commands the chemical fuse to ignite if any cell exceeds the internally referenced threshold. The peripheral components are Cell Inputs and Time Delay Capacitor.

#### 5.1 Cell Inputs

An input filter is provided for each cell input. This is comprised of resistors R2, R5, R6, and R8 along with capacitors C2, C4, C8, and C9. Note that this input network is completely independent of the filter network used as input to the bq29330. To ensure independent safety functionality, the two devices must have separate input filters.

Note that because the filter capacitors are implemented differentially, a low-voltage device can be used in each case.

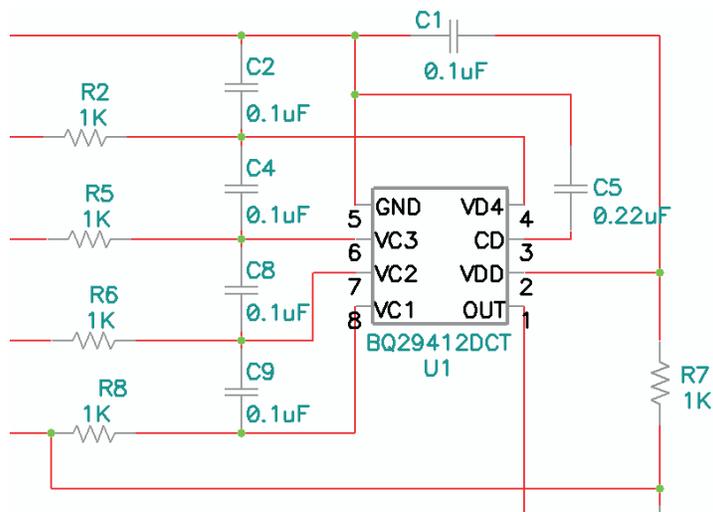
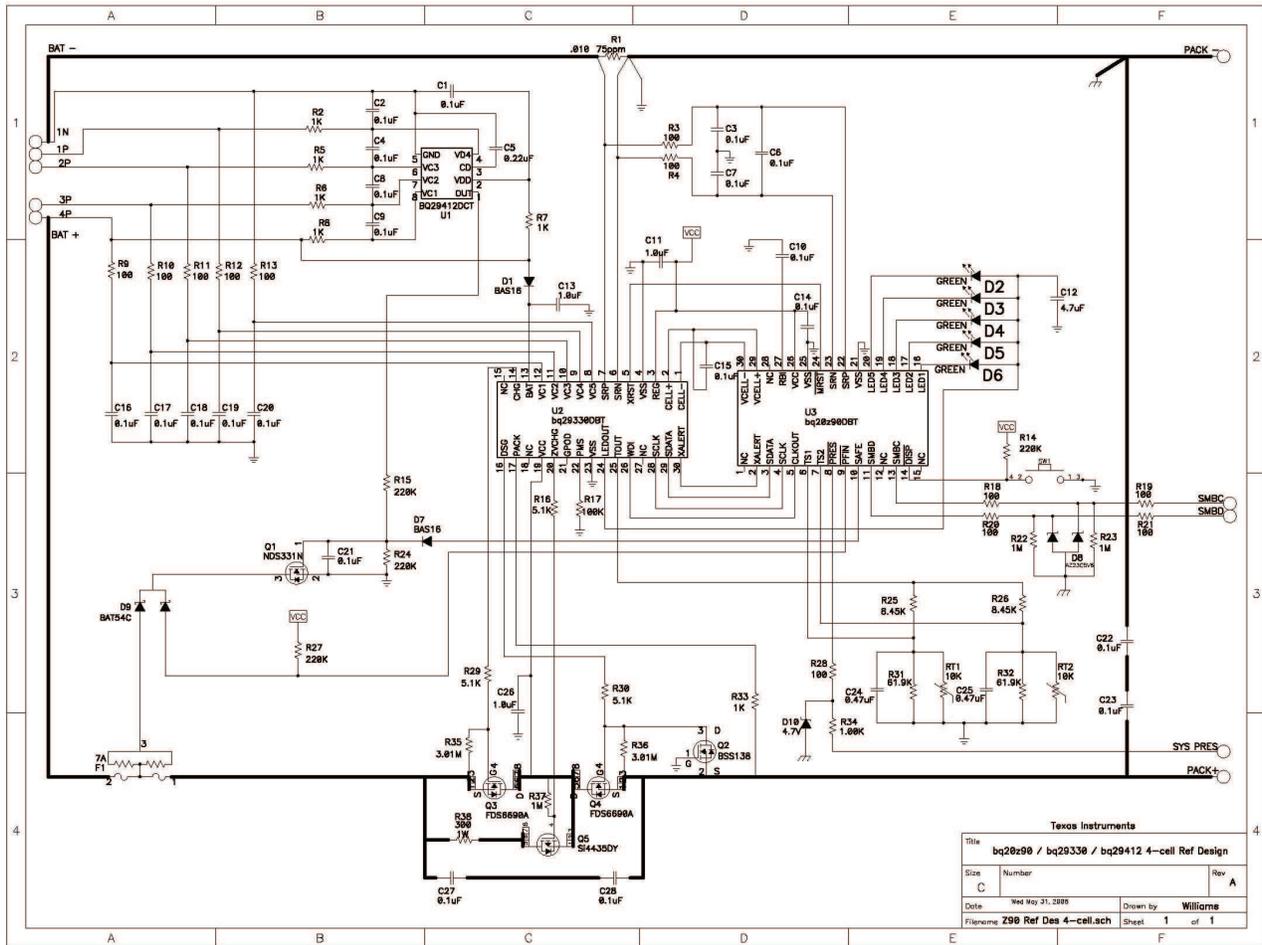


Figure 16. bq29412 Cell Inputs and Time-Delay Capacitor

## 5.2 Time-Delay Capacitor

C5 sets the time delay for activation of the output after any cell exceeds the threshold voltage. The time delay is calculated as  $t_d = 1.2 \text{ V} \times \text{DelayCap}(\mu\text{F}) / 0.18 \mu\text{A}$ .

## 6 Reference Design Schematic



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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
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Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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