UCC27221/2 Predictive Gate Drive™ Frequently Asked Questions

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ABSTRACT

The UCC27221/2 High-Efficiency Predictive Synchronous Buck Driver from Texas Instruments, employs the proprietary Predictive Gate Drive™ technology to maximize efficiencies of today's high frequency, low output voltage, synchronous buck converters. To gain a better understanding of this innovative new control technique, a list of frequently asked questions (FAQs) has been developed to address not only the UCC27221/2 but the Predictive Gate Drive™ technique as well.

Contents

1 Predictive Gate Drive General FAQs

1.1 What is Predictive Gate Drive™ (PGD) technology?

PGD technology is a digital control technique that virtually eliminates body-diode conduction while also minimizing reverse recovery losses in synchronous rectifiers. This can result in significant synchronous rectifier switching efficiency improvements. Texas Instruments is currently developing several new power products that use this innovative new technology, including the most recently released UCC27221/2, a high-efficiency predictive synchronous buck driver.

1.2 How is body-diode conduction measured?

Switching waveforms using the UCC27221/2 in a typical synchronous buck application are shown in Figure 1 and Figure 2.

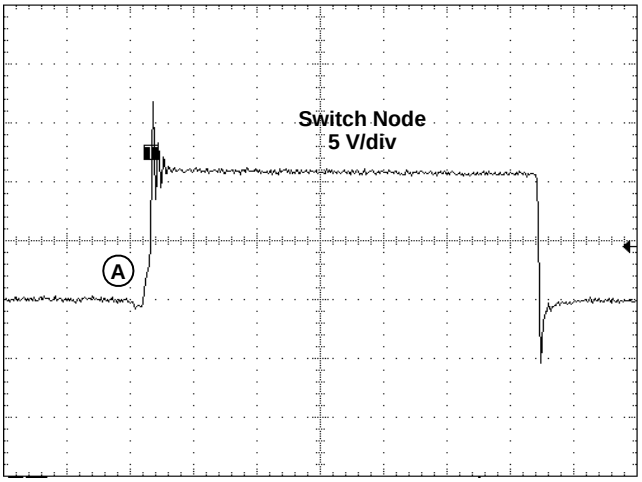

Figure 1. Switch-Node Voltage

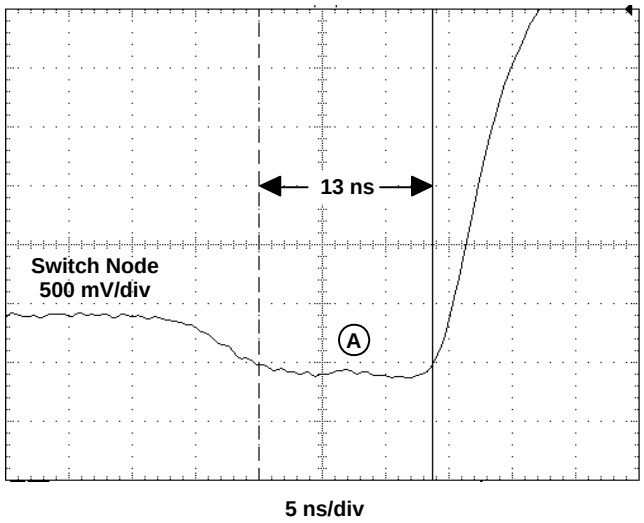

Figure 2. Switch-Node Voltage (Close-Up) of Point A

Figure 1 shows the drain-to-source voltage of the synchronous MOSFET in a 12-V synchronous buck application. This node, commonly referred to as the switch-node, is the point where the upper and lower MOSFET's connect to the output inductor. Body-diode conduction of the synchronous switch can be measured as the small dip labeled point A in Figure 1 and Figure 2. Similarly, some body-diode conduction exists at the falling edge of the switch-node as well. Point A, shown in Figures 1 and 2, is the time interval where neither the upper or lower MOSFET is conducting. During this brief time interval, the load current remains constant by flowing through the body-diode of the synchronous rectifier. A body-diode conduction time of 13 ns can be seen by zooming in on point A in a close up view as shown in Figure 2. For a synchronous buck converter not using PGD technology, this time can be as long as 100 ns. Allowing the output current to flow through the body-diode of the synchronous rectifier has a degrading effect on overall efficiency. PGD technology maximizes efficiency by reducing the delay time between turn-off of the high-side MOSFET and turn-on of the low-side MOSFET, in turn eliminating body-diode conduction time. Minimizing this delay time to near zero keeps the load current flowing where it belongs, through the conducting MOSFET switches.

1.3 How does PGD eliminate body-diode conduction in a synchronous rectifier?

For the synchronous buck stage shown in Figure 3, PGD starts by sensing the voltage at the switch-node (labeled point A), SWS, along with the gate voltage, G2S, of the synchronous rectifier.

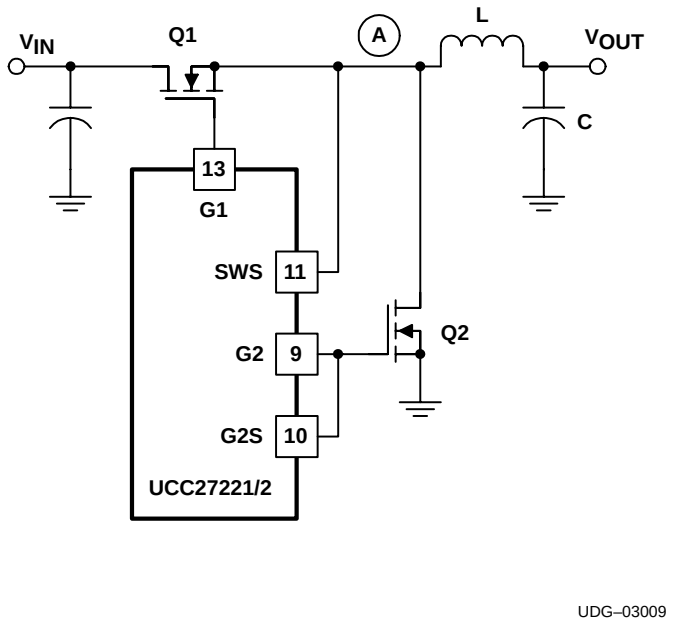

Figure 3. Sensing Q2 for Body-Diode Conduction

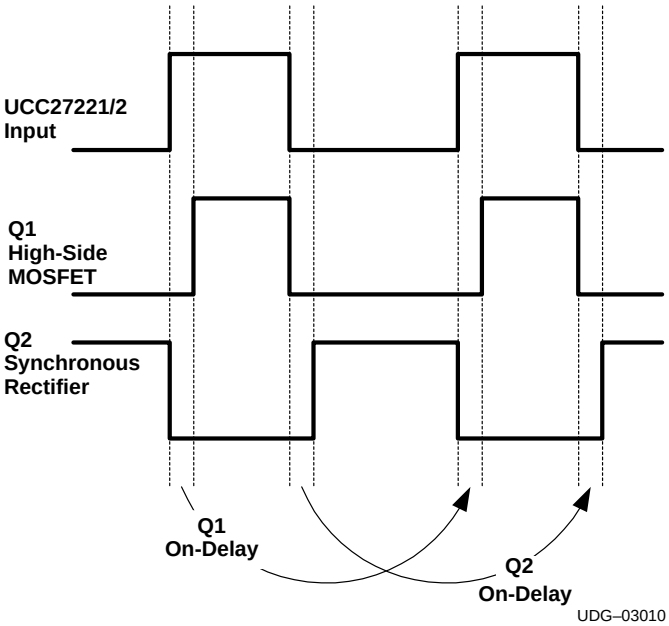

Figure 4. Predictive Timing

The smaller the delay time between Q2 turn-off and Q1 turn-on (as well as Q1 turn-off and Q2 turn-off), the less time that the body-diode of Q2 conducts. Ideally, if the delay time were zero, there theoretically would be zero body-diode conduction. Rather than sense the switch-node voltage for body-diode conduction and then adjust the delay time accordingly, PGD uses information from the current switching cycle to *predict* the minimum delay time for the next cycle. This predictive concept is illustrated in Figure 4.

PGD works on the premise that the delay time required for the next switching cycle is close to what was required for the previous cycle. When this assumption does not hold true, as in the case during a sudden line or load transient, PGD operation requires some time to adjust to the changing operating conditions. During the time PGD is recalibrating, there may be a very brief period of body-diode conduction in Q2, but this does not affect steady state efficiency or performance.

During the time that the PWM input signal transitions from high to low, a NOR gate senses the drain-to-source and gate-to-source voltage of Q2. If the NOR gate output is HIGH, as shown in Figure 5a, the delay is reduced by one bit of a 16-bit buffer delay line. For the UCC27221/2, each delay bit in the delay line represents a shift of approximately 4 ns. The delay is reduced by 4-ns intervals every switch cycle until the output of the NOR gate is low, as shown in Figure 5b. When the NOR gate output is low, the delay advances forward one delay unit on the next switching cycle. The process of continually shifting the delay forward and backward each cycle is known as *dithering*. When PGD is optimal, dithering should occur within an 8-ns (2 delay bits) window.

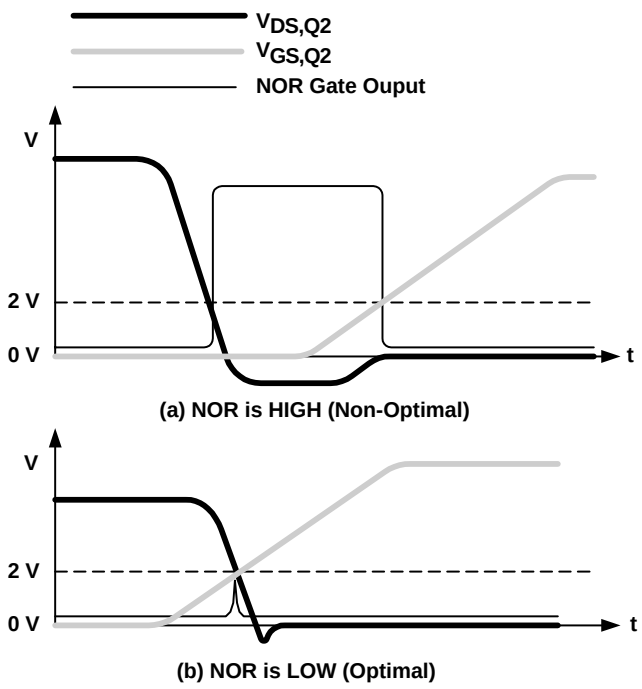

Figure 5. NOR Delays

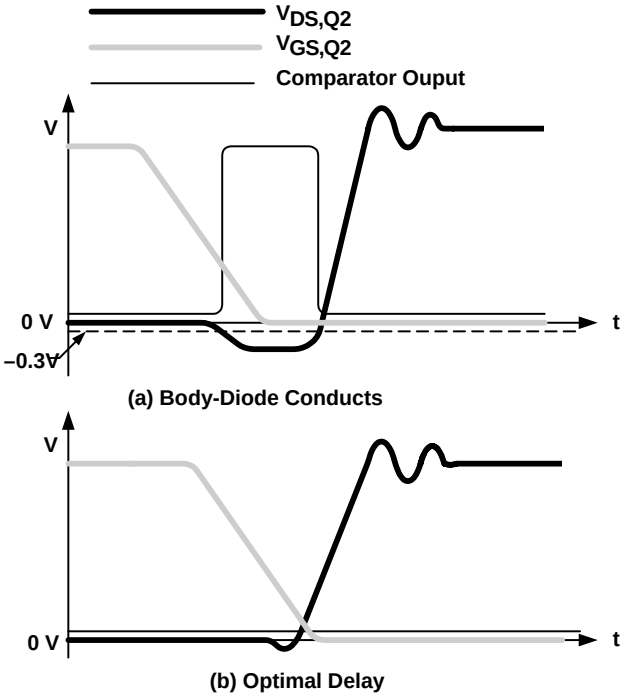

Figure 6. NOR Delays

Conversely, during the time the PWM input signal transitions from low to high, a comparator senses the drain-to-source and gate-to-source voltage of Q2. If body-diode conduction in Q2 is detected, the comparator output is HIGH, as shown in Figure 6a, and the delay time is once again reduced by one delay bit. Once enough delay segments have been introduced, such that the comparator output remains LOW, body-diode conduction in Q2 is now virtually zero, as shown in Figure 6b. From the optimal delay positioning of Figure 6b, the delay time increases by one delay bit on the next successive switch cycle.

Dithering within 8-ns of this optimal delay then becomes apparent.

1.4 Does PGD eliminate switching loss?

No. PGD technology does not eliminate switching loss. PGD minimizes body-diode conduction and reverse recovery losses that are typically a significant amount of the total device losses in a synchronous rectifier.

1.5 Does PGD offer any benefit to the high-side MOSFET?

In addition to minimizing body-diode and reverse recovery losses in the synchronous rectifier, PGD reduces power dissipation on the main (forward) MOSFET as well, although the savings is not as significant as that in the synchronous rectifier MOSFET.

The reason for this is that during reverse recovery the body diode is still forward biased, thus the reverse recovery current goes through the forward MOSFET while the drain-source voltage is still high, causing additional switching losses. During this transition, the switching losses in the high-side MOSFET are defined by the drain-to-source voltage and current as $V_{DS}=V_{IN}$ and $I_{DS}=I_{LOAD}+I_{RR}$, without PGD. When PGD is utilized, these same loss parameters are now defined by $V_{DS}=V_{IN}$ and $I_{DS}=I_{LOAD}$. The reduction in drain-to-source current explains the power savings in the high-side MOSFET. This can further be supported by comparing the thermal image shown in Figure 13, with PGD, to the image of Figure 14, without PGD.

1.6 Since PGD utilizes a dithering or *hunting* technique to hone in on the optimal delay time, what impact does this have on EMI?

While there is some dithering associated with the PGD control technique, this is expected and is not the same as gate-drive jitter commonly caused by high frequency noise. Unlike coupled noise that is random, high in di/dt content and varies with line and load, PGD dithering is controlled with zero additional di/dt content and occurs within an 8-ns window area. In addition, since PGD virtually eliminates body-diode conduction and reverse recovery, the high-frequency ringing commonly observed on the switch-node voltage of a synchronous buck is greatly reduced. Since switch-node ringing is a primary cause of radiated emissions, utilizing the UCC27221/2 with PGD technology along with good PCB layout practices can significantly reduce EMI for a synchronous buck or multi-phase converter.

1.7 How does PGD ensure that cross-conduction of the upper and lower switches does not occur?

Part of the PGD control includes an internal delay line and comparator used to detect when the body-diode of the synchronous rectifier is conducting. Once this comparator detects body-diode conduction, the PGD delay is adjusted to advance the delay time by one bit on the delay line. Because the comparator is slew-rate limited by the amount of time it takes to respond to a differential input voltage, it does not respond during the next cycle when body-diode conduction is now minimal. Since the delay time per element (typically 4 ns) of the delay line is less than the minimum detectable pulse width of the comparator, cross-conduction is completely avoided.

1.8 Which Texas Instruments products currently use Predictive Gate Drive™ Technology?

The two released products incorporating PGD technology are the TPS40000/1/2/3 series of synchronous buck DC/DC controllers and the UCC27221/2 high-efficiency predictive synchronous buck driver.

2 Competing Technologies

2.1 Do second sources offer similar synchronous buck control techniques?

PGD technology is unique and solely developed by Texas Instruments. A similar but different competing technology known as Adaptive Delay technology (also recognized as overlapping drive protection, adaptive shoot-through protection, anti-cross conduction) is also available from various manufacturers. Notable performance differences between PGD and Adaptive Delay are shown below. The upper waveforms are complementary gate drives, while the lower waveform is the switch-node voltage. Notice the minimal body-diode conduction time shown in Figure 8 using PGD versus the longer body-diode conduction interval associated with the adaptive delay control waveforms shown in Figure 7. Secondly, notice the reduced amount of ringing shown at the switch-node voltage in Figure 8.

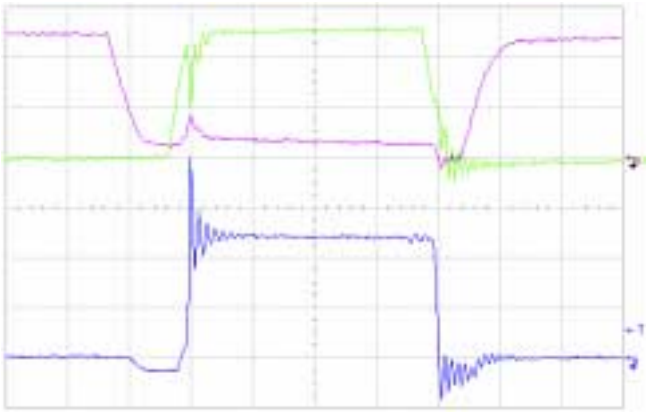

Figure 7. Adaptive Delay Control

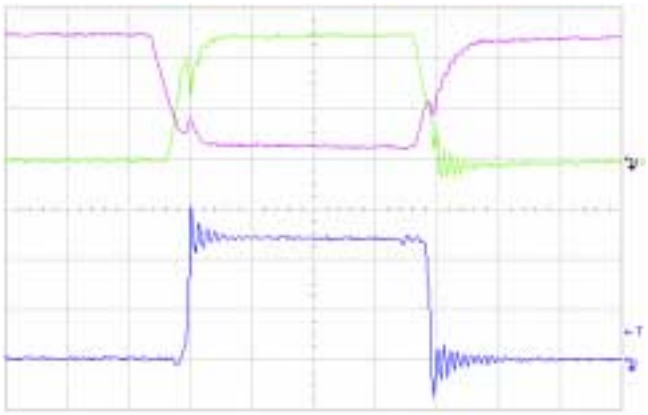

Figure 8. Predictive Gate Drive™ Techology

2.2 What is the difference between Predictive Gate Drive™ and Adaptive Delay Control?

Both of these control techniques aim to achieve the same thing, reducing the amount of delay time between turn-off of the main switch and turn-on of the synchronous switch in a synchronous buck regulator. Reduced delay time translates to minimizing body-diode conduction and reverse recovery time, which increases overall efficiency. The adaptive technique uses current state information from the power stage to control the turn-on of the two gate drivers. By the time the information is detected and processed, some finite dead time is still inevitable. The predictive technique is different from the adaptive technique in that it uses information from the previous switching cycle to set up the dead time for the current cycle. This information is processed in a way that allows the synchronous switch to begin to turn-on while the main switch is not yet fully turned off, yet cross-conduction is completely avoided. The result is that with PGD technology, the dead time between the two switches is nearly zero, resulting in virtually no body-diode conduction.

3 UCC27221/2 General FAQs

3.1 What are the differences between the UCC27221 and the UCC27222?

The UCC27221 has an inverted PWM input while the UCC27222 has a non-inverting PWM input. The UCC27222 is by far the more popular choice and recommended for new designs. However, the UCC27221 is available for applications that historically used a P-channel high-side, N-channel synchronous MOSFET combination. Using the UCC27221, these types of converters can now convert to using a N–channel high-side, N–channel synchronous MOSFET combination without having to change the PWM controller and compensation. With the exception of the inverted input, all other circuitry is identical between the UCC27221 and UCC27222.

3.2 Is there any additional control or compensation circuitry required when using the UCC27221/2?

No. PGD uses control loops that are stabilized internally and are therefore transparent to the designer. These loops use no external components, so no additional design is needed to take advantage of the higher efficiency offered by these drivers.

3.3 What are the noteworthy differences between TPS40000/1/2/3 and UCC27221/2?

The TPS40000/1/2/3 is a synchronous buck solution offering the controller and driver stage with PGD technology in a single 10-pin MSOP PowerPAD™ package. However, the TPS40000/1/2/3 is also limited to a maximum input voltage of 5.5 V, as well as user-selectable fixed frequency operation of either 300 KHz or 600 KHz. The UCC27221/2 is a synchronous buck 3-A driver with PGD in a 14-pin PowerPAD™ package. The UCC27221/2 uses TrueDrive™ output architecture for maximum gate drive capability at higher power levels than TPS40000/1/2/3. Since the UCC27221/2 is a driver stage only, a separate PWM controller is required, offering the designer additional flexibility in terms of controller choices, speed, performance and features. A maximum supply voltage of 20 V and input voltage of 30 V, make the UCC27221/2 well suited for optimal efficiency from intermediate bus voltages found in many of today's most popular distributed power systems.

3.4 What is TrueDrive™ ?

The UCC27221/2 driver stage uses Texas Instrument's unique TrueDrive™ hybrid BiPolar/CMOS output. The TrueDrive™ hybrid architecture consists of a mixed Bipolar CMOS parallel output stage as shown in Figure 9. The advantages of Bipolar are lower capacitance and smaller die size. The advantages of CMOS are direct ohmic connections to the power rails. The TrueDrive™ output stage of the UCC27221/2 combines the advantages of Bipolar and CMOS technologies to maximize drive current while minimizing charge. To the user, this simply means ultra-fast rise and fall times by providing the highest possible drive current where it is needed most, at the MOSFET Miller plateau region. As the output load current increases, the peak MOSFET drain current also proportionally increases, maintaining higher efficiency at higher load currents.

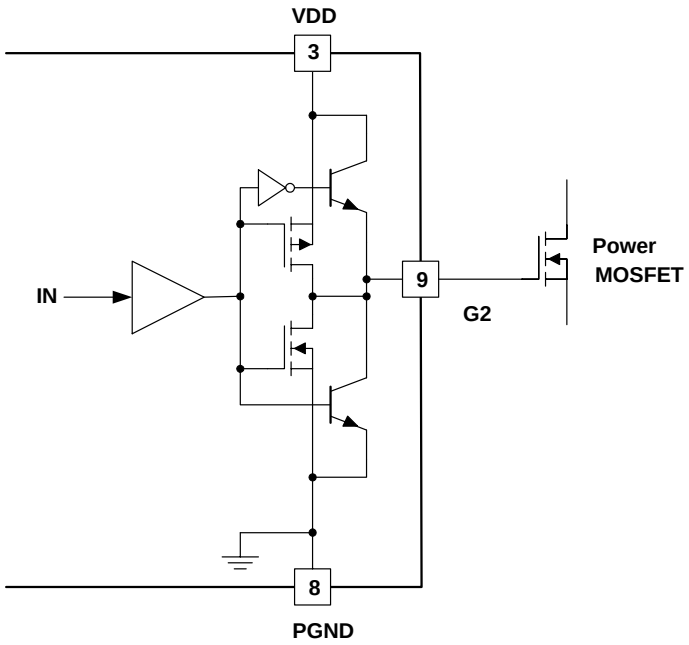

Figure 9. UCC27221/2 TrueDrive™ Hybrid Bipolar CMOS Output Stage

3.5 What types of PWM controllers work best with the UCC27221/2?

Any single-ended current mode, voltage mode or multi-phase PWM controller works well in conjunction with the UCC27221/2. The efficiency gains of the UCC27221/2 can offer tremendous benefit in multi-phase applications where each individual phase would benefit, resulting in a cumulative overall efficiency increase. Configurable with any multi-phase controller, the UCC27221/2 should seriously be considered as a preferred driver in these types of applications. Texas Instruments offers economy and high-performance single-ended PWM controllers with a variety of performance features. For 5-V-only systems, the UCC3803 with 4.1-V turn-on threshold, is a logical choice and is used in several Evaluation Modules (EVM) available from Texas Instruments. The UCC3803 is a BiCMOS current-mode PWM controller that can easily be configured for voltage-mode operation. For 12-V-only systems there are numerous PWM controller choices, such as the UCC3800 offered with a 9.4-V turn-on threshold.

3.6 How can the designer regulate an output voltage that is less than the reference voltage available on PWM controller's internal error amplifier?

Whether internal or external to the PWM, the error amplifier reference voltage does not have to limit how low the regulated output voltage can be. When the desired regulated output voltage is less than the error amplifier reference voltage, the feedback needs to be divided up instead of down. This is accomplished by applying the principle of superposition. Instead of referencing the resistive feedback divider to circuit ground, the divider is referenced to some voltage higher than the output voltage. The UCC3800 family of PWM controllers makes the internal device reference voltage externally available to the designer, allowing divide-up voltage regulation to easily be achieved.

3.7 Can the UCC27221/2 be used to drive a synchronous rectifier output stage of an isolated buck derived power supply topology?

No. The UCC27221/2 is specifically intended for driving a single non-isolated synchronous buck stage only. For isolated buck derived topologies with synchronous rectifier output stages, Texas Instruments is currently developing a secondary side driver utilizing PGD.

3.8 Why was 6.5 V chosen as the gate-drive voltage level for the UCC27221/2?

6.5 V was chosen as an optimal voltage for driving low-voltage logic level MOSFETs typically found in most synchronous buck power stages. As the gate voltage is increased the on resistance of the MOSFET decreases. However, the trade-off occurs in that as the gate voltage increases, the required gate charge also increases. By empirically characterizing gate voltage versus charge and gate voltage versus on resistance, the optimal gate-drive voltage was found to be 6.5 V.

4 Packaging

4.1 In what packages are the UCC27221/2 available?

The UCC27221/2 are only available in Texas Instrument's thermally enhanced 14-pin PowerPAD™ package. This package offers exceptional thermal impedance with a junction-to-case rating of 2°C/W. Shown as the crosshatched region in Figure 10, PowerPAD™ includes an exposed leadframe die pad located on the bottom side of the package. Exposed pad dimensions for the PowerPAD™ TSSOP-14 pin package are 69 mils x 56 mils (1.8 mm × 1.4 mm). However, the exposed pad tolerances can be + 41 / – 2 mils (+ 1.05 /– .05 mm) due to position and mold flow variation. Effectively removing the heat from the PowerPAD™ package requires a thermal land area, shown as the shaded gray region in Figure 10, designed into the PCB directly beneath the package. A minimum thermal land area of 5 mm × 3.4 mm is recommended as illustrated in Figure 10. Any tolerance variances of the exposed PowerPAD™ falls well within the thermal land area when the recommended minimum land area is included on the printed circuit board.

In addition, a 2 by 3 array of 13 mil thermal vias is required within the exposed PowerPAD™ area, as shown in Figure 10. If additional heat sinking capability is required, larger 25 mil vias can be added to the thermal land area.

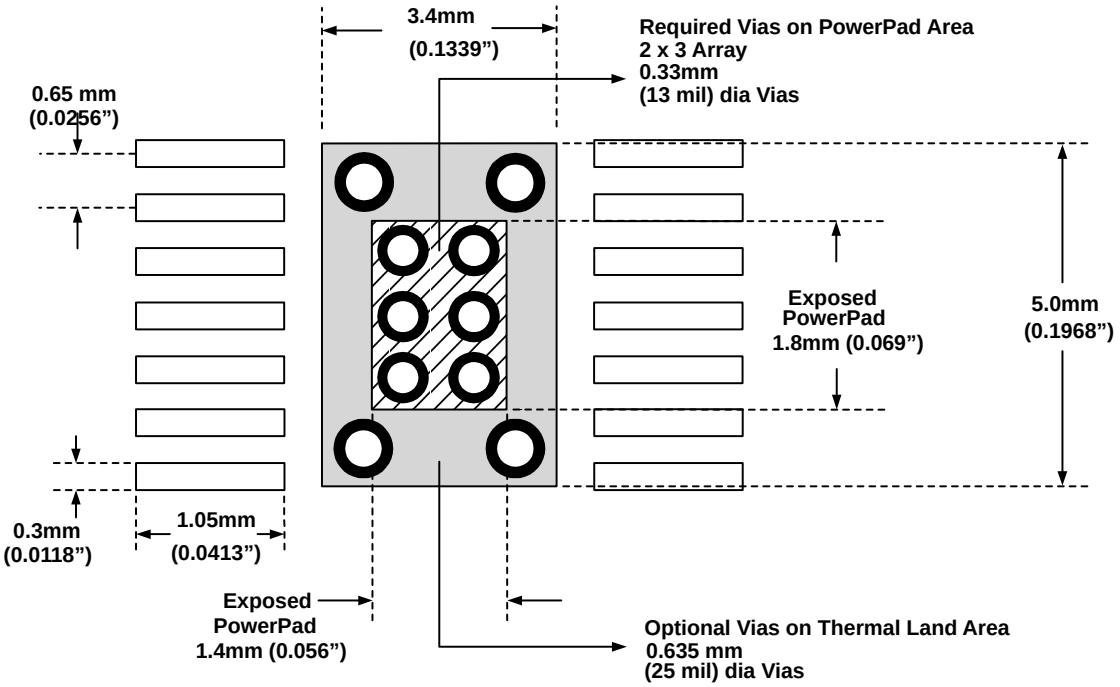

Figure 10. TSSOP-14PWP Package Outline and Minimum PowerPAD™ PCB Thermal Land

4.2 How is the exposed PAD soldered?

The PowerPAD™ package of the UCC27221/2 includes an exposed pad beneath the package that cannot be accessed by contact soldering. Conduction tools can be used for removal, but convection rework techniques are required for placement and recommended for removal as well. Detailed soldering and rework information is available in Appendix B and Appendix C of the Technical Brief, *PowerPAD™ Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002.

4.3 Can the UCC27221/2 operate if the PowerPAD™ is not soldered to a thermal land?

Leaving the exposed PowerPAD™ unsoldered to the minimum thermal land area, shown in Figure 10, does not allow the heat dissipating benefits of the PowerPAD™ package to be realized. The UCC27221/2 can operate with the exposed pad left unconnected, but this is not recommended, due to the high drive current capability of the 3-A TrueDrive™ output stage. When the UCC27221/2 PowerPAD™ is soldered directly to a 2-oz. copper land area as shown in Figure 10, the junction-to-ambient thermal impedance, θ_{JA}, is approximately 37.5°C/W, as opposed to a θ_{JA} of 98°C/W when the PowerPAD™ is not soldered. When the exposed PowerPAD™ is not soldered directly to the printed circuit board land area, the thermal impedance, θ_{JA}, is approximately 3% higher than a standard similar integrated circuit package. For development purposes only, this may or may not be acceptable, and is highly dependant upon the gate charge requirements of the MOSFETs being driven.

4.4 Where can a designer get additional information on PowerPAD™ packaging?

For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating capabilities, including soldering and PCB information, refer to:

1. Application Brief, *PowerPAD™ Made Easy*, Texas Instruments Literature No. SLMA004
2. Technical Brief, *PowerPAD™ Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002

Both of these documents are available through the Texas Instruments website at www.ti.com

5 Efficiency Improvements

5.1 How much overall efficiency improvement can I expect using the UCC27222 with PGD technology?

The exact amount of efficiency gain using PGD is highly dependant upon switching frequency and output voltage. As switching frequency is increased and output voltage is decreased, the efficiency gain of PGD over Adaptive Delay increases. A 5 V-to-0.9 V converter running at 500 KHz using PGD technology can realize an efficiency gain of nearly 4% over Adaptive Delay operating under similar conditions, as shown in Figure 11.

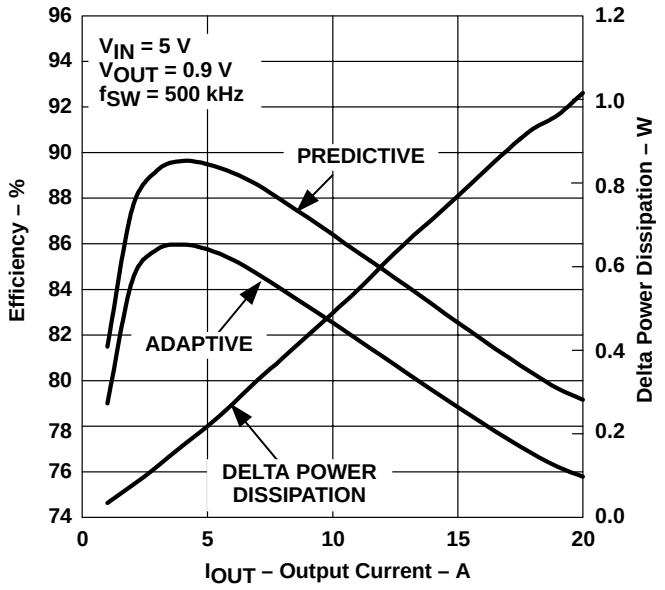

Figure 11. PGD vs. Adaptive Delay Efficiency Improvement

5.2 What are the thermal efficiency improvements of PGD versus Adaptive Delay control?

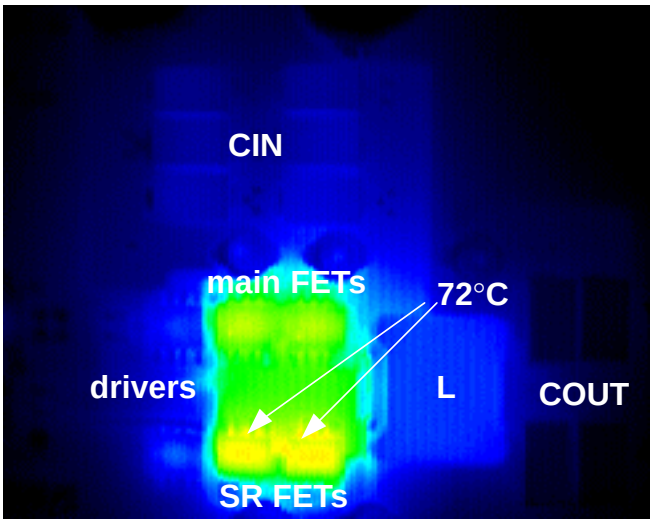

Figure 13. Predictive Gate Drive™

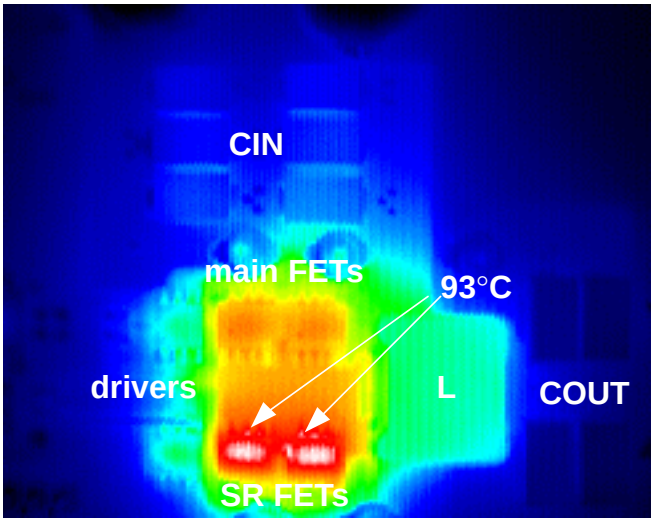

Figure 14. Adaptive Delay Control

White = 93°C, Yellow = 72°C, both images are scaled to the same unit measures. Approximately 21°C delta temperature rise in SR MOSFETs.

Both images shown in Figure 13 and Figure 14 were taken from identical synchronous buck power stages, operating at 500 KHz, from a 5-V input, with a 0.9-V output and a 20-A load. The converter also uses two Hitachi LF PAK MOSFET's in parallel for both the main MOSFETs and synchronous rectifiers.

Comparing the Predictive Gate Drive™ control to the Adaptive Delay control, the power stage using PGD operates approximately 21°C cooler than the same power stage controlled by Adaptive Delay. As expected, the highest thermal benefit is recognized in the synchronous rectifiers controlled by PGD. To the power supply designer, this increase in thermal efficiency translates to lower junction temperatures resulting in increased component reliability, lower failure rates and higher mean time between failure (MTBF). For both power stages operating at similar temperatures, the thermal efficiency gains of a converter using Predictive Gate Drive™ can also be realized in the form of higher output current capability and/or higher operating frequency meaning smaller power stage components

6 Supporting Reference Materials

6.1 What application support materials are available for Predictive Gate Drive™ technology and UCC27221/2?

As of January 2003, the following hardware and documents are all available through the UCC27221/2 Product Folder at www.ti.com. It is advised to check back often as additional support materials become available.

- UCC27222EVM: 12 V input, 1.8 V output, 20 A output using UCC27222 High-Efficiency Synchronous Buck Driver with Predictive Gate Drive™ Technology and UCC3803 Low-Power BiCMOS Current-Mode PWM configured for voltage-mode operation.
- UCC27222EVM–001: 5 V input, 1.8 V output, 20 A output using UCC27222 High-Efficiency Synchronous Buck Driver with Predictive Gate Drive™ Technology and UCC3803 Low–Power BiCMOS Current–Mode PWM configured for voltage-mode operation.
- SLUU140 – 12 V to 1.8 V, 20A High-Efficiency Synchronous Buck Converter Using UCC27222 with Predictive Gate Drive™ Technology, User Guide to accommodate UCC27222EVM
- SLUU147 – 5 V to 1.8 V, 20 A High-Efficiency Synchronous Buck Converter Using UCC27222 with Predictive Gate Drive™ Technology, User Guide to accommodate UCC27222EVM–001
- SLUS486A – UCC27221/2 Data Sheet, Application Information
- SLUP175 – Power Supply Design Seminar SEM–1400 Topic 7: The Implication of Synchronous Rectifiers to the Design of Isolated Single-Ended Forward Converters, by Christopher Bridge.
- SLUA281 – Predictive Gate Drive™ Boosts Synchronous DC/DC Power Converter Efficiency, by Steve Mappus

7 References

1. Power Supply Design Seminar SEM-1400 Topic 2: *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments Literature No. SLUP169.
2. Power Supply Design Seminar SEM-1400 Topic 7: *Implication of Synchronous Rectifiers in Isolated, Single-Ended, Forward Converters*, by Christopher Bridge, Texas Instruments Literature No. SLUP175.
3. UCC27221/2 High-Efficiency Predictive Synchronous Buck Driver Datasheet, Texas Instruments Literature No. SLUS486A.
4. TPS40000/1/2/3 Low-Input Voltage-Mode Synchronous Buck Controller Datasheet, Texas Instruments Literature No. SLUS507A.
5. *PowerPAD™ Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002.
6. *Predictive Gate Drive™ Boost Synchronous DC/DC Power Converter Efficiency*, by Steve Mappus, Texas Instruments Literature No. SLUA281.

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