UCC38C44 12-V Isolated Bias Supply

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ABSTRACT

This reference design describes a discontinuous, peak current-mode flyback converter whose input voltage is generated from the output of a universal power factor correction circuit. The converter is designed to operate at a switching frequency of 225 kHz, requires minimal parts, and supports an isolated 12-V, 3-W output and a non-isolated 12-V, 1-W output ideally suited for chip bias and voltage feedback control.

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1 Introduction

The UCC38C44 BiCMOS low-power current-mode pwm controller is used in this design because it is an enhanced version of the industry standard UC3842 family of devices. This BiCMOS version offers lower start-up and operating currents, faster current-sense-to-output delay time with improved output rise and fall times resulting in a higher performance device suitable for high-frequency, high-efficient systems while maintaining a similar conceptual functionality as the bipolar version. The complete design schematic is shown in Figure 1.

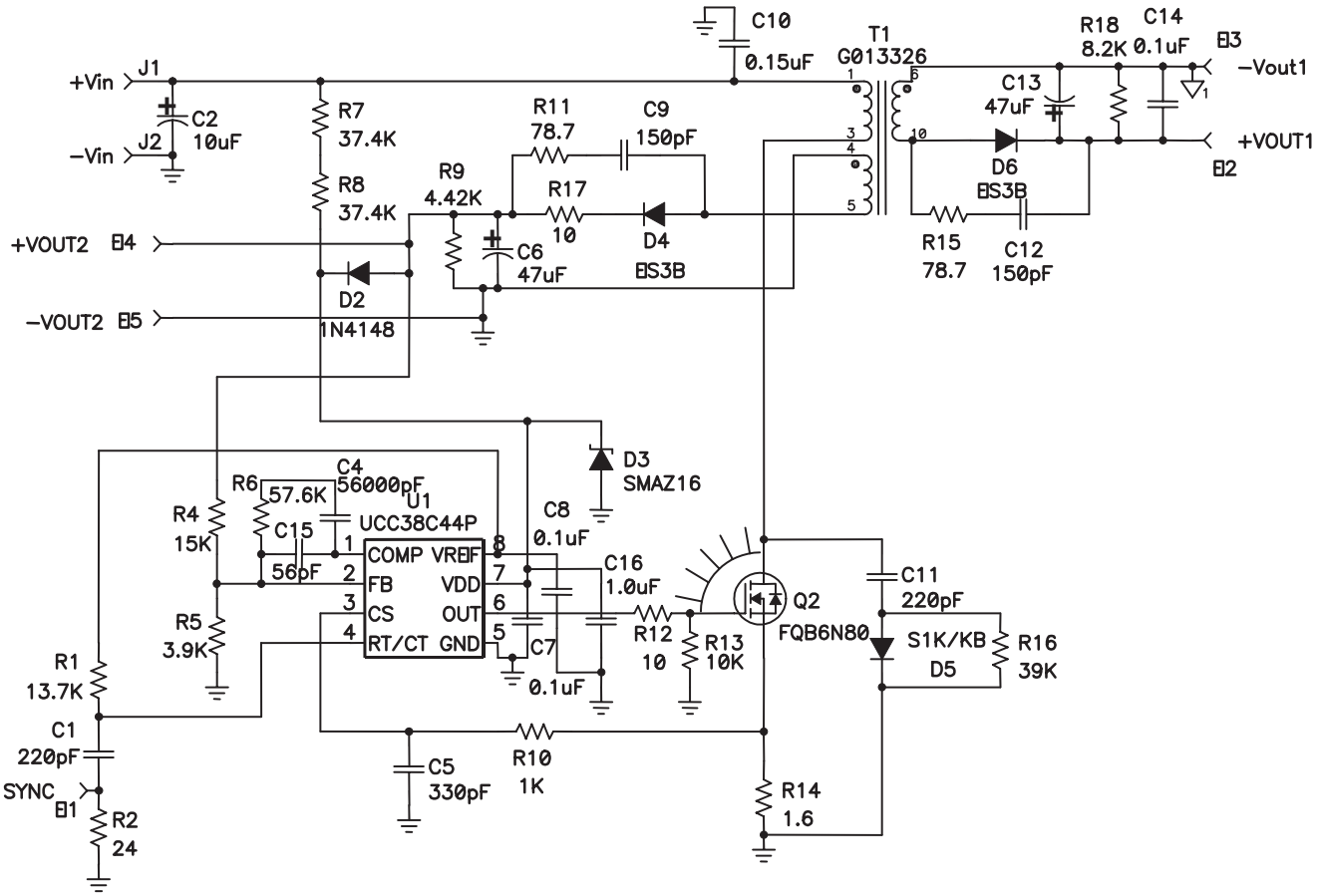

Figure 1. 12-V Flyback Bias Supply

1.1 Features

- PFC output stage input voltage range: $V_{IN(min)}$ = 100 Vdc, $V_{IN(max)}$ = 400 Vdc
- Isolated output
  - $V_{OUT(isolated)}$ = 12 Vdc
  - maximum load: $I_{OUT(isolated)}$ = 250 mA
  - maximum continuous power = 3 W
- Non-isolated output
  - $V_{OUT(non\text{-}isolated)}$ = 12 Vdc
  - maximum load: $I_{OUT(non\text{-}isolated)}$ = 83.3 mA
  - maximum continuous power = 1 W
- High-efficiency 225 kHz switching frequency (f_{SW})
- Low device start-up and operating currents
- Primary side voltage feedback eliminating the need for an external error amplifier, reference voltage, and optocoupler
- External synchronous input

2 Circuit Design Parameters

2.1 Maximum Duty Cycle, Oscillator, and Synchronization Input

The maximum duty cycle, D_{MAX}, is chosen to be 40%, allowing for equal off-time and a 20% dead-time margin to guarantee discontinuous operation throughout the entire operating range. The UCC38C44 PWM is ideally suited for designs with a maximum duty cycle of less than 50%. This device contains an internal toggle flip-flop which effectively clamps the output duty cycle to a maximum of 50%. The oscillator must be set up to operate at twice the desired output frequency because the PWM output is inhibited during every other oscillator pulse. The oscillator components are chosen based upon *Figure 6. Oscillator Frequency vs Timing Resistance and Capacitance*, in the UCC38C44 datasheet, TI Literature No. SLUS458. Using a 220-pF NPO capacitor and a 13.7-kΩ, 1% resistor resulted in a switching frequency of 225 kHz. A 24-Ω resistor from the timing capacitor to ground provides an insertion point for synchronization to an external clock source, as described in the data sheet.

2.2 Flyback Transformer Design

Because this supply was designed with cost in mind, the flyback topology was chosen. Flyback converters are more economical than other isolated topologies due to their minimal parts count. There is no need for an output L-C filter and this topology requires only one diode for each output. The basic flyback is based upon the buck-boost converter topology. Flyback converters operate by building up the current in the primary when the switch is on. During this on time, the load current is provided by the output capacitor. When the switch is opened, the current reverts to the secondary winding and flows through the diode and into the load. The transfer function relating the input voltage to the output voltage is determined by the turns ratio of the transformer windings and the maximum duty cycle, as shown in the following equation:

$$\frac{V_{OUT}}{V_{IN(min)}} = \frac{D_{MAX}}{N \times \left(1 - D_{MAX}\right)} \tag{1}$$

From this equation, the turns ratio, N, is rounded up to 6. The turns ratio ensures the Volt-second (V-s) product during the on time of the switch is equal to the V-s product during the off-time, preventing the core from saturation. Because the UCC38C44 requires a bias voltage between the UVLO lower threshold of 9 V and the maximum recommended input voltage of 18 V, the turns ratio for the non-isolated winding is also 6. Using this turns ratio, the maximum duty cycle is recalculated to be equal to 0.347. With this D_{MAX}, the maximum on time of the switch is calculated to be $t_{ON(max)} = D_{MAX} \times T$, where T is the switching period (equal to $1/f_{SW}$).

The maximum primary inductance, $L_{P(max)}$, is calculated at low input line, maximum load, assumes an efficiency, n, of 50%, and takes into account the voltage drop across the FET, which is calculated based upon the $R_{DS(on)}$ of the selected switch and the peak current through it, V_{DS} is assumed to be equal to 1.4 V.

$$L_{P(max)} = n\frac{\left[\left(V_{IN(min)} - V_{DS}\right) \times t_{ON(max)}\right]^2}{\left(2 \times T \times P_{OUT(total)}\right)} = 369\ \mu H \tag{2}$$

From equation(3), the peak primary current and the stored energy it represents can be determined.

$$I_{PEAK(pri)} = n\frac{\left[\left(V_{IN(min)} - V_{DS}\right) \times t_{ON(max)}\right]}{L_P} \tag{3}$$

$$E = \frac{1}{2} \times L_P \times \left(I_{PEAK(pri)}\right)^2$$

A ferrite EE−13 core with a primary inductance of 300-μH proved sufficient, resulting in a peak flux density of 800 Gauss.

2.3 Current Mode Control

Peak current-mode control determines the modulation of the switch. At the beginning of each switching cycle, current in the primary begins to rise. This current develops a voltage across the sense resistor. This voltage is fed into the current-sense input of the UCC38C44, which has a threshold voltage of 1 V. The resistor is selected such that the overcurrent detect is at approximately 10% higher than the peak current while in its normal operating range.

A leading-edge blanking filter, consisting of a resistor and a capacitor, is added to filter out any leading-edge spikes or noise caused by the reverse recovery of the output rectifier, equivalent capacitive loading on the secondary, and any inductive circuit effects. Note that this filter interferes with the fast over current protection circuit by adding an additional delay to the current sensing signal.

$$R_{SENSE} = \frac{CS_{THRESHOLD}}{1.1 \times I_{PEAK(pri)}} \tag{4}$$

2.4 MOSFET and Rectifier Requirements

The MOSFET switch is subjected to voltage stresses from the maximum input voltage, the reflected output voltage, and the induced voltage spike due to the inevitable leakage inductance. When allowing a 30% margin for the leakage inductance spike, the stress on the switch can be calculated as shown in equation (5).

$$V_{DS(stress)} = \left(V_{IN} - V_{DS}\right) + N \times \left(V_{OUT} + V_F\right) + 0.3 \times V_{IN} \tag{5}$$

Plotting $V_{DS(stress)}$ as a function of V_{IN}, it becomes apparent that a device rated for 800 V is required.

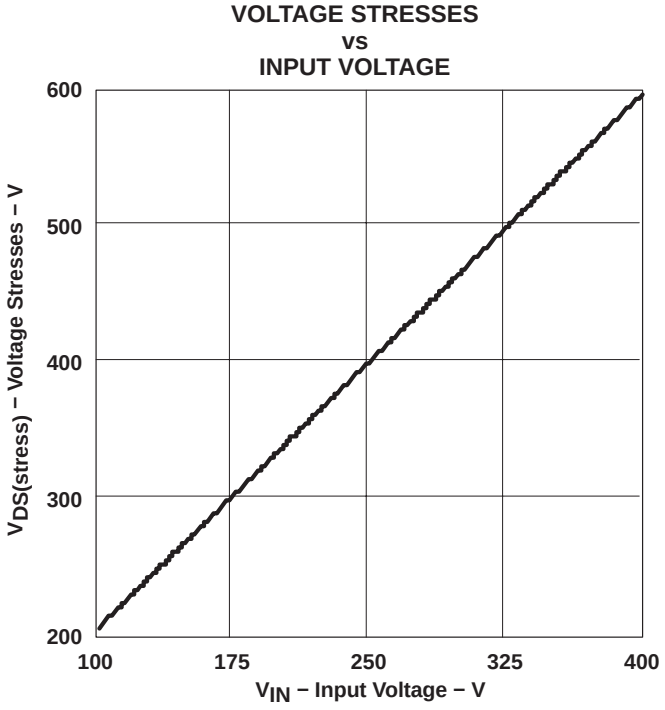

Figure 2.

An 800V N-channel MOSFET FQB6N80 from Fairchild, rated for 3.67-A of continuous current and $R_{DS(on)}$ = 1.95Ω at 100°C meets the design requirements. The switch conduction losses are calculated using the primary side root mean squared (RMS) current. For a discontinuous mode flyback converter, the current is a clipped saw tooth waveform:

$$I_{RMS} = \frac{I_{PEAK(pri)}}{\sqrt{3}} \times \sqrt{\frac{t_{ON(max)}}{T}} \quad (6)$$

$$P_{FET(cond)} = \left(I_{RMS}\right)^2 \times R_{DS(on)} \quad (7)$$

The switching losses are a combination of the losses associated with charging the output capacitance of the switch, C_{OSS}, and the charging of the Miller capacitor, Q_{GD}, at switch turn-on. These losses are estimated as follows:

$$P_{FET(sw)} = f_{SW}\left(\frac{1}{2} \times C_{OSS} \times \left(V_{DS(stress)}\right)^2 + \frac{1}{2} \times V_{DS(stress)} \times I_{PEAK(pri)} \times t_{MILLER}\right) \quad (8)$$

where:

- $t_{MILLER} = (Q_{GD} \times R_{GATE})/V_{DD}$
- R_{GATE} is a 10-Ω gate drive resistor

Any oscillations caused by the parasitic wiring inductance and the FET's input capacitance is dampened by this small resistor. To ensure the MOSFET gate does not get charged to its turn-on threshold during device start-up, a pull-down resistor is added to the gate drive. Because the total losses for this device add up to approximately 1.8 W, a heat sink is required to maintain the junction temperature (T_J) within the safe operating range.

The output rectifier needed for each output must support a reverse voltage, V_{REV}, equal to the reflected input voltage and the output voltage of the converter and be capable of handling the secondary-side peak current. The ES3B fast rectifier from Fairchild, with a forward voltage, V_F, of 0.9 V and a total capacitance, C_{DIODE}, of 45 pF, met these requirements. The rectifier losses are estimated by adding the conduction losses, the reverse leakage losses, and the capacitive losses:

$$P_{DIODE(cond)} = V_F \times I_{OUT} \quad (9)$$

$$P_{DIODE(rev)} = I_{LEAK} \times V_{REV} \times D \quad (10)$$

$$P_{DIODE(cap)} = \frac{1}{2} \times C_{DIODE} \times \left(V_{OUT}\right)^2 \times f_{SW} \quad (11)$$

2.5 Snubber and Clamp Design

An RCD clamp was used on the primary side to suppress the voltage spike induced by the leakage inductance of the transformer. The capacitor, $C_{PRI(clamp)}$, was chosen to clamp the voltage across the switch, ΔV, to approximately 60 V. The resistor, $R_{PRI(clamp)}$, is selected such that the R-C time constant is twice that of the switching period. This resistor must not only dissipate the energy stored in the leakage inductance, but also the voltage due to the dc bias of the capacitor. The diode is selected based upon the charging current of the capacitor.

$$C_{PRI(clamp)} = \frac{L_{LEAK} \times \left(I_{PEAK(pri)}\right)^2}{\left[\Delta V \times \left(\Delta V + 2N \times \left[V_{OUT} + V_F\right]\right)\right]} \quad (12)$$

$$R_{PRI(clamp)} = \frac{2T}{C_{PRI(clamp)}} \quad (13)$$

$$P_{RPRI(clamp)} = \frac{\frac{1}{2} \times L_{LEAK} \times \left(I_{PEAK(pri)}\right)^2 \times f_{SW} + \left[N \times \left(V_{OUT} + V_F\right)\right]^2}{R_{PRI(clamp)}} \quad (14)$$

The suspected ringing on the secondary side, without a snubber, is determined by the resonant tank frequency created by the reflected leakage inductance and the junction capacitance of the output diode:

$$f_{RING} = \frac{1}{2\pi\sqrt{L_{LEAK} \times C_{DIODE}}} \quad (15)$$

The optimum value for the snubber capacitor is three times the diode capacitance, resulting in a damping Q-value very close to one. This added value decreases the ringing frequency by one-half. The snubber resistor provides critical damping to the oscillation.

$$C_{SNUB} = 3 \times C_{DIODE} \quad (16)$$

$$R_{SNUB} = \sqrt{\frac{\left(\frac{L_{LEAK}}{N^2}\right)}{C_{DIODE}}} \quad (17)$$

Because the time constant of this R-C snubber is much less than the switching period, but much longer than the voltage rise time, the power dissipated by the resistor is dependent upon the energy stored in the capacitor. Since the capacitor charges and discharges each cycle, the power dissipated is equal to:

$$P_{R(SNUB)} = C_{SNUB} \times \left[\left(\frac{V_{DS(stress)}}{N}\right) - \left(V_{OUT} + V_F\right)\right]^2 \times f_{SW} \quad (18)$$

2.6 Capacitor Selection

The output capacitor selection is first based upon its ability to handle the ac portion of the secondary side output current, calculated according to the following equation:

$$I_{ac(RMS)} = I_{PEAK(sec)} \times \sqrt{\left[\left(\frac{T - t_{ON(max)}}{T}\right) \times \frac{4 - 3 \times \left(\frac{T - t_{ON(max)}}{T}\right)}{12}\right]} \quad (19)$$

The maximum acceptable peak-to-peak output ripple voltage was chosen to be 2% of the output voltage. The output capacitance contributes to the voltage ripple according to the following relationship:

$$V_{CAP} = \frac{\left[\frac{1}{2} \times \left(T - t_{ON(max)}\right) \times I_{PEAK(sec)}\right]}{C_{OUT}} \quad (20)$$

The voltage ripple contribution from the output capacitor's ESR is a result of the peak secondary current. Given the maximum ripple voltage is limited to $0.02 \times V_{OUT}$, the maximum allowable ESR can be calculated:

$$ESR = \frac{\sqrt{\left(0.02 \times V_{OUT}\right)^2 - \left(V_{CAP}\right)^2}}{I_{PEAK(sec)}} \quad (21)$$

A Vishay 47-µF type 94SA met the ripple current requirements and was used for each output. A small ceramic capacitor across the isolated output terminals helped to smooth out high frequency noise and a 10-Ω resistor helped to peak charge the non-isolated output used to bias the device. Each output was also pre-loaded to guarantee output loads within the minimum required range.

The size of the input capacitor is determined by the ripple current, peak voltage, and the energy storage requirements. The desire was to keep the input voltage ripple limited to 10% of the input voltage at full-load, low-line conditions. Assuming 50% converter efficiency, the energy storage requirements, and the resultant minimum input capacitance, can be determined:

$$E_{IN} = \frac{P_{OUT(total)}}{\left(4 \times f_{SW}\right)} \tag{22}$$

$$C_{IN} = \frac{2 \times E_{IN}}{\left(0.1 \times V_{IN(min)}\right)^2} \tag{23}$$

A Panasonic aluminum electrolytic 450-V, 10-µF EB-series capacitor met the criteria. An additional small (0.15-µF) ceramic capacitor is placed physically close to the transformer to help filter out high-frequency noise from the circuit.

2.7 Device Bias and Voltage Feedback

The non-isolated output is utilized to bias the primary side controller. This controller, the UCC38C44, receives its start-up current from the input line via the start up resistor. The start-up current requirement through this resistor must supply the device with its maximum rated start-up current and must also charge the bypass capacitor up to the maximum UVLO turn on threshold. Using a 1-µF bypass capacitor, placed as physically close to the device as possible, the start-up resistor value can be calculated:

$$R_{START} = \frac{V_{IN(min)} \times \ln\left[\frac{\left(-V_{UVLO(max)} + V_{IN(min)}\right)}{V_{IN(min)}}\right] + V_{UVLO(max)}}{I_{START(max)} \times \ln\left[\frac{\left(-V_{UVLO(max)} + V_{IN(min)}\right)}{V_{IN(min)}}\right]} \tag{24}$$

Two resistors are needed due to the high voltage drop across them when the input line is at its maximum value. Because the absolute maximum supply voltage rating for the device is 20 Vdc, which includes all noise spikes and transient conditions, a 16-V zener protection diode is added from the supply to ground.

This non-isolated winding is also used for the voltage feedback signal. The output voltage of this winding is resistively divided down and input into the FB pin of the controller device. Using this winding eliminates the need for the signal to cross the isolation boundary, eliminating the need for an optocoupler, secondary side error amplifier, and reference voltage. Unfortunately, by using this winding as the master, the isolated output becomes a slave output resulting in a predicted regulation of only 8% whereas the non-isolated output will be much better regulated. Preloading this output helped maintain its regulation to within 5% at minimal cost to efficiency.

2.8 Compensation

In order to have good dynamic response and adequate line and load regulation, the voltage feedback loop must be closed about the error amplifier with a compensation network that results in optimum closed loop bandwidth. Optimum closed-loop performance can be achieved only by first knowing what the transfer characteristic of the power stage looks like. The power stage DC gain, the power stage pole resulting from the output capacitance and the load, and the ESR-zero directly resulting from the output capacitance and its parasitic impedance must first be calculated:

$$f_{PWRSTG(pole)} = \frac{1}{2\pi \times R_{OUT} \times C_{OUT}} \tag{25}$$

$$f_{ESR(zero)} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (26)$$

$$PWRSTG_{DC(gain)} = \frac{V_{IN}}{I_{PEAK(pri)}} \times \sqrt{\frac{R_{OUT} \times n}{2 \times L_P \times f_{SW}}} \quad (27)$$

$$G_{PS}(f) = 20 \log\left[\left|PWRTSG_{DC(gain)} \times \left(\frac{1 + s(f) \times ESR \times C_{OUT}}{1 + s(f) \times R_{OUT} \times C_{OUT}}\right)\right|\right] \quad (28)$$

$$s(f) = j \times 2\pi \times f \quad (29)$$

A Bode plot is used to graph the results of the above equation, and its corresponding phase, at all four operating corners as a function of frequency:

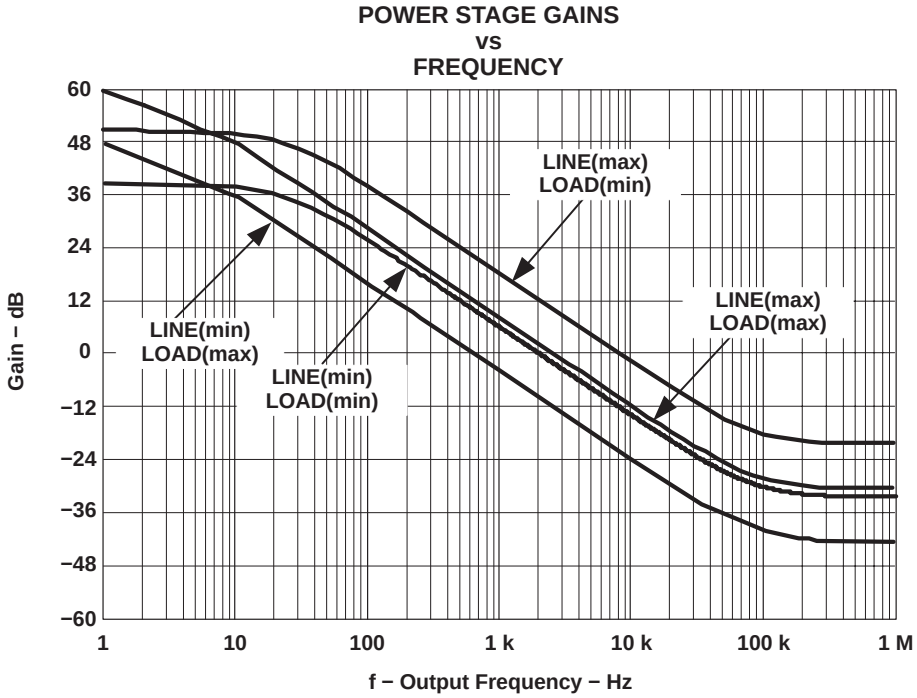

Figure 3. Bode Plot of the Power Stage Gain

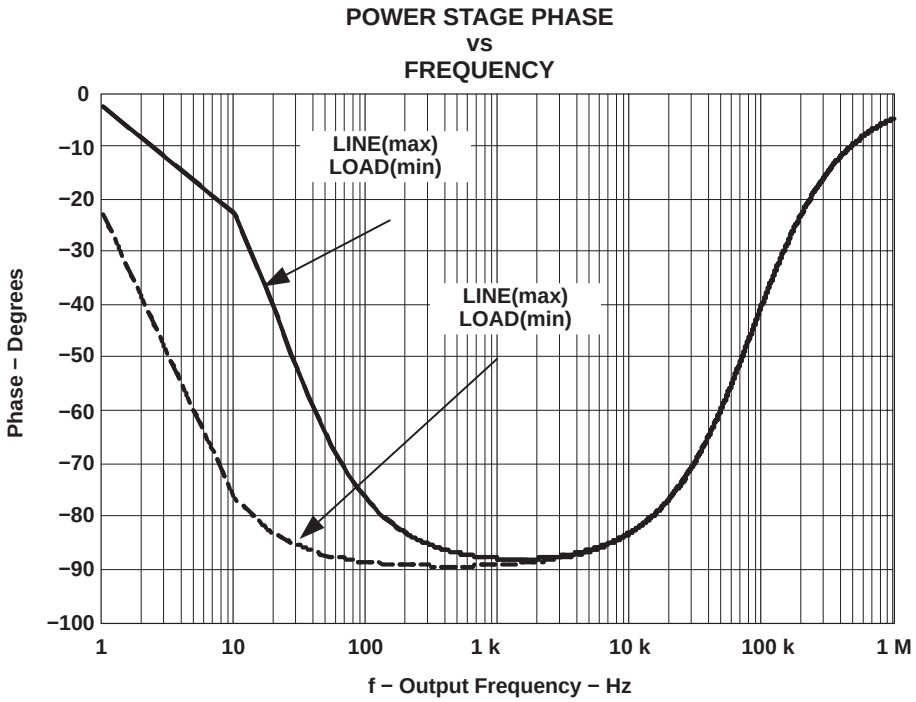

Figure 4. Bode Plot of the Power Stage Phase

A type II amplifier is used to compensate the loop. The best possible loop crossover frequency for stability is equal to $f_{SW}/2\pi D_{MAX}$, a realistic goal is more on the order of $f_{SW}/4$. Because this frequency falls very close to the ESR zero, the crossover frequency is chosen to be at f_C = 10 kHz. Approximately 24 dB of gain is required. The ESR zero is cancelled by adding a pole at, ideally, one-tenth the ESR zero frequency. This decade offset increases the low-frequency gain and adds 45° of phase lag. Unfortunately, with a one-decade lead, the ESR zero is at approximately equal to the crossover frequency. The pole is then added at approximately f_{POLE} = 50 kHz and a zero is needed at f_{ZERO} = 50 Hz. The required error amplifier gain and its implementation, can be determined using the following relationships:

$$EA_{GAIN}\,(dB) = 24 + 20\,\log\left(\frac{f_C}{f_{POLE}}\right) \tag{30}$$

$$R_{EA} = 10^{\left(\frac{EA_{GAIN}}{20}\right)} \times R_{FB} \tag{31}$$

$$C_{EA} = \frac{1}{2\pi \times R_{EA} \times f_{ZERO}} \tag{32}$$

Where:

- R_{EA} is shown as R6 in Figure 1
- R_{FB} is shown as R4 in Figure 1
- C_{EA} is shown as C4 in Figure 1

The obtain the desired pole to offset the ESR zero, the capacitor needed in parallel, shown as C15, is calculated:

$$C_{EA[\|]} = \frac{1}{2\pi \times R_{EA} \times f_{POLE}} \tag{33}$$

Plotting the error amplifier compensation:

$$GAIN_{EA)}(f) =$$

$$20 \log \left[\left| \frac{1 + s(f) \times R_{EA} \times C_{EA}}{\left(s(f) \times R_{FB1}\right) \times \left[\left(C_{EA} + C_{EA[\|]} \right) \times \left[1 + \frac{s(f) \times R_{EA} \times C_{EA} \times C_{EA[\|]}}{\left(C_{EA} + C_{EA[\|]} \right)} \right] \right]} \right| \right] \quad (34)$$

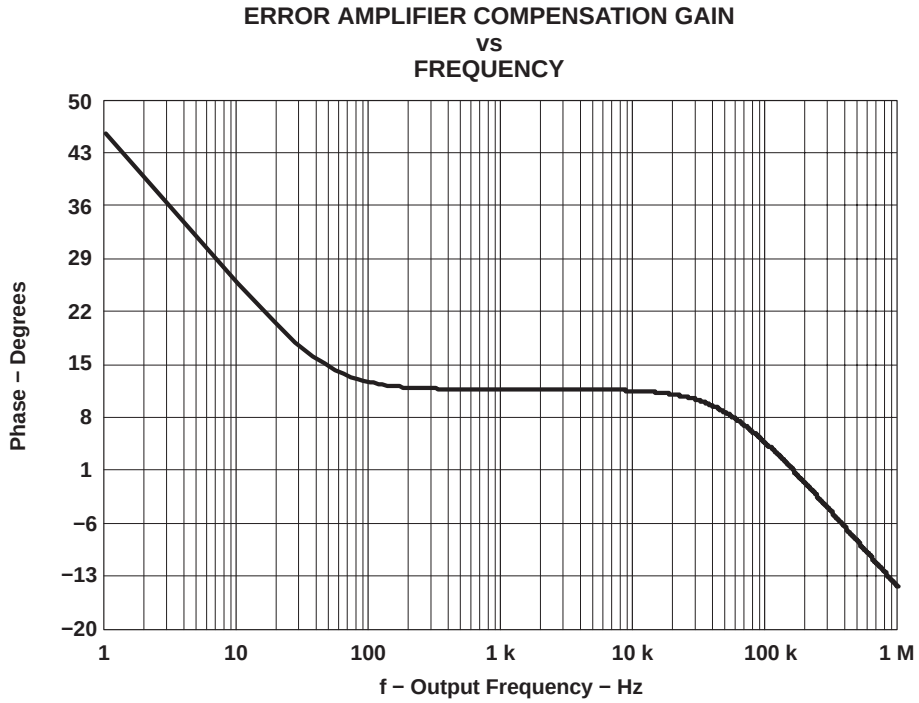

Figure 5. Bode Plot of Error Amplifier Compensation Gain

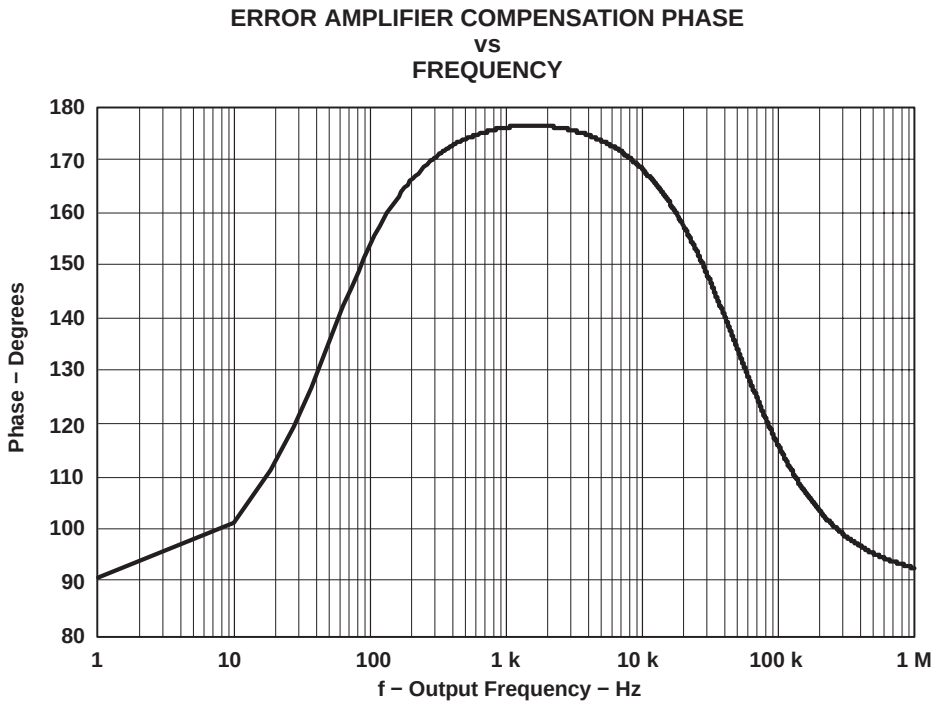

Figure 6. Bode Plot of Error Amplifier Compensation Phase

The combined closed-loop Bode plots show a nominal crossover frequency of 10 kHz with a phase margin of approximately 80°.

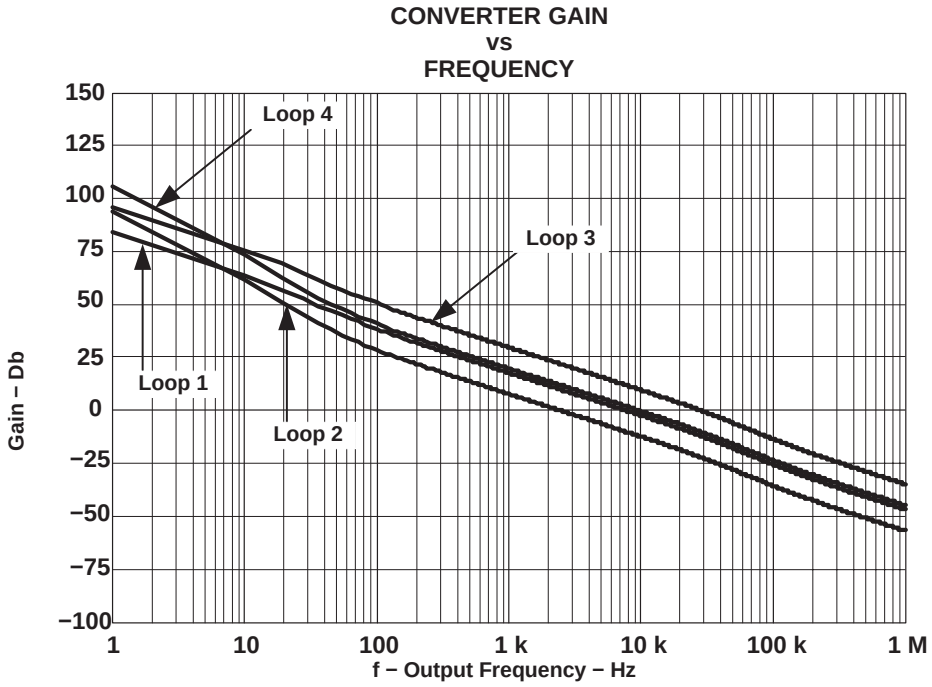

Figure 7. Closed Loop Bode Plot of the Converter Gain

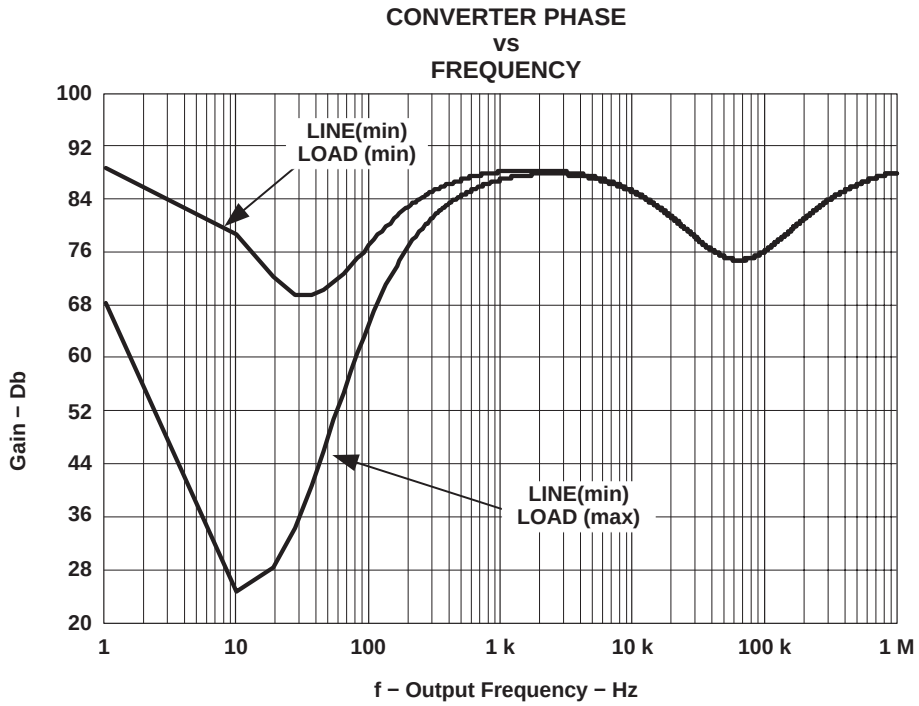

Figure 8. Closed Loop Bode Plot of the Converter Phase

3 Reference Design Performance

The following graphs show the overall performance of the reference design.

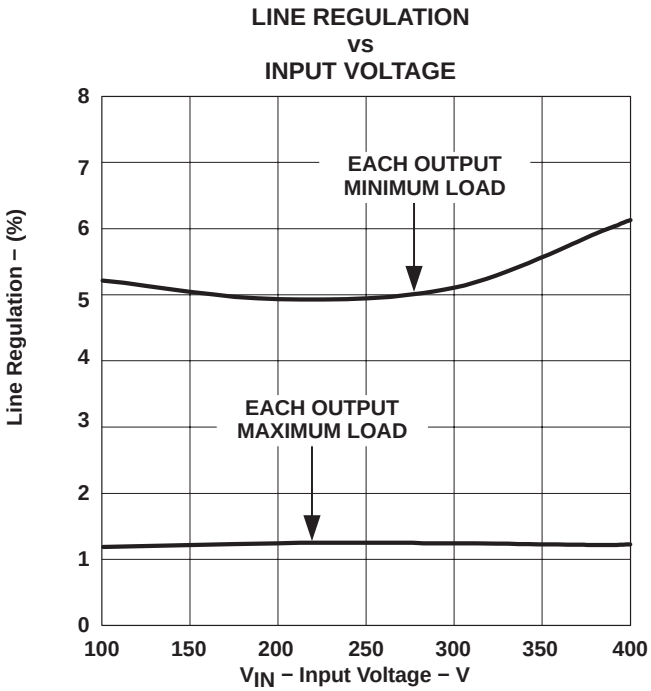

Figure 9.

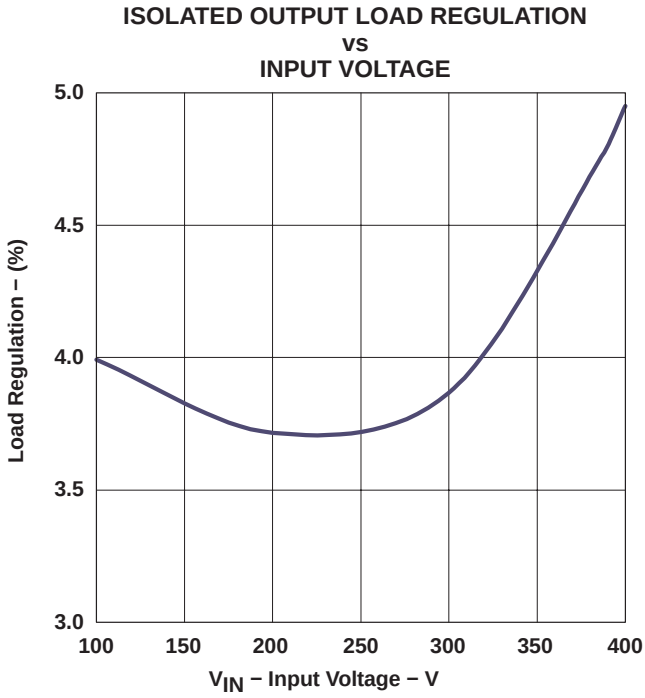

Figure 10.

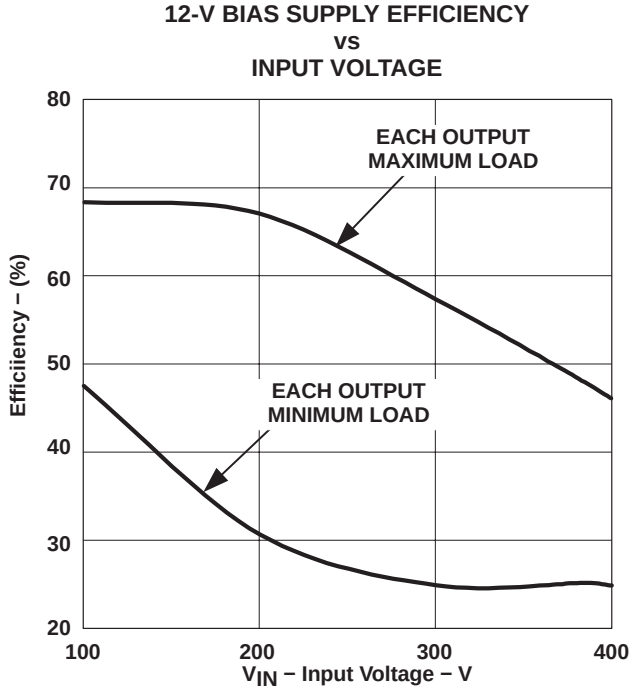

Figure 11.

4 Design Description

4.1 List of Materials

. List of Materials

REFERENCE DESIGNATOR	QTY	PART NUMBER	DESCRIPTION	MANUFACTURER
C1	1	ECJ−2VC1H221J	Capacitor, ceramic, 220 pF, ±5%, 50 V, NPO	Panasonic
C2	1	EEV−EB2W100SN	Capacitor, aluminum, 10 µF, ±20%, 450 V	Panasonic
C4	1	ECJ−2VB1C563K	Capacitor, ceramic, 56000 pF, ±10%, 16 V, X7R	Panasonic
C5	1	ECJ−1VC1H331J	Capacitor, ceramic, 330 pF, ±5%, 50 V, NPO	Panasonic
C6, C13	2	94SA476X0020EBP	Capacitor, aluminum, 47 µF, ±20%, 20v	Vishay
C7, C8, C14	3	ECJ−2YB1H104K	Capacitor, ceramic, 0.1 µF, ±10%, 50 V, X7R	Panasonic
C9, C12	2	ECJ−2VC2A151J	Capacitor, ceramic, 150 pF, ±5%, 100 V, NPO	Panasonic
C10	1	1825CC154KA19A	Capacitor, ceramic, 0.15 µF, ±5%, 600 V, COG	Avx
C11	1	1825AA221JA19A	Capacitor, ceramic, 220 pF, ±5%, 1000 V, COG	Avx
C15	1	ECJ−2VC1H560J	Capacitor, ceramic, 56 pF, ±5%, 50 V, NPO	Panasonic
C16	1	C1206C105K3RACTU	Capacitor, ceramic, 1 µF, ±10%, 25 V, X7R	Kemet
D2	1	1N4148W−7	Rectifier, switching, 75 V, 350 mW	Diodes, Inc.
D3	1	SMAZ16	Rectifier, zener, 16 V, 1 W	Diodes, Inc.
D4, 6	2	ES3B	Rectifier, superfast, 100 V, 3 A	Fairchild
D5	1	S1K/KB	Rectifier, 800 V, 1 A	Diodes, Inc.
E1, E2, E3, E4, E5	5	K24C/M	Terminal pins	Vector
H1	1	573300	Heatsink	Aavid
J1	1	111−0702−001	Insulated binding post, red	Johnson
J2	2	111−0703−001	Insulated binding post, black	Johnson
Q2	1	FBQ6N90	MOSFET, N−channel, 900 V, 5.8 A, 1.95 Ω	Fairchild
R1	1	ERJ−6ENF1372V	Resistor, thick film, 13.7 kΩ, ±0.1%, 1/10 W	Panasonic
R2	1	ERJ−6GEYJ240	Resistor, thick film, 24 Ω, ±5%, 1/10 W	Panasonic
R4	1	ERA−6YEB153V	Resistor, thick film, 15 kΩ, ±0.1%, 1/10 W	Panasonic
R5	1	ERA−6YEB392V	Resistor, thick film, 3.9 kΩ, ±0.1%, 1/10 W	Panasonic
R6	1	ERJ−6ENF5762V	Resistor, thick film, 57.6 kΩ, ±5%, 1/10w	Panasonic
R7, R8	2	9C12063A3742JLHFT	Resistor, thick film, 37.4 kΩ, ±5%, 1/4 W	Phycom
R9	1	ERJ−6ENF4421V	Resistor, thick film, 4.42 kΩ, ±1%, 1/10 W	Panasonic
R10	1	ERJ−6GEYJ1R0V	Resistor, thick film, 1.0 Ω, ±5%, 1/10 W	Panasonic
R11, R15	2	ERJ−14NF78R7U	Resistor, thick film, 78.7 Ω, ±1%, 1/4 W	Panasonic
R12, R17	2	ERJ−6GEYJ100V	Resistor, thick film, 10 Ω, ±5%, 1/10 W	Panasonic
R13	1	ERA−6YEB103V	Resistor, thick film, 10.0 kΩ, ±0.1%, 1/10 W	Panasonic
R14	1	ERJ−12ZYJ1R6U	Resistor, thick film, 1.6 Ω, ±5%, 1/2 W	Panasonic
R16	1	ERJ−1WYJ393U	Resistor, thick film, 39 kΩ, ±5%, 1 W	Panasonic
R17	1	ERJ−6GEYJ822V	Resistor, thick film, 8.2 kΩ, ±5%, 1 W	Panasonic
T1	1	G013326	Transformer, EE13, 300 µH	GCI Technologies
U1	1	UCC38C44P	Bicmos low-power current-mode PWM controller	Texas Instruments
	1		PCB, FR4, 2−Layer, 1 OZ, 2.90”(L) X 2.50”(W) X 0.062”(T)	
	4	1902D	4-40 Threaded nylon standoff	Keystone
	4	NSS−4−4−01	1/4 Inch 4-40 nylon screw	Richo

4.2 Physical Layout

4.2.1 Top Layer Component Placement

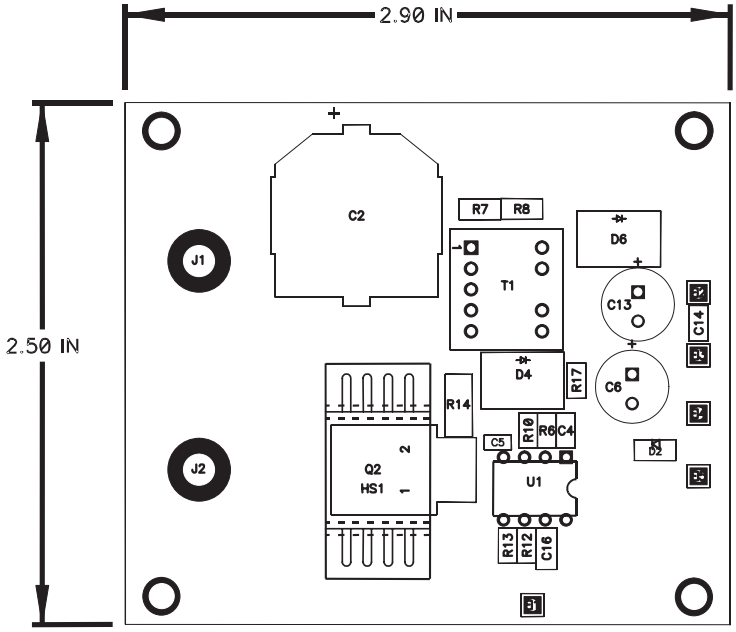

Figure 12. Top Layer Component Placement

4.2.2 Top Layer Route

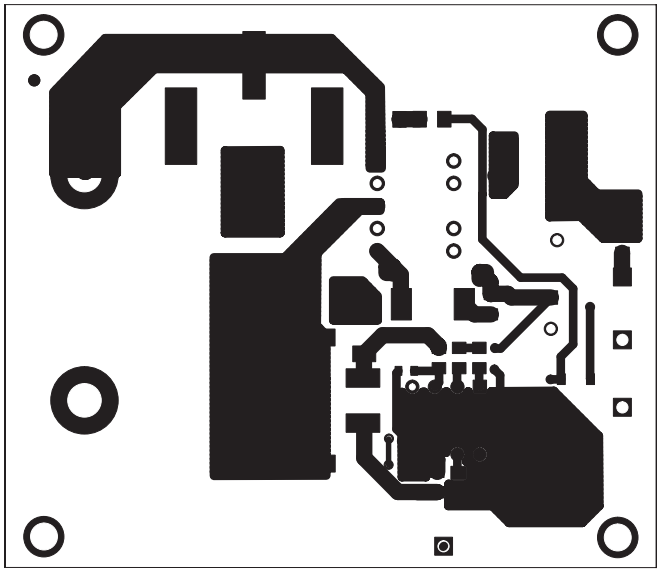

Figure 13. Top Layer Route

4.2.3 Bottom Layer Route

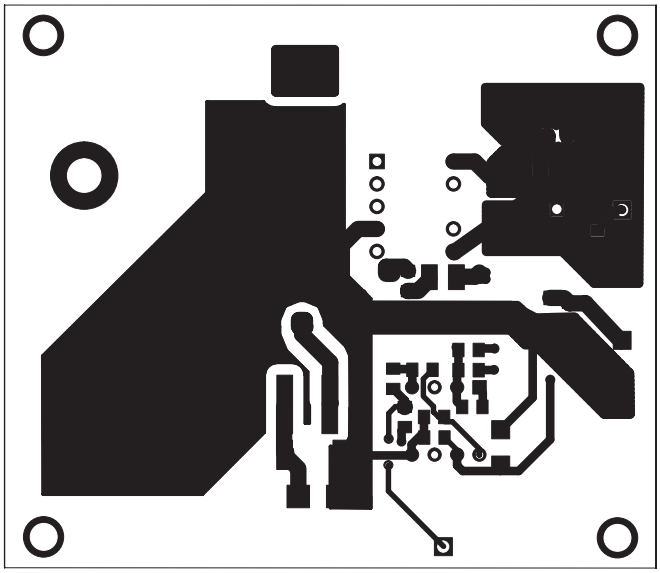

Figure 14. Botom Layer Route

4.2.4 Bottom Layer Component Placement

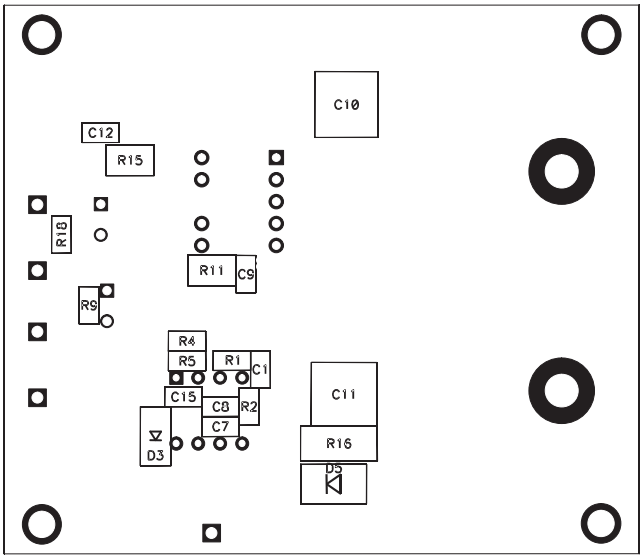

Figure 15. Bottom Layer Component Placement

5 References

1. Andreycak, William, *The UCC38C42 Family of High−Speed, BiCMOS Current Mode PWM Controllers*, Texas Instruments Literature No. SLUA257.
2. UCC28C40 BiCMOS Low-Power Current-Mode PWM Controller Data Sheet, Texas Instruments Literature No. SLUS458B

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