Texas Instruments

Application Report
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2.5-V to 5.0-V, 600-kHz High-Efficiency Synchronous Boost Converter With TPS43000 PWM Controller

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ABSTRACT

The application report describes the functionalities of the cTPS43000 controller and explains the design procedures of a step-up application from 2.5 V to 5.0 V.

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1 Introduction

The TPS43000 is a high-frequency, voltage-mode, synchronous PWM controller that can be flexibly used in buck, boost, buck-boost, and SEPIC topologies. This full-featured controller is designed to drive a pair of external MOSFETs (N/P) and can be used with a wide range of output voltages and power level. It can be widely used in networking equipment, servers, PDAs, cellular phones, and telecommunication applications.

A schematic of this board is shown in Figure 1. Recommended parts list is provided in Table 1. The layout of the PCB board is shown in Figure 7.

The specification for this board is as follows:

- V_{IN} = 2.5 V ±10%
- V_{OUT} = 5.0 V
- I_{OUT} = 0.2 A to 4 A, nominal current is 3 A and enters PFM at 1 A.
- Ripple = 1%
- Efficiency > 90%

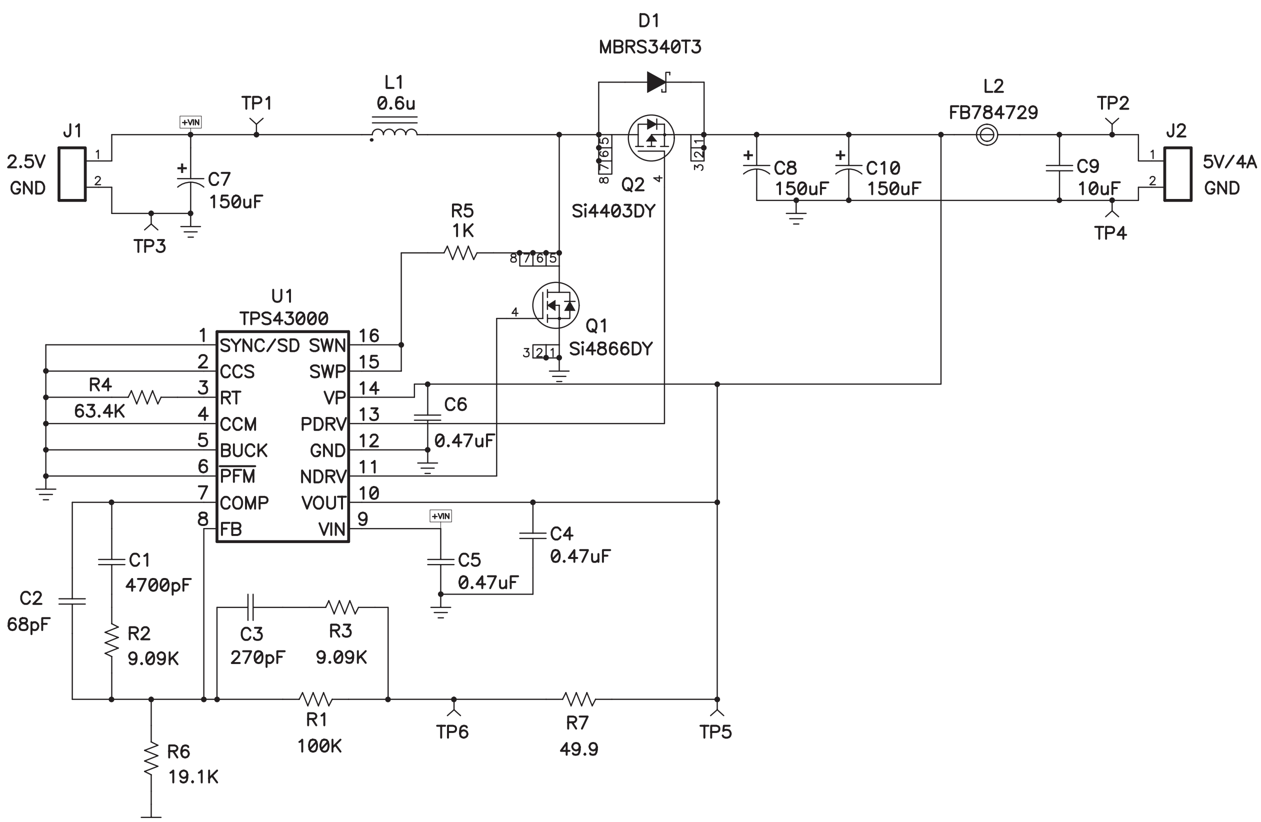

Figure 1. Schematic of PMP144

2 Design Procedure

2.1 Frequency Setting

The TPS43000 operates either in constant frequency, or in an automatic PFM mode. In the automatic PFM mode, the controller goes to sleep when the inductor current goes discontinuous, and wakes up when the output voltage has fallen by 2%. Refer to the TPS43000 datasheet (TI literature number SLUS489) for more detail. The PFM mode is used in this application. The converter operates at fixed 600 kHz above 1 A and enters into PFM at 1 A.

A resistor R4, which is connected from the RT pin to ground, programs the oscillator frequency. The approximate operating frequency is calculated in equation (1).

$$f\,(MHz) = \frac{38}{R4(k\Omega)} \tag{1}$$

R4 = 63.4 kΩ is chosen for 600 kHz operation.

2.2 Inductance Value

The inductance value is calculated in equation (2).

$$L_{MIN} = \frac{V_{OUT} \times D \times (1 - D)^2}{f \times 2 \times I_{OUT(\mathrm{min})}} \tag{2}$$

I_{RIPPLE} is the ripple current flowing through the inductor, which affects the output voltage ripple and core losses. Based on the requirement to enter PFM at 1 A and 600 kHz, the inductance value is calculated as 0.52 µH and a 0.6-µH inductor is used.

2.3 Input and Output Capacitors

The output capacitance and its ESR needed is calculated in equations (3) and (4).

$$C_{OUTPUT(\mathrm{min})} = \frac{I_{OUT(\mathrm{max})} \times D_{MAX}}{f \times V_{RIPPLE}} \tag{3}$$

$$ESR_{OUT} = \frac{V_{RIPPLE}}{\dfrac{I_{OUT(\mathrm{max})}}{1-D_{MAX}} + \dfrac{I_{IN(ripple)}}{2}} \tag{4}$$

With 1% output voltage ripple, the required capacitance is at least 73 µF and its ESR should be less than 5 mΩ. In order to meet the 1% output ripple requirement, at least four Panasonic 6.3-V/150-µF capacitors, whose ESR is 18 mΩ, are needed. Instead of using four expensive low-ESR capacitors, two capacitors (C8 and C9) are used and a second L-C filter (L2 and C10) is used to filter output voltage. The secondary L-C filter parameters are L2: FB784729 from GCI and C10 = 10 µF

The input capacitance is calculated in equation (5). The calculated value is about 65 μF and a 150-μF low-ESR specialty polymer, (SP), capacitor is used.

$$C_{IN(\min)} = I_{IN(ripple)} \times D_{MAX} \times \frac{T_S}{V_{IN(ripple)}} \qquad (5)$$

2.4 Compensation Design

For the boost converter, there is a right-half-plane (RHP) zero, which moves with operating conditions. The system phase starts to drop off a decade before this zero, limiting the system's bandwidth. In this circuit, the RHP zero is around 88 kHz. The L-C frequency of the power stage, f_C, is around 6.0 kHz and the ESR zero is around 70.7 kHz, as shown in Figure 2. The overall crossover frequency, f_{0db}, is chosen at 10 kHz for reasonable transient response and stability. R1 to R3 and C1 to C3 combine to form a Type III compensator network. Both zeros, f_{Z1} and f_{Z2}, from the compensator are set at 0.5 f_C to compensate the phase delay caused by RHP zero. The two poles $f_{P1 \text{ and }} f_{P2}$ and are set at ESR zero and half of switching frequency separately. The frequency of poles and zeros are defined by the following equations:

$$f_{Z1} = \frac{1}{2 \times \pi \times R2 \times C1}; \quad f_{Z2} \approx \frac{1}{2 \times \pi \times R1 \times C3}, \quad \text{assuming } R1 \gg R3 \qquad (6)$$

$$f_{P1} = \frac{1}{2 \times \pi \times R3 \times C3}; \quad f_{P2} \approx \frac{1}{2 \times \pi \times R2 \times C2}, \quad \text{assuming } C1 \gg C2 \qquad (7)$$

The compensator values are shown below:

C1 = 4700 F, C2 = 68 pF, C3 = 270 pF, R1 = 100 kΩ, R2 = 9.09 kΩ; R3 = 9.09 kΩ.

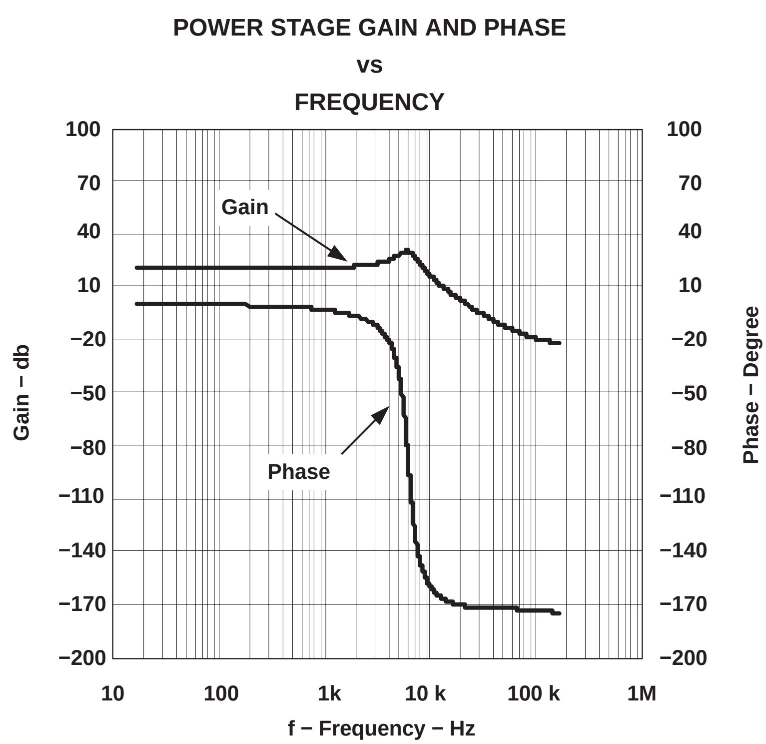

Figure 2.

2.5 MOSFETS and Diode

For a 5-V output voltage, the lower the $R_{DS(on)}$ of the MOSFET, the higher the efficiency. Si4486 ($R_{DS(on)}$ = 10 mΩ) and Si4403DV ($R_{DS(on)}$ = 20 mΩ) are chosen. MBRS340T3 is used for a parallel diode with Q2.

2.6 Voltage Sense Resistor

R1 and R6 operate as the output voltage divider. The internal reference voltage is 0.8 V. The relationship between the output voltage and divider is described in equation (8).

$$\frac{V_{REF}}{R6} = \frac{V_{OUT}}{R1 + R6} \qquad (8)$$

Setting resistor R1 to 100 kΩ using a value of 5.0-V output regulation, R6 is calculated as 19.1 kΩ.

3 Test Results

3.1 Efficiency Curves

Efficiency tested at different loads and input voltages are shown in Figure 3. The maximum efficiency is as high as 91.8% at light load. This comes from the PFM function and the losses from driving the gate are reduced significantly.

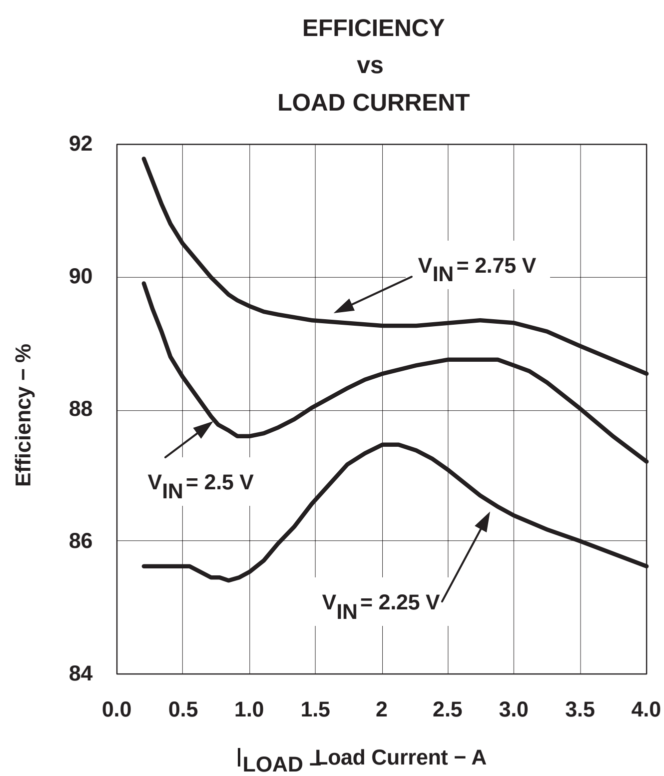

Figure 3.

3.2 Typical Operation Waveform

Typical operation waveform is shown in Figure 4 with V_{IN} = 2.5 and I_{OUT} = 3.0 A.

TYPICAL OPERATION

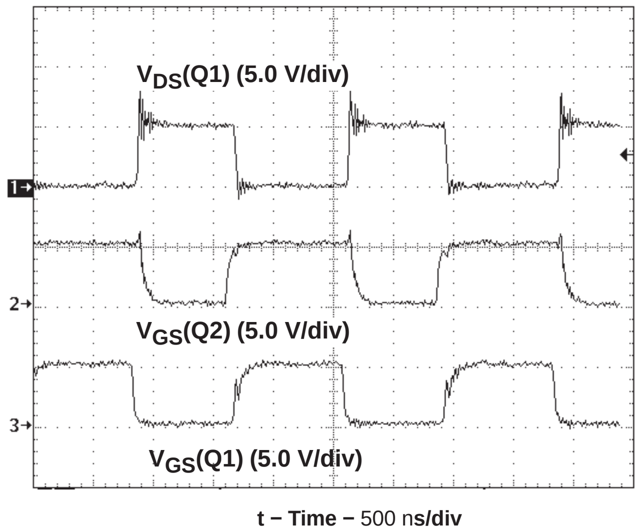

Figure 4.

3.3 Transient Response and Output Ripple Voltage

The output ripple is approximately 18.6 mV peak-to-peak with a 3.0-A output.

When the load changes from 2.4 A to 3.0 A, the overshooting voltage is approximately 76 mV.

OUTPUT RIPPLE

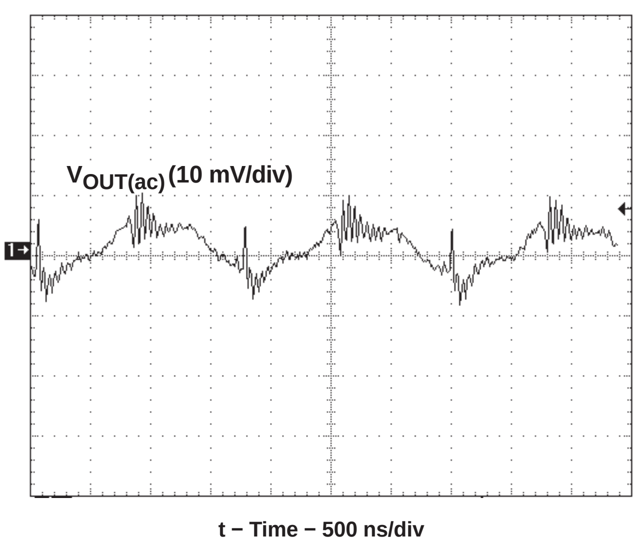

Figure 5.

TRANSIENT RESPONSE

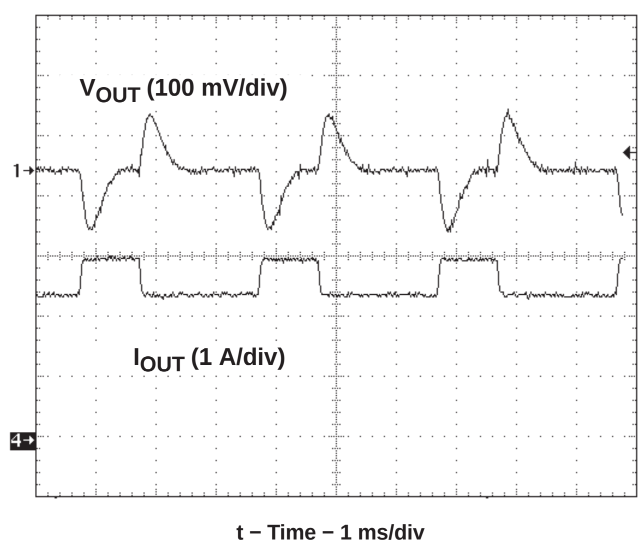

Figure 6.

4 PCB layout

Figures 7 and 8 show the PCB layout and the photo of a built-up board. All components are on the top side of the board. The bottom side of the board is the ground plane. The PWB is made large to dissipate the losses.

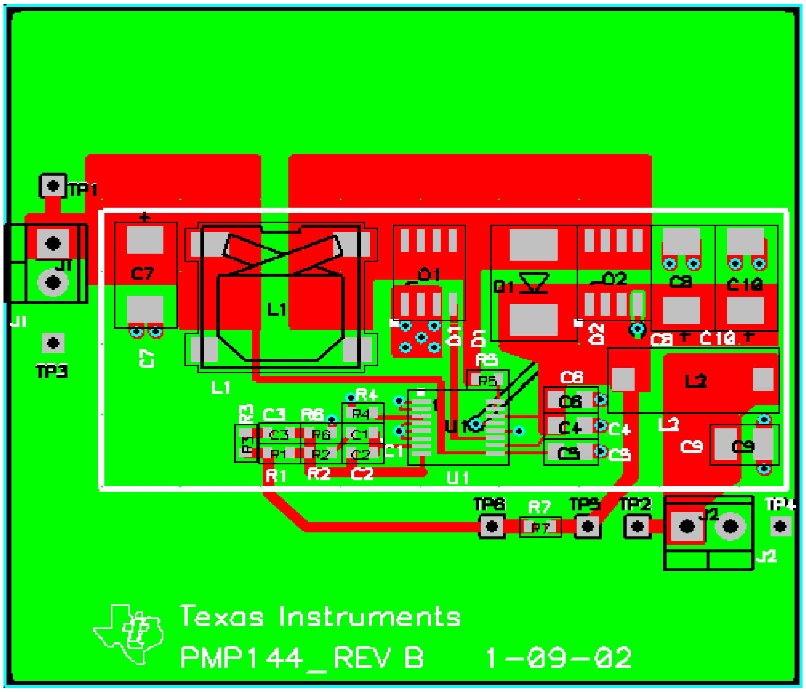

Figure 7. Top Side

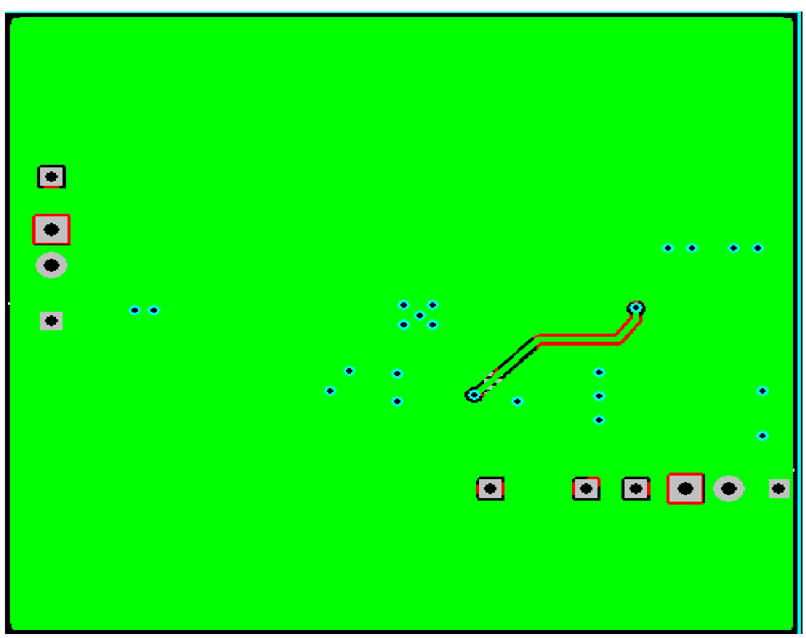

Figure 8. Bottom Side

5 List of Materials

Table 1 lists board components and their values, which can be modified to meet the application requirements.

Table 1. List of Materials

	Reference	Qty	Description	Manufacturer	Part Number
Capacitor	C1	1	Ceramic, 4.7 nF, 16 V, X7R, 10%, 603	Murata	GRM219R71C472K
	C2	1	Ceramic, 68 pF, 50 V, COG, 5%, 603	Murata	GRM1885C1H680J
	C3	1	Ceramic, 270 pF, 50 V, COG, 5%, 603	Murata	GRM1885C1H271J
	C4, C5, C6	3	Ceramic, 0.47 µF, 16 V, X7R, 10%, 805	Murata	GRM219R71C474K
	C9	2	Ceramic, 10 µF, 6.3 V, 20%, 1210	Taiyo−yuden	JMK325BJ106MM
	C7, C8, C10	3	150 µF, 6.3 V, 18 mΩ, 20%, 7343 (D)	Panasonic	EEFUE0J151R
Diode, Schottky	D1	1	3 A, 40 V, SMC	On Semiconductor	MBRS340
Terminal Block	J1, J2	2	2-pin, 6 A, 3.5 mm, 0.27 x 0.25””	OST	ED1514
Inductor	L1	1	SMT, 0.6 µH, 24 A, 6 mΩ, 13.5 mm x 6 mm	Sumida	CEP12D38−0R6
Ferrite	L2	1	Bead, 0.9 mΩ DCR, 48 Ω at 25 Mhz, 12.25 mm x 5 mm	GCI Technologies	FB784729
Resistor	R1	1	Chip, 100 kΩ, 1/16 W, 1%, 603	Std	Std
	R2, R3	2	Chip, 9.09 kΩ, 1/16 W, 1%, 603	Std	Std
	R4	1	Chip, 63.4 kΩ, 1/16 W, 1%, 603	Std	Std
	R5	1	Chip, 1.00 kΩ, 1/16 W, 1%, 603	Std	Std
	R6	1	Chip, 19.1 kΩ, 1/16 W, 1%, 603	Std	Std
	R7	1	Chip, 49.9 Ω, 1/16 W, 1%, 603	Std	Std
MOSFET	Q2	1	P-channel, 1.8 Vgs, 9 A, 17 mΩ, SO−8	Siliconix	Si4403DY
	Q1	1	N-channel, 2.5 Vgs, 17 A, 10 mΩ, SO−8	Siliconix	Si4866DY
IC	U1	1	Multi-topology high-frequency, PWM controller, TSSOP−16	Texas Instruments	TPS43000PW
Test Point	TP1, TP2, TP3, TP4, TP5, TP6	6	Black, 1mm, 0.038”	Farnell	240−333
PCB	N/A	1	FR4, 0.032, SMOBC	any	PMP144

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