

A HIGH PERFORMANCE LINEAR REGULATOR FOR LOW DROPOUT APPLICATIONS

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INTRODUCTION

Today's microprocessors are placing ever greater demands upon power system design. Most state of the art devices now require a 3.3V bus and therefore necessitate some means of stepping down the existing 5V system supply. To complicate matters further, microprocessor performance is directly related to the quality of the supply voltage. This results in the need for tight regulation and excellent transient response if the maximum potential of the processor is to be realized. Recently, the trend has been to implement the function using a switching regulator, primarily due to the high efficiencies obtainable with this topology. However, when the difference between input and output voltage is low, the efficiency advantage of the switcher is no longer as great. A linear regulator design, on the other hand, offers several desirable features including low output noise and wide bandwidth, resulting in excellent transient load response. This application note presents a high performance linear regulator design capable of maximizing the performance of these digital systems.

LINEAR VS SWITCHER

Figure 1 illustrates the basic elements of both a linear and switching stepdown regulator. In the linear topology, the output is regulated by controlling the voltage drop across a power transistor biased in the linear region. The switching circuit, on the other hand, provides regulation by varying the duty cycle of a saturated power switch. Although switchers offer a substantial efficiency advantage in applications with large differences between input and output voltage, the savings become less significant as this difference is reduced. To illustrate this point, consider the differences in a 3A, 5V to 3.3V converter design using the two topologies.

The power dissipation in the linear regulator is a function of the difference between input and output voltage, output current, output driver power, and quiescent controller power:

$$\text{Input/Output Voltage Drop} \quad (5.0-3.3V)(3A) = 5.1W$$

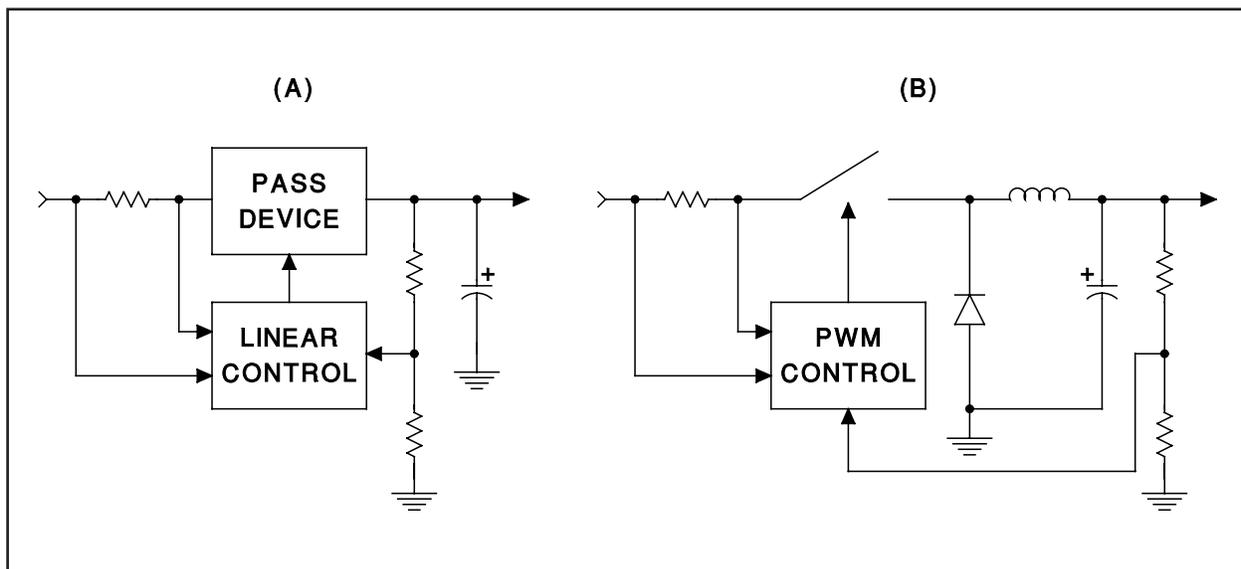


Figure 1. Basic elements of a A.) Linear and B.) Switching Regulator.

$$\begin{aligned} \text{Pass Device Driver} & (5.0V)(0.005A) = 0.03W \\ \text{Controller Icc} & (5.0V)(0.01A) = 0.05W \\ \text{Total} & = 5.18 W \end{aligned}$$

The resulting efficiency is equivalent to the ratio of output power to input power or $(3.3)(3)/((3.3)(3)+5.18) = 65.7\%$.

The efficiency of the switching regulator is not as simple to calculate. Power dissipated by the regulator is a combination of both conduction and switching losses in each of the circuit elements. Assuming an inexpensive, commercial power MOSFET with an $R_{ds(on)}$ of 0.28W, the duty cycle of the regulator is approximately:

$$\frac{t_{ON}}{t_{OFF}} = \frac{3.3}{(5 - 3)(0.28)} \approx 88\%$$

Taking duty cycle into account, the itemized circuit losses are estimated as follows:

$$\begin{aligned} \text{FET Conduction Losses} & (3A)^2(0.28\Omega)(80\%) = 2.02W \\ \text{FET Switching Losses} & (8.4E-9C)(5V)(250kHz) = 0.01W \\ \text{Diode Forward Voltage} & (0.6V)(3A)(20\%) = 0.36W \\ \text{Inductor Voltage} & (3A)^2(0.017\Omega)(100\%) = 0.15W \\ \text{RSENSE Voltage} & (3A)^2(0.043\Omega)(80\%) = 0.31W \\ \text{AC Capacitor Losses} & (0.15)^2(2.2\Omega) = 0.05W \\ \text{Controller Icc} & (5V)(1E-3A) = 0.01W \\ \text{Switching Transients} & \approx 0.10W \\ \text{Total} & = 3.01W \end{aligned}$$

Based upon these losses, the efficiency of the switching regulator is approximately $(3.3)(3)/((3.3)(3)+3.01) = 76.7\%$. These results indicate that the switching topology is approximately 11% more efficient in this application. However, the increase in efficiency doesn't come for free. The catch diode and inductor required in the switching topology increase the cost of the solution. In addition, due to the pulsed nature of the input current, the switching topology can generate considerable noise or electromagnetic interference (EMI), often requiring additional filtering to provide a compliant design. Differential current sensing and minimum load requirements further complicate the solution. Synchronous switching topologies and better components can improve the efficiency to better than 90%, but the number of components and cost of the solution increases even further.

The linear regulator, on the other hand, while slightly less efficient offers several attractive features. Low noise is inherent to the design due to the lack of fast switching circuits. Reduced component count coupled with a relatively simple design help to ensure system reliability and lower cost. Moreover, the linear solution does not have a minimum load restriction making it attractive in applications with widely varying load currents. The remainder of this application note provides the design details for a high performance linear regulator, taking advantage of each of these performance features.

TOPOLOGY OVERVIEW

Referring again to Figure 1, the linear design can be broken-down into several key elements including a pass device, driver, error amplifier, reference, output capacitance and over current protection block. The crux of the design arguably lies in the pass device. It's characteristics determine what the differential, input/output voltage limitations are in addition to how much quiescent power is required by the regulator. Error amplifier characteristics directly effect system bandwidth and the achievable DC regulation while the voltage reference primarily governs the steady state accuracy of the output voltage. Lastly, the overcurrent protection block protects the regulator during output fault conditions.

POWER PASS DEVICES

The power device selected to provide the pass function must be capable of operating under very low differential input/output voltages while still providing reasonable efficiency. Traditionally the PNP bipolar transistor has been applied in low dropout applications, primarily due to its low saturation voltage when compared to Darlington devices, and simpler base drive than an NPN configuration. Unfortunately, as the output requirements of the regulator grow, the gain of suitable PNP power transistors decreases, ultimately resulting in excessive base current losses. In addition, large amounts of base drive current often require more elaborate drive stages, further complicating the design. Consequently, the efficiency and advantages of the linear regulator are no longer as great.

Having eliminated bipolar configurations for either excessive drive current or dropout voltage, pass device options are limited to power MOSFETs. N-channel devices are most advantageous due to their low on-resistance and cost. Unfortunately, the gate drive difficulties associated with high side topologies make them less than ideal in applica-

tions operating from a single supply. P-channel MOSFETs, while easier to drive in high side applications, have historically been plagued with higher on-resistance. However, recent advancements in high cell density technology have led to substantial reductions in $R_{DS(on)}$. For instance, Motorola's new HDTMOS devices boast 50% lower on-resistance than the previous generation of P-channel devices. The MTP50P03HDL, a 50A, 30V, P-channel MOSFET is one such example, specified with a maximum on-resistance of 30m Ω at drain currents of 25A and a maximum gate threshold voltage of 2.0V. The logic level gate characteristics are required in applications limited to a supply voltage of 5 volts. An additional advantage of the MOSFET power stage is the minimum amount of drive current required. Since the device is voltage controlled and operating in transconductance mode it can be biased with minimal drive current, further improving the efficiency and decreasing the complexity of the regulator.

OUTPUT CAPACITANCE

Bulk output capacitance is required in order for the design to meet the specified transient requirements. As with any control system, the voltage loop has a finite bandwidth and cannot instantaneously respond to a change in load conditions. In order to keep the output voltage within the specified tolerance, sufficient capacitance must be provided to source the increased load current throughout the initial portion of the transient period. During this time, charge is removed from the capacitor and its voltage correspondingly decreases until the control loop can catch the error and correct for the increased current demand. The amount of capacitance used must be enough to keep the voltage drop within specification according to the charge relationship $I=CdV/dt$. Unfortunately, the equivalent series resistance (ESR) and inductance (ESL) of the capacitor generate an additional voltage transient, the total of which must be kept within specification. In order to limit this transient, the ESR and ESL of the selected devices will usually dictate a much larger value of capacitance than might normally be expected to satisfy the charge relationship.

OVERCURRENT PROTECTION

Traditional over current protection schemes usually involve either "constant current" or "current fold-back" techniques. Unfortunately, each of these solutions offers a compromise between the needs

of the user and the optimization of the power supply. Constant current techniques, while easy to interface with, result in massive overkill in terms of thermal management and heatsink implementation. Current foldback implementations, on the other hand, ease the design of the regulator while complicating startup scenarios for the user. Newer, switchmode protection techniques offer a solution to this compromise. By modulating the output at a fixed duty-cycle during an over current condition, thermal management of the regulator is greatly simplified. Adjusting the pulse width of the duty-cycle allows start-up load characteristics to be easily accommodated.

CONTROL CIRCUIT

In the design example that follows, the regulator is implemented using a UC3833, precision linear controller. This IC incorporates all of the functions required to design a very low dropout, precision regulator, including a 1% reference, error amplifier, and an uncommitted output stage. Providing an output driver with both source and sink capabilities allows the use of a variety of power devices including NPN or PNP bipolar devices and N or P-channel MOSFETs. Switchmode current limiting is also implemented by the UC3833, significantly reducing power dissipation during fault conditions. Further information regarding this device can be found in Unitrode application note U-116.

DESIGN DETAILS

The regulator was designed to meet the following performance requirements, typical of today's microprocessor systems. The schematic is shown in Figure 2.

$$V_{IN} = 5V, \pm 10\%$$

$$V_{OUT} = 3.3V, \pm 5\%$$

$$I_{OUT} = 3.5A \text{ typical, } 4A \text{ maximum}$$

$$\text{Transient Response: } 5\% \text{ to } 75\% I_{OUTmax} \text{ in } 100\text{nsec, } V_{reg} = \pm 5\%$$

In order to select a pass device for the design, the dropout voltage requirements must first be established. Input voltage tolerance, along with the voltage drop across the current sense resistor, must be taken into account. The sense resistor value is calculated based on the maximum output current specification of the regulator and the current limit threshold of the UC3633. In order to ensure the regulator can deliver 4A under worst case conditions, the maximum resistor value, including tolerance, is given by:

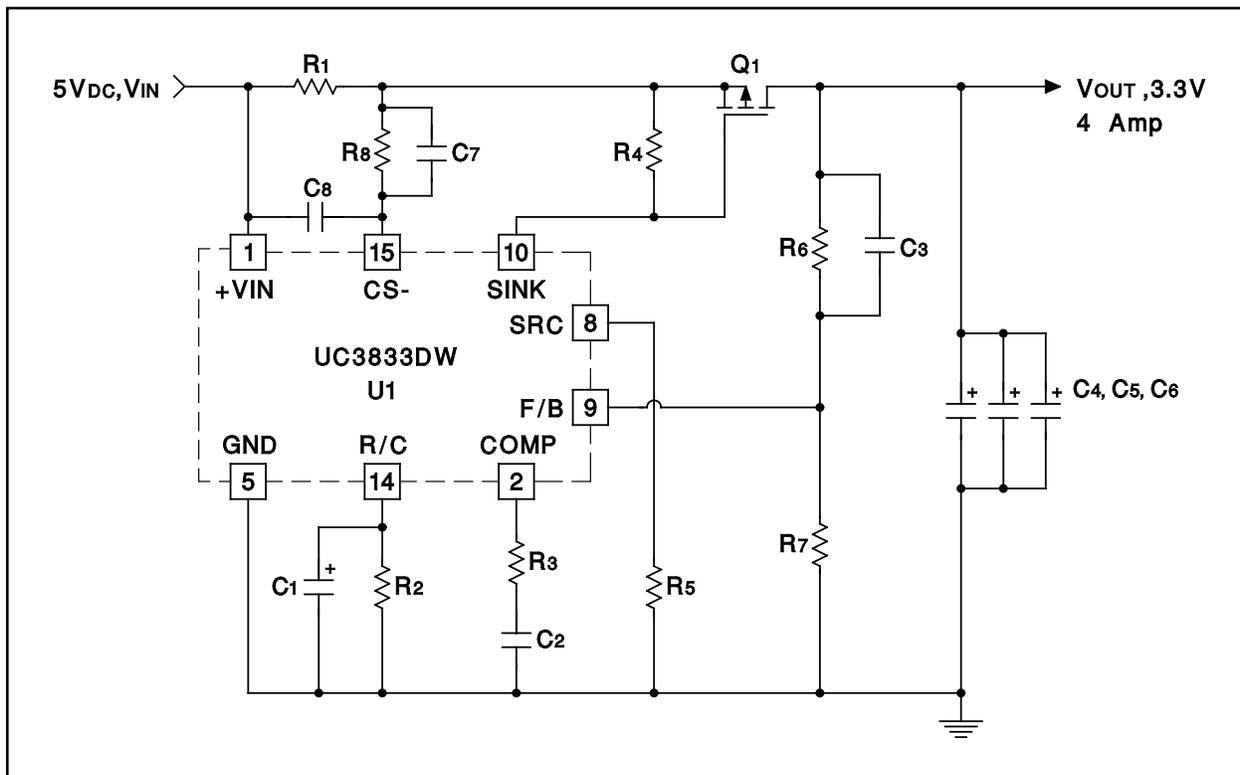


Figure 2: A 3.3V, 4A regulator featuring low dropout voltage, switchmode overcurrent protection and excellent transient response.

$$R_{MAX} = \frac{V_{CLmin}}{I_{OUT}} \quad (1)$$

$$R_{MAX} = \frac{0.093}{4} = 23.25m\Omega$$

Using a 5%, 22m Ω sense resistor and low line conditions, the dropout requirement for the pass device is calculated as follows:

$$V_{DO} = V_{INmin} - I_{OUTmax}(R_{SENSEmax}) - V_{OUT} \quad (2)$$

$$V_{DO} = 4.5 - 4(1.05)(0.022) - 3.3 = 1.29V$$

This dropout voltage results in a maximum MOSFET $R_{DS(on)}$ of 0.323 Ω . In addition, logic level gate characteristics are required in order to ensure adequate gate enhancement with a 5 volt input. These requirements are easily met with the MTP50P03HDL's 30m Ω ($T_C=25^\circ C$) on-resistance and 2.0V maximum gate threshold voltage.

Having selected the pass device, the UC3833 output driver can now be configured. While the simplest approach would be to configure the driver as a common emitter, including a small amount of emitter resistance eliminates the drive transistor's β from the loop gain expression, thereby simplifying

the frequency compensation. Resistors R6 and R7 attenuate and feedback the output voltage to the inverting input of the error amplifier.

Sprague 595D surface mount tantalum capacitors were chosen for the output based upon their ESR/ESL specifications and package style. By paralleling three 270 μF , 10V capacitors, the equivalent ESR/ESL is reduced by 1/3, providing an equivalent impedance of approximately 13m Ω typical and 60m Ω maximum at 100kHz. Surface mount packaging helps to further reduce the parasitic effects induced by component leads. The equivalent 810 μF provides more than sufficient capacitance to keep the transient voltage drop within specification.

SMALL SIGNAL AC RESPONSE

With the driver and power stage configured, the voltage and current control loops can now be analyzed and properly compensated. Figure 3 illustrates the basic configuration of the two loops. The frequency response of the MOSFET driver includes a gain factor of R_4/R_5 with a pole introduced from the combination of the MOSFET's gate to source capacitance and R4. The transconductance of the MOSFET is represented by g_{FS} . Modeling the load as a resistance in parallel with

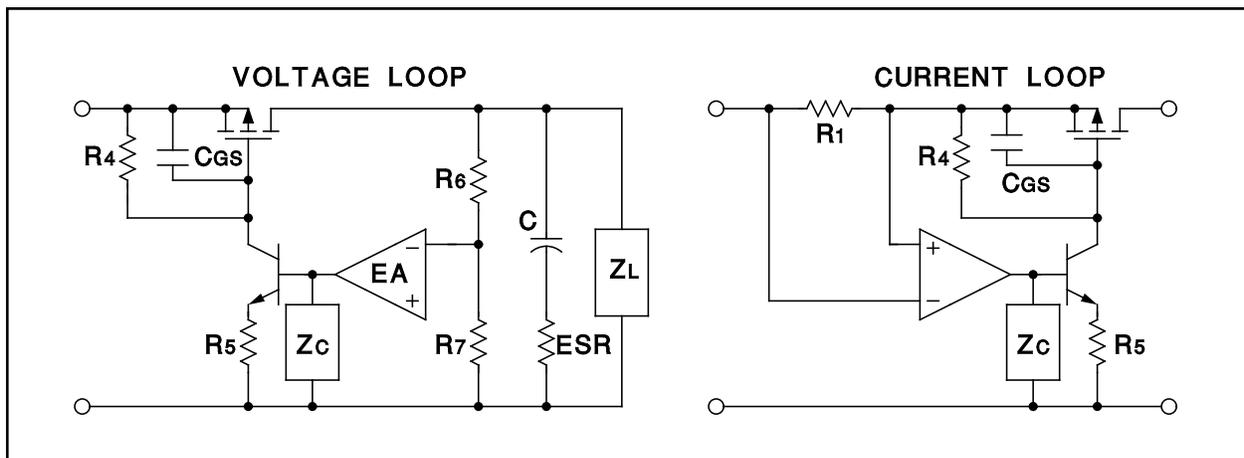


Figure 3. Basic configuration of the voltage and current control loops.

the output capacitor and its associated ESR results in a loop gain expression, excluding the error amplifier, of:

$$A_v = \left(\frac{R_4}{R_5(1 + sR_4C_{GS})} \right) \cdot \left(g_{FS} \left(\frac{R_L(1 + s(ESR)C)}{1 + s(R_L + ESR)C} \right) \right) \left(\frac{R_7}{R_6 + R_7} \right) \quad (3)$$

The dashed curves of Figure 4a represent the resulting voltage loop response. Although the response is stable, the low frequency gain and closed loop accuracy are limited. This is easily improved by compensating the UC3633's error amplifier using a series RC network. Doing so introduces a pole at 0Hz, thereby improving the DC regulation, in addition to a zero at $1/(2\pi RC)$ Hz. The zero is located between the poles resulting from the load and the MOSFET gate to source capacitance. Together with the ESR zero, they provide enough phase boost to maintain adequate phase margin. Adding a capacitor across R6 helps to squeeze additional bandwidth from the loop by introducing another pole/zero pair. The gain and phase of the compensated voltage loop (solid lines) are also shown in Figure 4a.

Having stabilized the voltage loop, the current loop can now be examined. The established compensation impedance must be taken into account as both the current and error amplifier share a common output node. The complete current loop expression, including the transconductance (g_m) of the current amplifier, is given below:

$$A_i = \left(\frac{R_4}{R_5(1 + sR_4C_{GS})} \right) \cdot \left(g_{FS} R_1 \right) \left(\frac{g_m(1 + sR_3C_2)}{sC_2} \right) \quad (4)$$

The corresponding response is shown in Figure 4b. From this plot, it is evident the loop lacks sufficient phase margin to be stable under all conditions. Filtering the current signal with the network composed of R8, C7 and C8, as shown in Figure 2, introduces a pole and zero according to the following transfer function, rolling off the current loop gain without effecting the voltage loop. The gain and phase of the compensated current loop (solid lines) are also shown in Figure 4b.

$$\frac{V_o(s)}{V_i(s)} = \frac{(1 + sR_8C_7)}{(1 + sR_8(C_7 + C_8))} \quad (5)$$

When performing small signal analysis such as this, the use of a spreadsheet program can prove invaluable. The software can be easily configured to provide Bode plots using pole and zero locations input by the user. The graphical output allows the user to quickly evaluate a variety of compensation techniques and relatively easily optimize the design.

OVERCURRENT PROTECTION AND THERMAL MANAGEMENT

Overcurrent protection is provided via the UC3833's internal amplifier and overcurrent comparator. When the voltage across R1 crosses the comparator threshold the UC3833 begins to modulate the output driver. During the on-time the current sense amplifier provides constant output current by maintaining a fixed voltage across R1. On and off times are controlled by timing components C1 and R2 according to the following expressions:

$$T_{ON} = 0.693(10k)(C_T) \quad (6)$$

$$T_{OFF} = 0.693(R_T)(C_T) \quad (7)$$

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{10k}{10k + R_T} \quad (8)$$

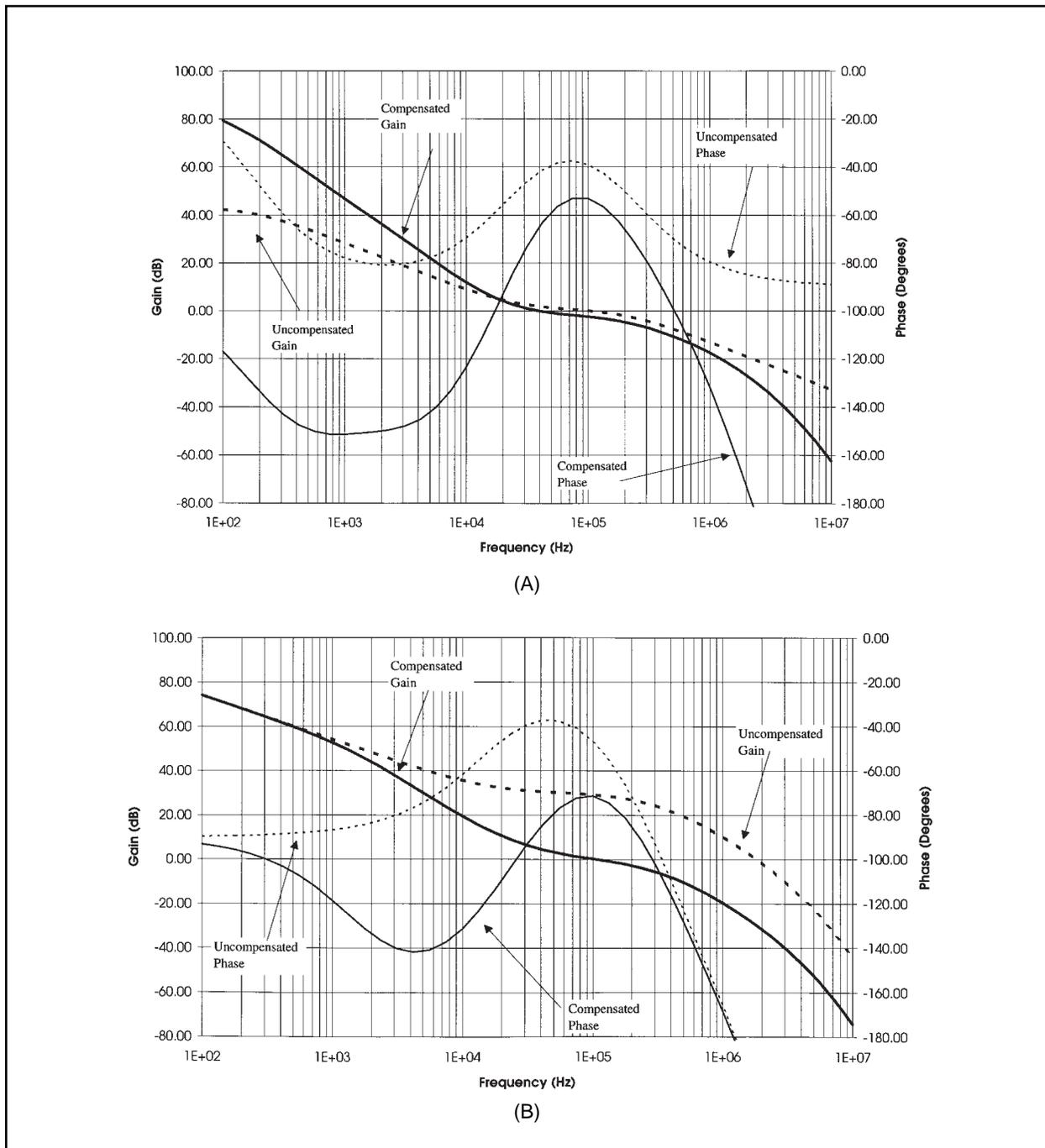


Figure 4: Uncompensated and compensated open loop responses for the circuit of Figure 2. (A) Voltage Loop, (B) Current Loop.

When implementing switchmode protection, the “on” time (T_{ON}) must be of sufficient duration to charge the output capacitance during a normal startup sequence or when recovering from a fault. If not, the charge accumulated on the output capacitor will be depleted by the load during the “off” time. The cycle will then repeat, preventing the output from turning on. A maximum load current of just less than the trip limit results in the difference between the I_{MAX} and I_{TRIP} values as the

current available to charge the output capacitance. In this case the minimum “on” time can be calculated as follows:

$$T_{ONmin} = \frac{C_{OUTmax} \cdot V_{OUT}}{I_{MAX} - I_{TRIP}} \tag{9}$$

The duty cycle can then be adjusted to minimize power dissipation using equation (8).

Switchmode protection offers significant heat sinking advantages when compared to conventional, constant current solutions. Since the average power during a fault condition is reduced as a function of the duty cycle, the heat sink need only have adequate thermal mass to absorb the maximum steady state power dissipation and not the full short circuit power. With a 5.5 volt input and a maximum output of 4A, the power dissipated in Q1 is given by:

$$P = (V_{IN} - V_{RSENSE} - V_{OUT})(I_{OUT}) \quad (10)$$

$$P = (5.5 - 4(0.022)(0.95) - 3.3)4 = 8.47W$$

The thermal resistivity of the MOSFET is specified as 1.0°C/W for the TO-220 package style. Assuming an ambient temperature of 50°C and a case to heat sink resistivity of $\theta_{CS}=0.3^\circ\text{C/W}$, the heat sink required to maintain a 125°C junction temperature can be calculated as follows:

$$T_J = T_A + P(\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad (11)$$

$$25 = 50 + 8.47(1.0 + 0.3 + \theta_{SA})$$

$$\theta_{SA} \leq 7.55^\circ\text{C/W}$$

Based on this analysis, any heatsink with a thermal resistivity of 7.55°C/W or less should suffice. Under short circuit conditions the output current will be limited to 6.14A at a 5% duty cycle, resulting in a MOSFET power dissipation of only:

$$P = ((V_{INmax} - (I_{OUT})(R_{SENSE}))I_{OUT})(d.c.) \quad (12)$$

$$P = ((5.5 - 6.14(0.022))6.14)0.05 = 1.65W$$

Without switchmode protection, the short circuit power dissipation would be 33W, almost four times the nominal dissipation!

PRACTICAL CONSIDERATIONS

In order to achieve the expected performance, careful attention must be paid to circuit layout. The printed circuit board should be designed using a single point ground, referenced to the return of the output capacitor. All traces carrying high current should be made as short and wide as possible in order to minimize parasitic resistance and inductance effects.

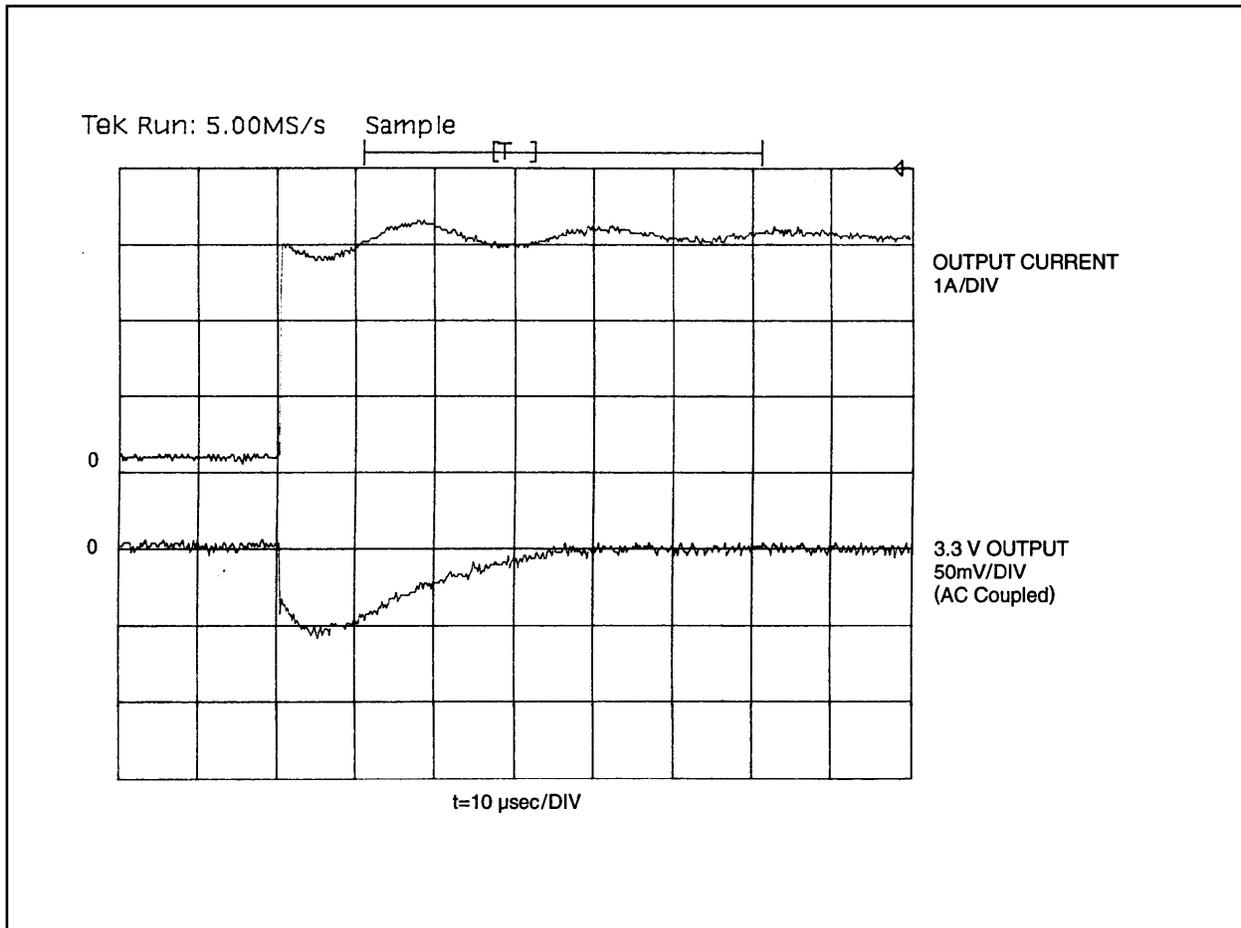


Figure 5: Transient response of the regulator illustrated in Figure 2 with a time base of 10 μsec.

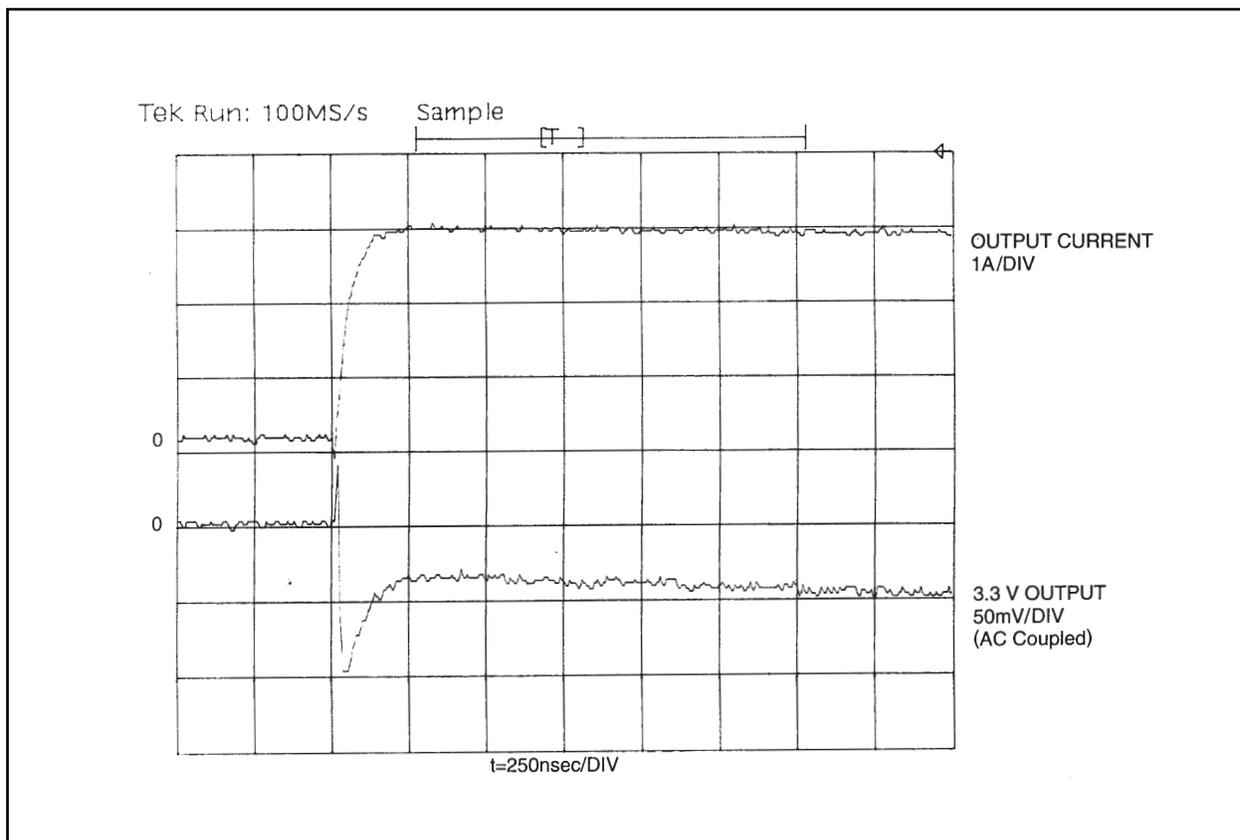


Figure 6: Transient response of the regulator illustrated in Figure 2 with a timebase of 250 nsec.

To illustrate the importance of these concepts, consider the effects of a 1.5" PCB trace located between the output capacitor and the UC3833 feedback reference. A 0.07" wide trace of 1oz. copper results in an equivalent resistance of 10.4m Ω . At a load current of 3A, 31.2mV is dropped across the trace, contributing almost 1% error to the DC regulation!! Likewise, the inductance of the trace is approximately 3.24nH, resulting in a 91mV spike during the 100nsecs it takes the load current to slew from 200mA to 3A.

PERFORMANCE

The efficiency of the regulator is 65.7% in a typical application with 3A of output current and a 5.0V input. Under maximum load and worst case conditions, the efficiency drops to 60%. During a short circuit scenario the regulator limits the peak current to approximately 6A. At the 5% duty cycle set by C1 and R2, the average current is 300mA, resulting in less than 2W of power dissipated in the MOSFET!

The design provides a worst case DC regulation of $\pm 3\%$ using the UC3833 in conjunction with 1% feedback resistors. If even tighter tolerance is required, the UC3832 can be substituted along

with 0.1% resistors. The UC3832 has provisions for an external voltage reference allowing increased performance over the UC3833's $\pm 1\%$ internal reference.

The AC characteristics of the voltage loop determine how fast the regulator can respond to sudden load disturbances. Figure 5 illustrates how the design behaves during the specified 100nsec transient. Starting with 200mA of load current, a step change to 3A was applied to the regulator. This load current waveform is shown in the upper trace of Figure 5. Notice that in the lower trace, following the increase in load, the output drops approximately 50mV and then recovers to a stable state within 40 μ sec. Figure 6 shows the same response with the timebase expanded to 250nsec. In this plot, the initial transient resulting from the equivalent impedance of the output capacitor is clearly visible. The parallel combination of the three output capacitors and careful layout limits the transient to roughly 100mV.

SUMMARY

The circuit described in this application note was specifically designed to meet the demanding performance requirements of today's

V _{OUT}	I _o	R ₆	R ₁	C _{OUT}	θ _{SAmax}	Applications
3.0V	3A	1k	0.03	810μF	9.06°C/W	D/A converters, Gate Arrays
	5A	1k	0.0169	1320μF	4.91°C/W	
	7A	1k	0.012	1980μF	3.13°C/W	
2.7V	3A	698	0.03	810μF	7.9°C/W	MCUs
	5A	698	0.0169	1320μF	4.22°C/W	
	7A	698	0.012	1980μF	3.64°C/W	
2.5V	3A	499	0.03	810μF	7.28°C/W	Low voltage digital logic
	5A	499	0.0169	1320μF	3.84°C/W	

Notes: 1. Thermal resistivities assume 50°C ambient and max T_J of 125°C.
2. C_{OUT} is comprised of multiple Sprague 595 style tantalum capacitors.

microprocessors. It is capable of providing excellent transient response with reasonable efficiency for less cost and complexity than a switching regulator. The design is easily modified to accommodate other output voltage and current requirements. Table I provides the necessary component substitutions to achieve a variety of the more popular output voltages and their typical applications. The same MTP50P03HDL MOSFET is used for all designs.

Output voltages below 2.0V dictate the use of a UC3832. The UC3832 enables the user to set the error amplifier voltage reference below 2.0V. In the UC3833 the noninverting error amplifier input is internally committed to 2.0V. For additional information regarding the UC3832/3 linear controllers, consult Unitrode application note U-116.

Additional information on HDTMOS MOSFETs and low impedance capacitors is available from Motorola (602-244-3377) and Sprague (603-224-1961) respectfully.

REFERENCES

- [1] "Versatile UC1834 Optimizes Linear Regulator Efficiency", Application Note U-95, Unitrode Integrated Circuits, Merrimack, NH,1993-94.
- [2] Mammano, R., Radovsky, J. and Harlan, G. "A New Linear Regulator Features Switch Mode Overcurrent Protection", Application Note U-116, Unitrode Integrated Circuits, Merrimack, NH,1993-94.

PARTS LIST:

Resistors	Capacitors	Transistors	Integrated Circuits
R1 = 0.022Ω	C1, C8 = 1μF	Q1 = MTP50P03HDL	U1 = UC3833
R2 = 200k	C2, C3 = 0.1μF		
R3, R8 = 100Ω	C4, C5, C6 = 270μF		
R4 = 300Ω	C7 = 33000pF		
R5 = 20Ω			
R6 = 1.3k			
R7 = 2.0k			

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