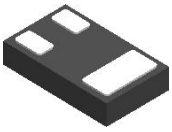
FemtoFET™ Surface Mount Guide

Texas Instrument (TI) is facilitating the electronics industry's drive towards smaller packaging outline technologies with the FemtoFET™ series of packages. The FemtoFET™ is a Land Grid Array (LGA) package, which is a silicon Chip Scale Package with metallized pads instead of solder balls. This document describes the Surface Mount Technology (SMT) issues to be considered when attaching these parts to printed circuit boards.

The FemtoFET™ package series is targeted toward handheld and mobile applications where small form factor, space, and weight limitations are essential. This technology is capable of replacing standard small signal MOSFETs, providing a 70% reduction in footprint size. For more information, visit: **www.ti.com**

F3(YJM)

F4(YJC)



F4 (YJJ)

F5(YJK)

Device Name Suffix	F3	F4	F4	F5
Package Designator	YJM	YJC	YJJ	YJK
Package Width (W)*	0.60	0.60	0.60	0.73
Package Length (L)*	0.69	1.00	1.00	1.49
Package Thickness (Max)	0.35	0.35	0.20	0.35

* Nominal dimensions shown. All measurements in mm. For additional information, see package designator at www.ti.com

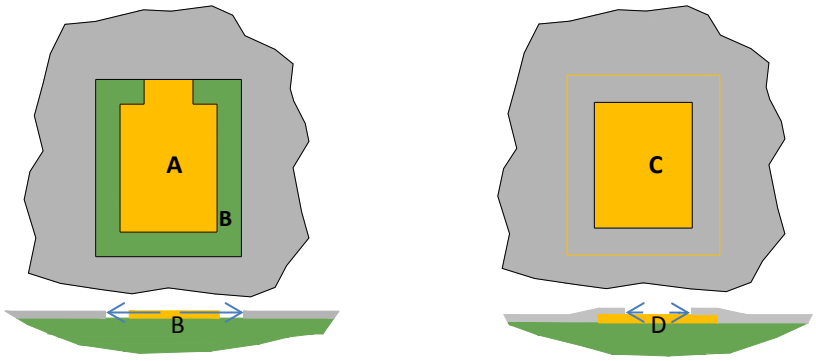
Operation	Assembly Quick Start Checklist
Solder Paste	TI recommends the use of type 3 or finer solder paste when mounting the FemtoFET™ devices. Either no-clean or water-soluble solder paste is acceptable.
	TI recommends inspection of solder paste printing quality by SPI (solder paste inspection) machine.
Reflow Profile	Measure the peak reflow temperature by placing a fine gauge thermocouple (Type K) on top of the package body center.
	Ensure that the peak reflow temperature does not exceed 260°C max. (260°C +0/- 5°C) Exceeding the max temperature may damage the part.
	Reflow time within 5°C Peak Temp must not exceed 20 seconds and the reflow time above liquidus must not exceed 60 seconds.
	Minimizing the number of reflow cycles seen by the FemtoFET™ devices is recommended.
Moisture Handling	FemtoFET™ products are classified as MSL1 and require no special handling due to moisture sensitivity. MSL1 parts are not limited by max floor exposure.
	See IPC/JEDEC J-STD-033 for additional details.

PCB Design Guidelines

SMD (Solder Mask Defined) pads are preferred over NSMD (Non Solder Mask Defined) pads to avoid issues due to solder mask registration error when surface mounting FemtoFET™.

If NSMD configuration has to be used, the following precautions are recommended:

1. A copper layer thickness of less than 1 oz is recommended to achieve higher solder joint stand-off. A 1 oz. (30 micron) or greater copper thickness causes a lower effective solder joint stand-off, which may compromise solder joint reliability.
2. The trace width at the connection to the land pad should not exceed 2/3 of the pad diameter.
3. Control the solder mask shift on the PCB to avoid inconsistent pad size.



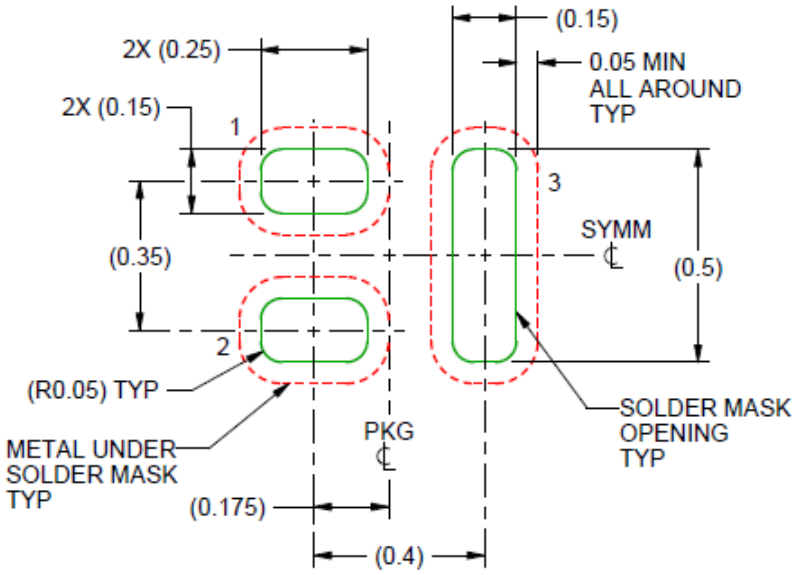
Non-Solder Mask Defined Pad (NSMD) Not-Preferred		Solder Mask Defined Pad (SMD) Preferred	
Copper Pad	Solder Mask Opening	Copper Pad	Solder Mask Opening
"A"	"B"	"C"	"D"

Stencil Vitals

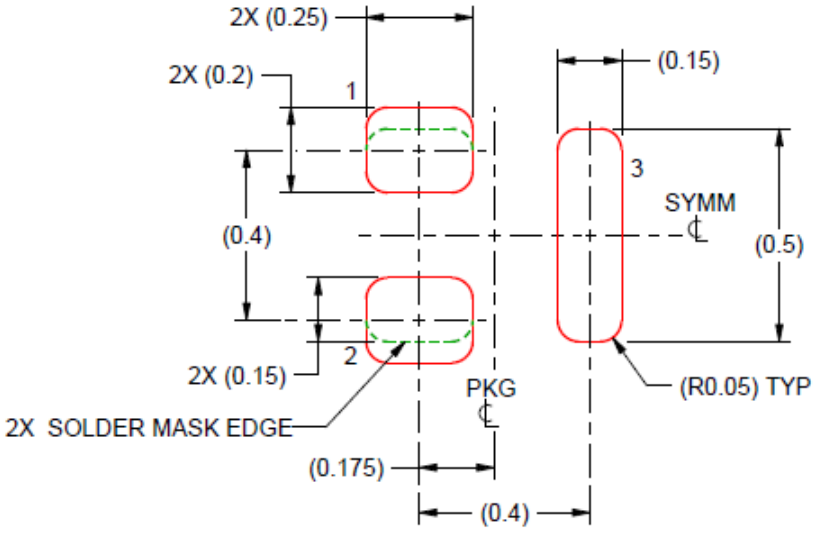
TI recommends stencil manufacturing by either laser cut / electro polished or electroform with tapered aperture walls with a 5 degree tapper to facilitate paste release.

To improve solder paste transfer efficiency, TI recommends to enlarge the stencil opening and offset it outward to maintain the same separation between pins 1 and 2 for F3 and F4 (pin 1 and 3 for F5).

F3 (YJM) Package: Land pattern and stencil recommendation

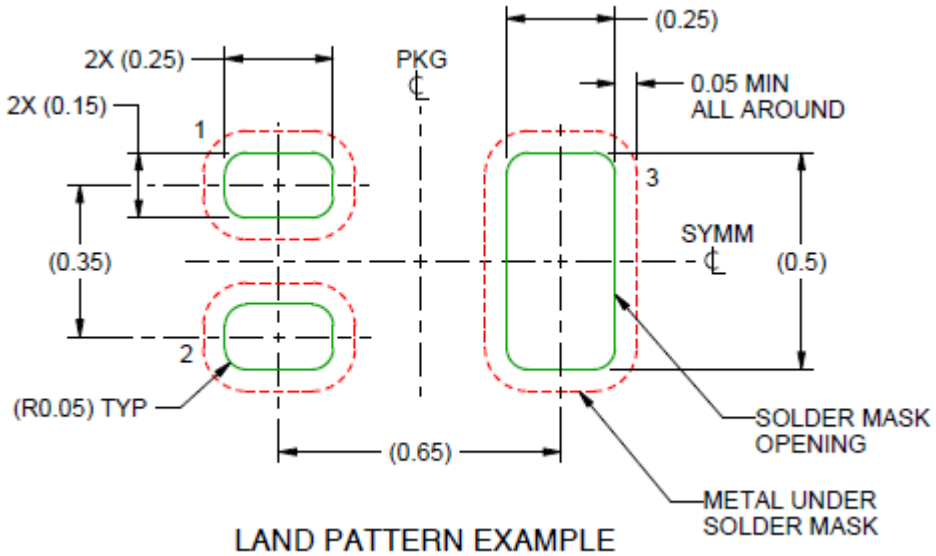


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

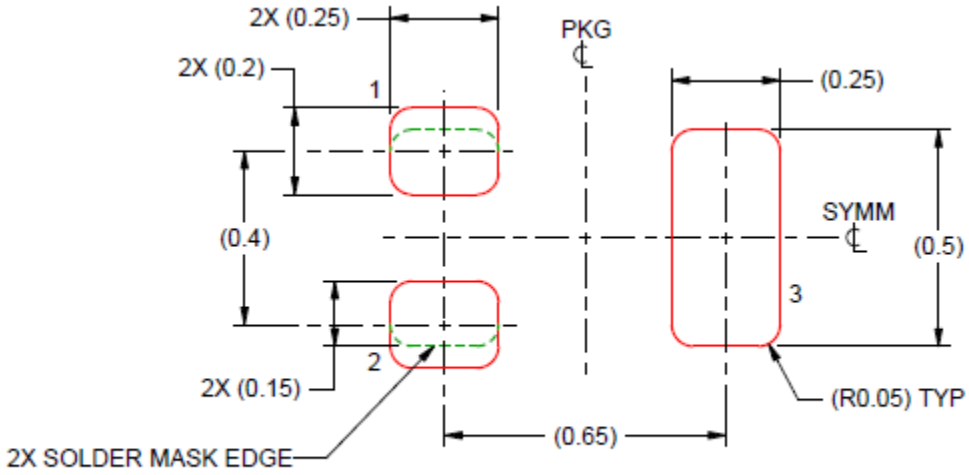


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL

F4 (YJC/YJJ) Package: Land pattern and stencil recommendation

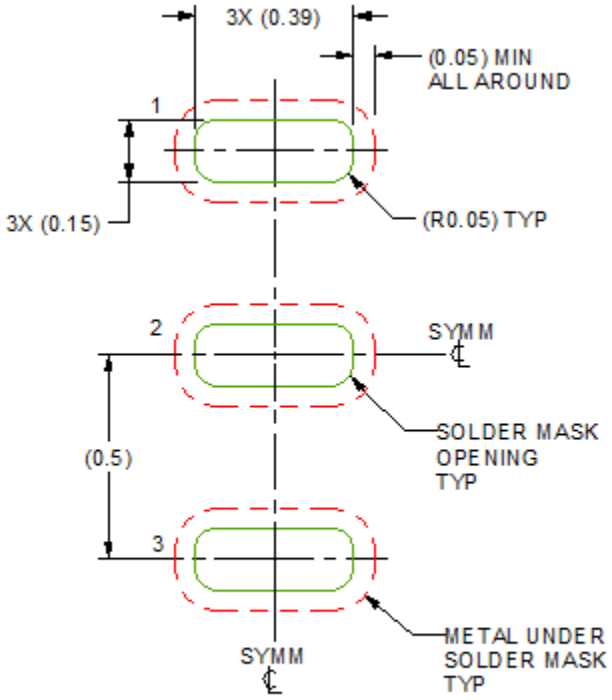


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

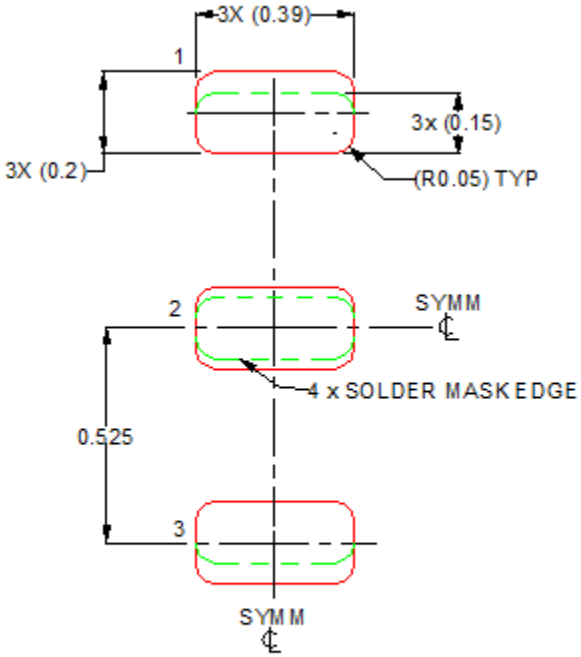


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL

F5 (YJK) Package: Land pattern and stencil recommendation



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL

Summary of stencil opening

TI recommends stencil thickness of 75 µm which gives an optimum area ratio larger than 0.61, see table below for detail information.

for stencil thickness = 0.075 All dimensions in mm

	pin 1			pin 2			pin 3		
Package	W	L	Area ratio	W	L	Area ratio	W	L	Area ratio
F3 (YJM)	0.2	0.25	0.74	0.2	0.25	0.74	0.15	0.5	0.77
F4 (YJC/YJJ)	0.2	0.25	0.74	0.2	0.25	0.74	0.25	0.5	1.11
F5 (YJK)	0.2	0.39	0.88	0.2	0.39	0.88	0.2	0.39	0.88

Solder Paste

TI recommends the use of type 3 or finer solder paste when mounting FemtoFET™. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the package to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimal joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the “no clean” compositions are preferred due to the difficulty in cleaning under the mounted components.

The FemtoFET™ series packages do not require underfill.

Package Placement

TI recommends a pick and place nozzle size of 0.4mm in placement of the FemtoFET™ package. If placement method is by programming the component thickness, add 0.05mm to the actual component thickness so that the package will be sitting halfway into paste. Use a nozzle with a soft rubber tip rather than a hard tip to minimize damage to the device during the component mounting process. If placement is by force feedback, then utilize minimum force while not exceeding 3 Newton's of force. This control is to avoid forcing out solder paste or package free fall resulting in solder balling.

Package Repair Guidelines

Repair Procedure

A package repair/rework station is strongly recommended for this process. (i.e. Air-Vac Engineering, Metcal, or Den-On Inst.)

Package Replacement Procedure:

- Board preheat (package bake recommended)
- Reflow of component solder
- Vacuum removal of component
- Cleaning and preparation of PWB lands
- Screening of solder paste (If possible, a mini stencil is recommended)
- Placement and reflow of new component
- Inspection of solder joints

Repair Procedure Notes:

- Prior to any rework process, it is recommended to bake the board 4 hours at 125C to remove any moisture that might cause delamination or cracking.

- Reuse of a removed package is not recommended.

- Use a new package for the repair process. The new package should be kept dry and should not exceed stated floor life. Only re-bake a package a maximum of 3 times.

Mechanical Stress Test Results

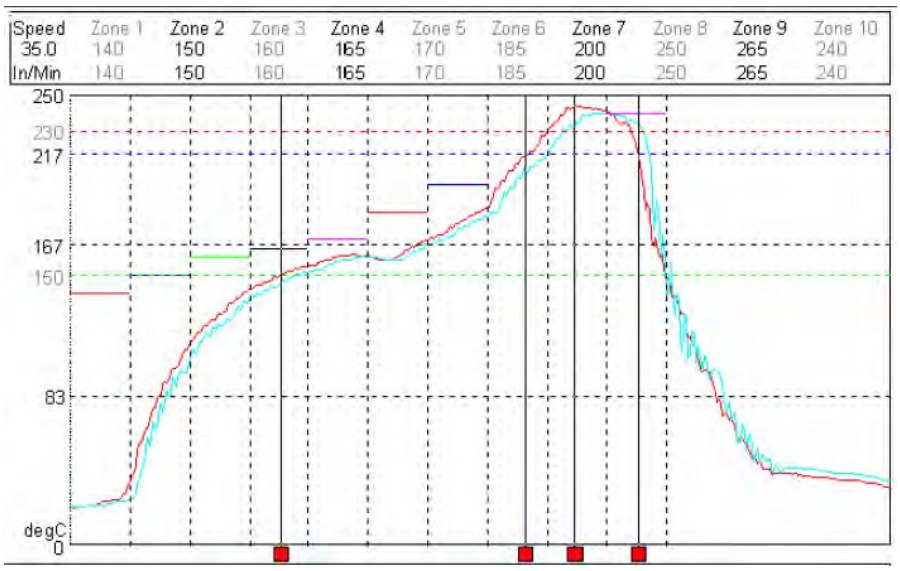
- Shear Test > 1kgf
- Monotonic Bend Test (JEDEC-9702) displacement of 30 mm without failure
- Cyclic Bend Test (JESD22B113) displacement of 3 mm up to 10,000 cycles without failure
- Board Level Drop Test (JESD2-B111) more than 600 drops without failure

IR Reflow Profiles

Customers should consider their solder manufacturer recommended reflow profile as optimal source for their specific application. Actual temperature profile depends on various factors such as board size, board thickness, component density and solder paste etc. The FemtoFet™ package is compatible with lead and lead-free pastes.

Ramp Rate	3°C/sec. Max.
Preheat	150 to 180°C
	60 to 120 sec.
Time Above Liquidus	220°C
	30 to 90 sec.
Peak Temp.	260°C +0/-5°C
Time Within 5°C Peak Temp.	10 to 20 sec.
Ramp Down Rate	6°C/sec. Max.

Example Pb Free Reflow Profile



Temperature profile above is JEDEC Pb Free reflow compliant and shown as example only,

Questions & Answers

Q. Is package rework possible? Are tools available?
A. Yes, rework is possible, and there are several semi-automatic SMT rework machines and profiles available. However, TI does not guarantee the reliability of re-used packages. It is best to discard and replace any package that fails test. Please refer to the repair guideline section of this document for more details.

Q. What size land diameter for these packages should I design on my board?
A. Land size is the key to board-level reliability, and Texas Instruments strongly recommends following the design rules included within this summary.

Q. Can customers mount FemtoFet™ packages on the bottom side of the PCB board?
A. Yes, they can and the ideal 2nd reflow profile is the same as the 1st.

Q. Can the solder joints be inspected after reflow?
A. Many customers are achieving satisfactory results during process setup using X-ray techniques.

Q. Are there pressure requirements for mounting FemtoFet™ packages?
A. TI recommends controlling the placement pressure in mounting the FemtoFET™ package. The mounting force should not exceed 3N.

Q. Has TI developed a lead-free version of FemtoFet™ ?
A. Yes, Texas Instruments has developed the FemtoFet™ series as a Pb-Free option in order to comply with lead-free environmental policies.

Q: What routing choices do I have when using FemtoFet™ packages?
A: The pad design is wide enough to allow for via-in-pad routing techniques to be employed on an economical basis.

Q. Any EMI concerns for traces under the package and how can customers design their board to minimize EMI?
A. EMI can be controlled by minimizing any complex current loops on the PCB trace. Some helpful hints include:

- Solid ground and power planes can be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops increasing radiation.
- Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance causing signal degradation.
- Minimize power supply loops by keeping power and ground traces parallel and adjacent to each other. Significant package EMI can be reduced by using this method.

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Email	epic@ti.com
Internet	support.ti.com/sc/pic/euro.htm

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Fax	International	+81-3-3344-5317
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