Application Brief

Tips for Successfully Paralleling Power MOSFETs

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Paralleling power metal-oxide semiconductor field-effect transistors (MOSFETs) is a common way to reduce conduction losses and spread power dissipation over multiple devices to limit the maximum junction temperature. This application brief shares best practices and examples of paralleling power MOSFETs in various applications.

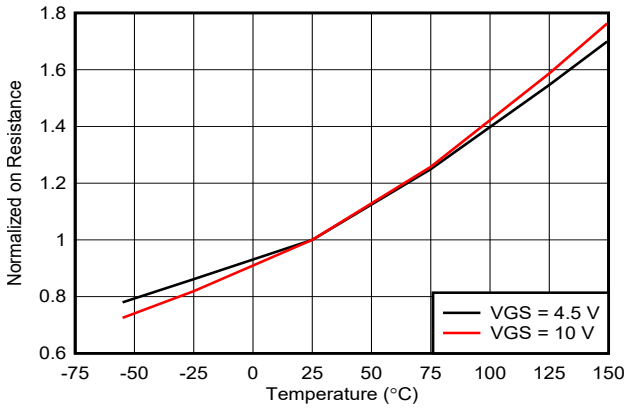

Figure 1. Power MOSFET On-Resistance vs. Temperature

First, consider static operation with two FETs operating in parallel, as shown in Figure 2.

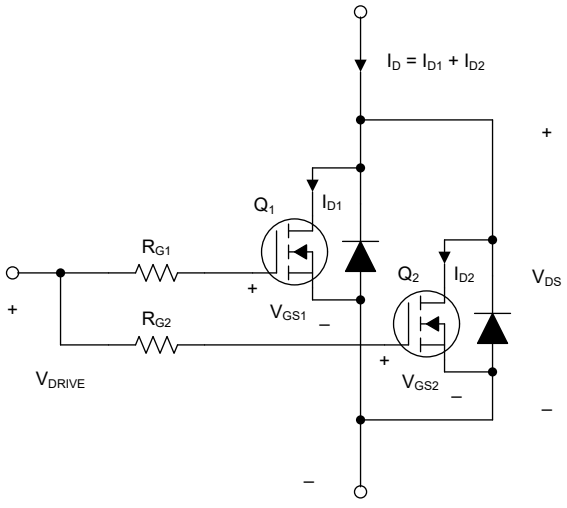

Figure 2. Two MOSFETs Connected in Parallel

The current in each FET is proportional to the inverse of its on resistance, $R_{DS(on)}$. Naturally, the device with the lowest $R_{DS(on)}$ will carry more current. As it heats up, its $R_{DS(on)}$ increases, shifting some of the current to the other FETs. The junction temperatures of paralleled FETs with good thermal coupling will be roughly the same. Current sharing still depends on the relative on-resistance of each FET and will be within the $R_{DS(on)}$ tolerances specified in the MOSFET data sheet.

During dynamic operation, the FET with the lowest threshold voltage, $V_{GS(th)}$, turns on first and turns off last. This FET takes more of the switching losses and sees higher stresses during switching transitions. To some extent, the thermal sharing effect balances out the switching and conduction losses, and the FETs will operate at roughly the same temperature.

Best Practices When Paralleling Power MOSFETs

Here are helpful tips when using FETs in parallel:

- Each FET needs its own gate resistor with a value from a few ohms up to tens of ohms. This helps with current sharing and prevents gate oscillations.
- FETs need good thermal coupling to ensure current and thermal balancing between devices. They can be mounted on a common heat sink or copper plane to maintain equal temperatures.
- The placement and layout of each FET should be identical and symmetrical, within reason, to equalize parasitic inductance in the critical gate-to-source and drain-to-source loops.
- Ensure that the gate-drive circuit can drive the higher capacitance (charge) of multiple devices without getting too hot. Remember, capacitance (charge) is multiplied by the number of paralleled MOSFETs.
- Avoid adding external capacitors from gate-to-source or gate-to-drain. If necessary, adjust the gate resistor's value to optimize the switching speed of the FETs .
- If you need Zener diodes to protect the MOSFET driver, place them close to the gate-driver outputs and before the gate resistors.

Schematic and PCB Layout Examples

Figure 3 shows a partial schematic and picture of the TPS2482 hot-swap evaluation module (EVM).

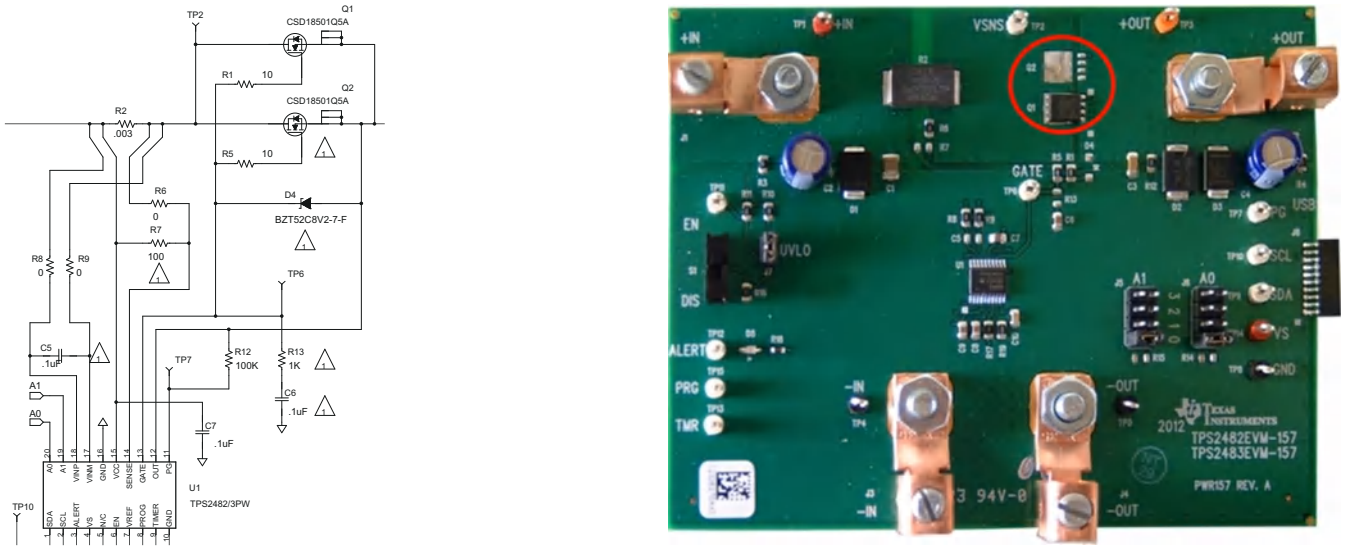

Figure 3. TPS2482 EVM Schematic and Printed Circuit Board (PCB)

As you can see in Figure 4, the TPS2482 EVM uses two CSD18501Q5A MOSFETs in parallel. The schematic shows how each FET has a 10-Ω gate resistor; the Zener diode is on the gate-driver output before the gate resistors. The FETs are placed close together on the same copper shape and use vias for good thermal coupling to spread the heat.

The next example, shown in Figure 4, is from the 18 V/1 kW, 160A Peak, >98% Efficient, High Power Density Brushless Motor Drive Reference Design.

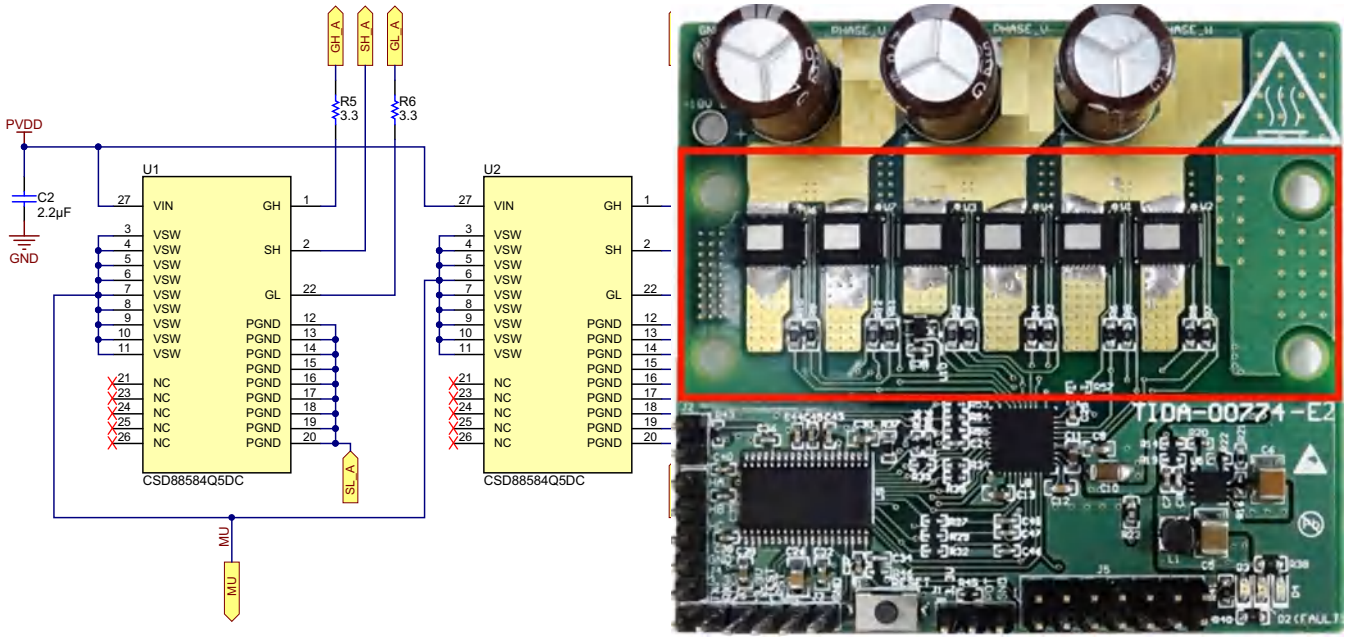

Figure 4. 18-V/1-kW Brushless Motor Drive Reference Design Schematic and PCB

This reference design uses two CSD88584Q5DC power MOSFETs in parallel per phase. Attaching the MOSFETs to the same heat sink for good thermal coupling helps remove the heat through the top side of the package. The design includes individual 3.3-Ω gate resistors for each FET in the power block.

The final example, shown in Figure 5 is from the 48-VDC Battery Powered 5-kW Inverter Power Stage Reference Design for Forklift AC Traction Motor.

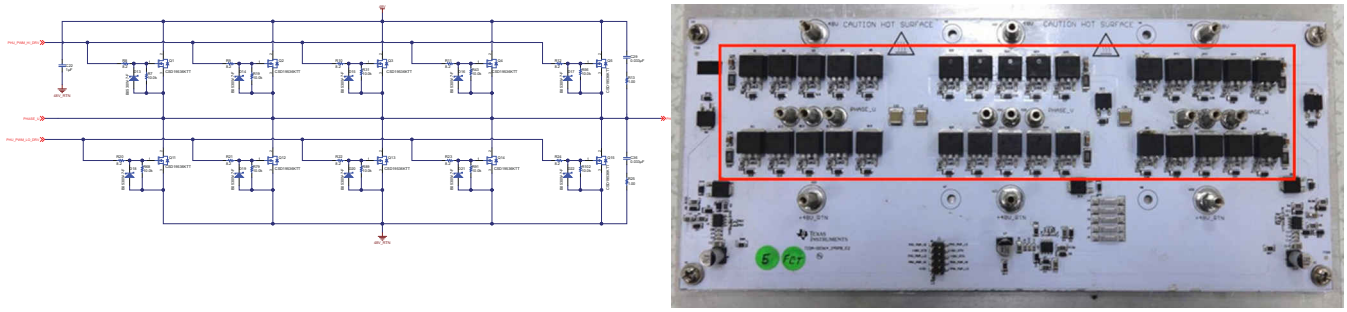

Figure 5. 5-kW Power-Stage Reference Design Schematic and PCB

This reference design uses five CSD19536KTT power MOSFETs in parallel for the high- and low-side switches in each phase. The FETs are mounted on an insulated metal substrate for cooling and good thermal coupling between devices. Each FET has an 8.2-Ω gate resistor.

Conclusion

Because of their inherent current- and thermal-sharing properties, paralleling MOSFETs can reduce conduction losses and limit their maximum junction temperature. Operating power MOSFETs in parallel can help solve the problems discussed in this article, but at a higher component count and cost, and a larger PCB area. If possible, use a single FET; if you cannot, carefully consider the design and layout of parallel FETs in your application to ensure success.

Additional Resources

Check out the following technical articles:

- *How to Choose the Right Power MOSFET or Power Block Package for Your Application*.
- *Improve the Performance of Your Power Tool Design with Power Blocks*
- Visit the TI MOSFET Support and Training Center.

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