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Advancing Silicon Performance Beyond the Capabilities of Discrete Power MOSFETs

Combining NexFET™ MOSFETs with stacked die techniques significantly reduceds parasitic losses

The drive for higher efficiency and increased power in smaller form factors is being addressed by advancements in both silicon and packaging technologies. The NexFET™ Power Block combines these two technologies to achieve higher levels of performance, and in half the space versus discrete MOSFETs. This article explains these new technologies and highlights their performance advantages.

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End equipment users from servers to base stations are becoming more concerned about efficiency and power loss as well as their impact on annual operating costs. This means that designers must improve efficiency throughout the power conversion process. Traditional approaches to improve efficiency in DC/DC synchronous buck converters include reducing conduction losses in the MOSFETs through lower $R_{DS(ON)}$ devices and lowering switching losses through low-frequency operation. The incremental improvements in $R_{DS(ON)}$ are at a point of diminishing returns and low $R_{DS(ON)}$ devices have large parasitic capacitances that do not facilitate the high-frequency operation required to improve power density. The NexFET Power Block is designed to leverage the NexFET power MOSFET's significantly lower gate charge and an innovative stacked die packaging approach to achieve dramatic performance improvements.

New Power Silicon

The major losses that occur within a MOSFET switch in a typical synchronous buck converter consist of switching, conduction, body diode and gate drive losses. The switching losses are primarily caused by the parasitic capacitances formed within the structure of the device. The conduction losses are a result of the device's resistance ($R_{DS(ON)}$) when in the enhanced mode of operation. The body diode losses are a function of its forward voltage and reverse recovery (Qrr). Gate drive losses are determined by the Qg of the MOSFET. Therefore, the parasitic capacitances and the $R_{DS(ON)}$ determine the performance of the device in a specific application. The most common technology used in today's low-voltage MOSFETs is the Trench-FET® (see Figure 1). The Trench-FET is known for its ability to achieve ultra-low resistance for a specific die size over the planar technology that it replaced. The only negative was that its parasitic capacitances actually increased. The large area of the trench walls makes it difficult to keep the internal capacitances small. The resulting high capacitances force designers to choose between a low operating frequency to optimize the efficiency and high frequency with better power density.

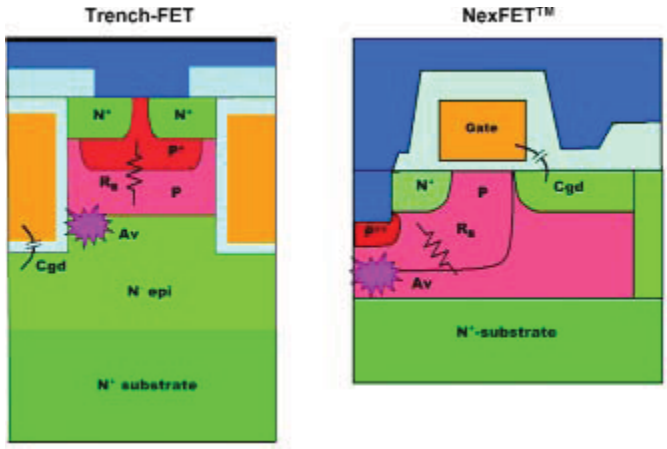

Figure 1: MOSFET structure comparison

In 2007, the NexFET power MOSFET was introduced. The NexFET can achieve a similar specific on resistance to the Trench-FET technology, while reducing associated parasitic capacitances by about fifty percent. The NexFET device finds its roots in a laterally diffused MOSFET (LDMOS) and combines vertical current flow to achieve high-current density. A closer look at the structure shown in Figure 1 reveals that the area underneath the gate has minimum overlap over source and drain regions, keeping the internal capacitances small. The reduced capacitances result in lower charges (Qg, Qgs, Qgd) required to switch the device. Therefore, the device switches faster, reducing switching losses within the MOSFET. With less energy required from the drive circuit, driver losses are reduced. The Miller charge (Qgd) within the device impacts its switching losses as well as determines the switch's ability to avoid C dv/dt turn on, which can further reduce efficiency and potentially damage the MOSFETs. The extremely low Qgd in the NexFET device minimizes turn on time and the potential for C dv/dt.

New Power Packaging

The NexFET power MOSFET takes a step toward creating an ideal switch by reducing parasitic capacitances. In order to maximize the performance of a typical synchronous buck converter, we need to minimize the parasitic inductances and resistances in the power circuit formed by the two MOSFETs in the power stage. This is accomplished through an innovative packaging approach in the NexFET Power Block where the MOSFETs are actually stacked on a grounded lead frame with two copper clips (see Figure 2). The resulting power block package has characteristics that make it unique in the power electronics industry. The package accomplishes four primary functions: small footprint, very low parasitics, excellent thermal performance, and solid reliability.

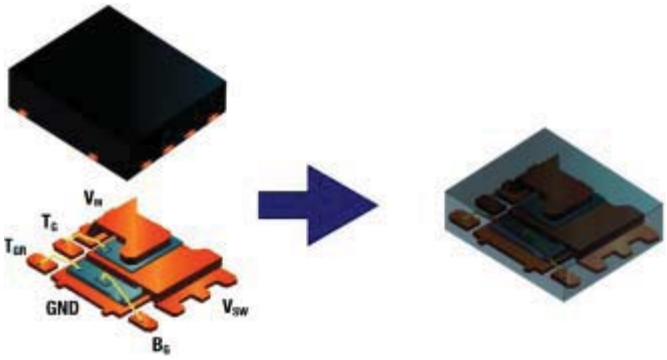

Figure 2: Source down technology allows MOSFETs to be stacked

To achieve a small footprint and the lowest parasitics possible, a stacking topology is used in the NexFET Power Block package design. A source down silicon technology allows high-side die to be stacked on top of the low-side transistor to implement a synchronous buck converter topology in a very simple and cost-effective manner. The low-side die is attached to the main pad of the lead frame, providing the ground connection of the MOSFET pair (see Figure 3). The low-side drain is connected to the outside through a thick copper clip that constitutes the device's switching node (V_{SW}). On top of the thick copper clip we solder die attached the high-side MOSFET, which also uses a source down technology. Finally, another thick copper clip connects the high-side drain (V_{IN} of the buck converter) to the device's external pins. The gate connections are made using Au wire bonds (T_G and B_G), and T_{GR} is the top gate return to the IC driver. T_{GR} is the switching voltage node sense signal that allows the IC driver to properly bias the high-side MOSFET gate.

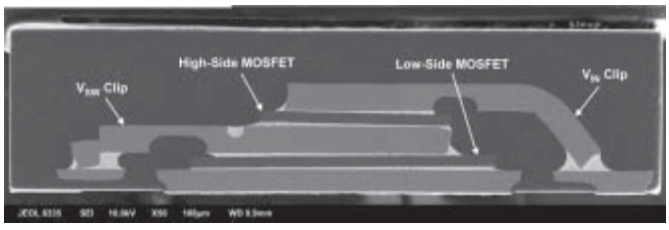

Figure 3: A cross sectional view of the NexFET Power Block illustrates a unique packaging approach

This package has an excellent electrical performance, which is critical in achieving high efficiency. Contributions to high efficiency can be summarized as:

1) Using thick copper clips for high-current connections (V_{IN} and V_{SW}), which substantially reduce the device's $R_{DS(ON)}$ in comparison with wire-bonded solutions. This also reduces conduction losses.

2) Thin silicon dies substantially reduce conduction losses by dropping the contribution of the device's substrate to $R_{DS(ON)}$.

3) The stacked configuration virtually eliminates the parasitic inductance and resistance between high- and low-side MOSFETS; and using thick copper clips substantially reduce parasitics associated with the V_{IN} and V_{SW} connections when compared to wire-bonded solutions. For a more detailed view of the package parasitics, refer to Figure 4. In general, reducing or even eliminating the buck converter's internal parasitic allows the system to switch faster and work at higher frequencies because of the reduced switching losses.

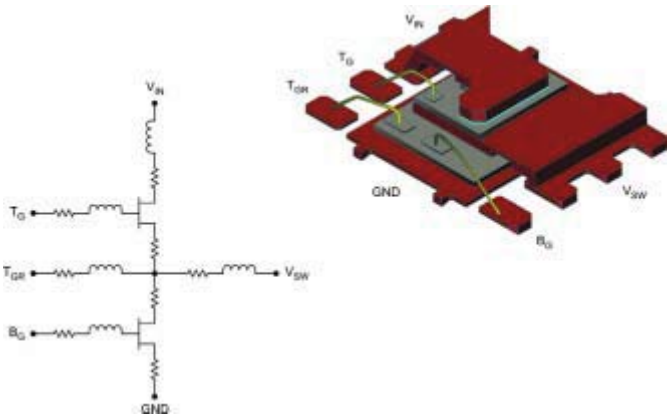

Figure 4: NexFET Power Block parasitic model package

The NexFET Power Block thermal performance is excellent with a measured thermal resistance junction to case $R_{\Theta JC}$ = 2°C/W and thermal resistance junction to air $R_{\Theta JA}$ = 50°C/W. The main reason behind these low-thermal resistance values are the reduced silicon thickness and thick copper clips that help to conduct heat generated to the package exterior. One might think that the stacked topology could increase the junction temperatures, especially on the high-side transistor. However, thermal measurements and simulations show that in normal operation the high-side junction temperature is only a fraction of a degree above the low-side die junction temperature. For example, in an experiment with the NexFET Power Block mounted in a typical application board with two Watts dissipated in the low-side die and one Watt dissipated in the high side, the top-side MOSFET junction is only 0.4°C higher than the junction of the low-side device. The results are reasonable considering that the thermal resistance between the die is extremely low, and the clips are conducting a substantial part of the heat generated by the stack to the package exterior.

Thermal performance combined with its lower power losses allow the NexFET Power Block to operate at similar temperatures to competitive solutions using two discrete MOSFETs. Figure 5 compares the measured temperatures of the NexFET Power Block versus a pair of MOSFETs. Both circuits operated under similar conditions and the Power Block's junction temperature was cooler than the discrete low-side MOSFET, and slightly hotter than the high-side device.

Another important characteristic is the package's impressive reliability performance. The power block has passed the following reliability tests:

- 1,000 cycles of temperature cycling –40 to 125°C (three cells of 77 units)
- 10,000 cycles of power cycling, delta junction temperature = 100°C (three cells of 77 units)

- 96 hours of autoclave, 121°C/100% RH (three cells of 77 units)
- 1,000 hours of THB, 85°C/85% RH (three cells of 77 units)
- 1,000 hours of HTRB, 150°C/80% rated VDS (three cells of 77 units)
- 1,000 hours of HTGB, 150°C/80% rated VGS (three cells of 77 units)

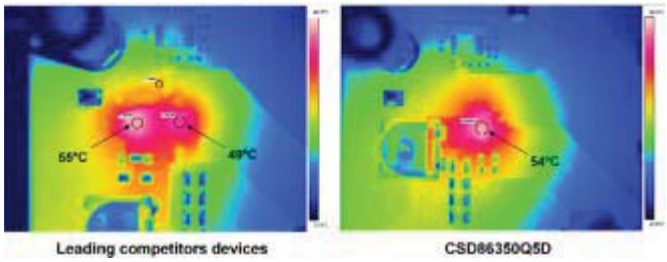

Figure 5: Thermal comparison of discrete MOSFETs versus the CSD86350Q5D NexFET Power Block

The combination of the silicon die thickness, bill of materials and a detailed design of the lead frames and clips results in a very reliable device that can sustain extreme temperature cycles and humidity levels without impacting performance.

New Power Solution

Combining the source down NexFET technology and the stacked die packaging technique significantly reduces the associated parasitics and creates a synchronous buck power block capable of outperforming discrete MOSFET transistors. The power block achieves over two percent higher efficiency at 25 amps than two discrete NexFETs with similar conduction and switching characteristics (see Figure 6). Efficiency peaks at over 93 percent and is 90.7 percent at 25 amps. The higher efficiency translates into more than a 20 percent reduction in power loss. The reduced power loss improves thermal performance and reduces system operating costs, or can be used to enable higher frequency operation to improve power density.

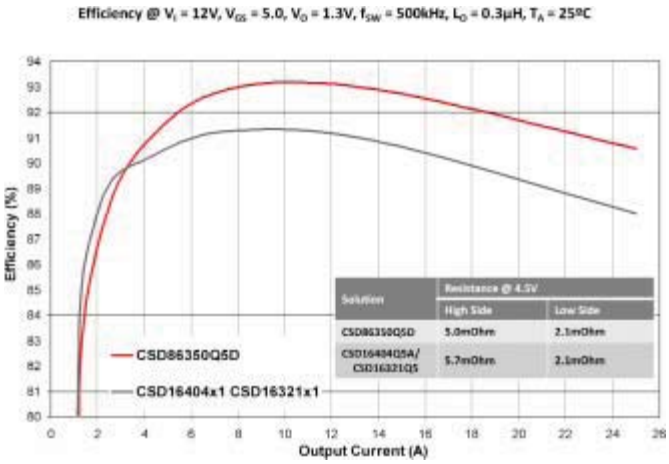

Figure 6: NexFET Power Block significantly improves efficiency over similar discrete MOSFETs

Beyond improving performance and reducing board space by 50 percent versus discrete MOSFETs, the NexFET Power Block simplifies the development effort. In discrete implementations, care must be taken in the layout when connecting the two devices to reduce inductance – now this concern is eliminated. The pinout allows easy placement of discrete components. This includes locating input capacitors close to the package, and the output inductor with the noise generating switch node on the opposite side of the package from the input capacitor and PWM controller IC. The NexFET Power Block also benefits from a grounded lead frame that should improve thermal performance and reduce electromagnetic interference (EMI). These attributes can help designers to achieve first-time success when designing with the NexFET Power Block.

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Learn more about NexFET technology here: www.ti.com/nexfet-ca.

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