User's Guide
SLOU444A–May 2016–Revised May 2016

TPA3136D2 Evaluation Module

This user's guide describes the operation of the TPA3136D2EVM. The user's guide also provides design information such as schematic, BOM, and PCB layout.

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1 Hardware Overview

The TPA3136D2 EVM customer evaluation module demonstrates the TPA3136D2 integrated circuit from TI.

The TPA3136D2 is a 10-W (per channel) efficient stereo digital amplifier power stage for driving 2 bridge-tied speakers. This document covers EVM specifications and design documentation that includes schematics, a parts list, and layout design.

Figure 1 illustrates the EVM board.

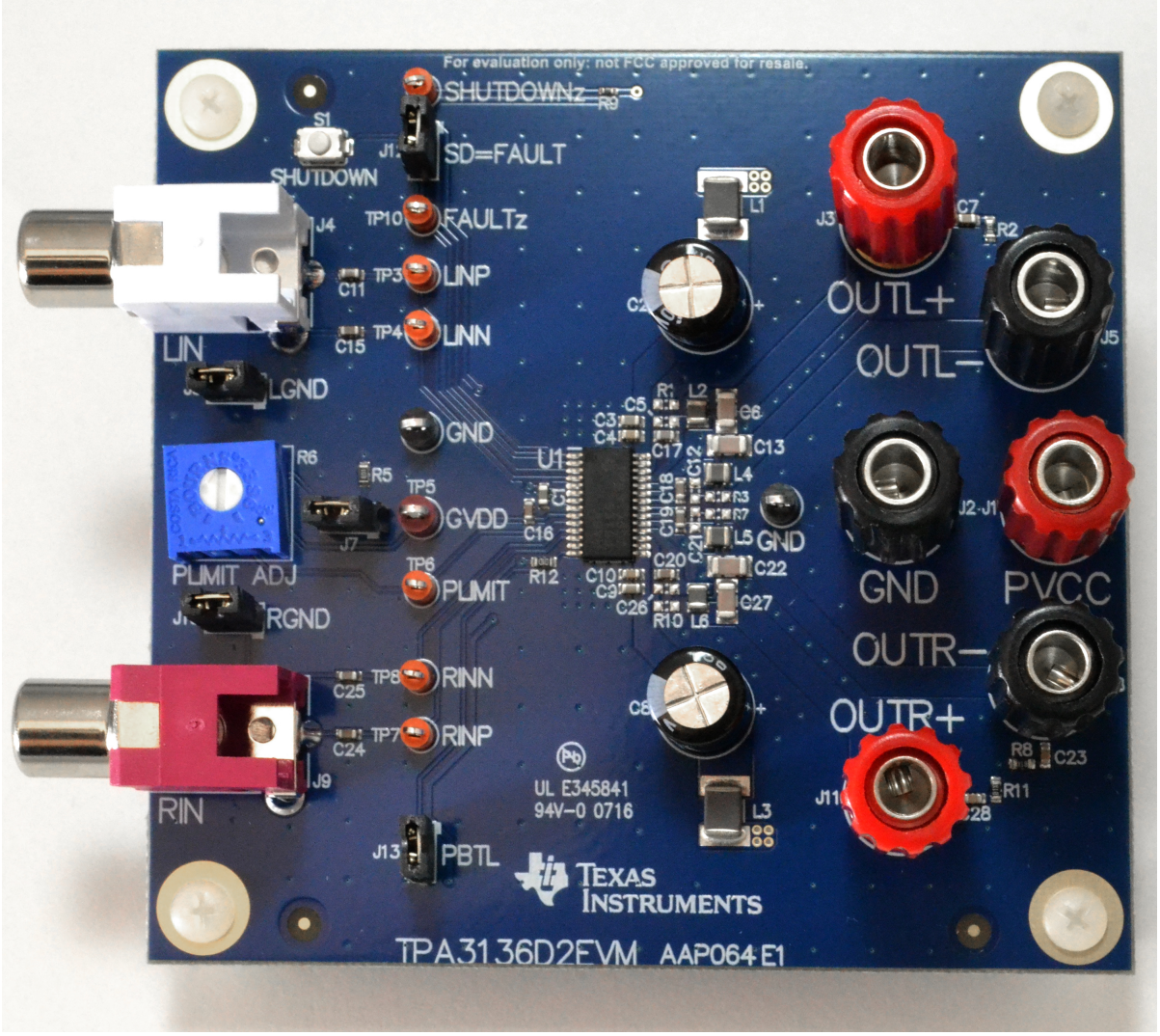

Figure 1. TPA3136D2EVM

Table 1 lists the specifications for the EVM board.

Table 1. TPA3136D2EVM Specifications

Key Parameters	Value
Power Supply Voltage	4.5 V to 14.4 V
Number of Channels	2 Bridge-Tied Load (BTL) Stereo
Load Impedance	4 Ω (12 V) to 6 Ω (> 12 V)
Output Power BTL	10 W per channel into an 8-Ω load

2 Operation

This section describes the TPA3136D2EVM board in regards to power supply and system interfaces. Information regarding handling and unpacking, absolute operating conditions, and a description of the factory default switch and jumper configuration are provided.

The following is a step-by-step guide to configuring the TPA3136D2EVM for device evaluation.

2.1 Electrostatic Discharge Warning

Many of the components on the TPA3136D2EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

CAUTION

Failure to observe ESD handling procedures may result in damage to EVM components.

2.2 Unpacking the EVM

On opening the TPA3136D2EVM package, ensure that the following item is included:

- 1 piece TPA3136D2EVM board using one TPA3136D2

If this item is missing, contact the Texas Instruments Product Information Center nearest you to inquire about a replacement.

2.3 Power Supply Setup

A single power supply is required to power up the EVM. Since most of the pins are PVCC-compliant, the PVCC supply can also be used to power the analog supply (AVCC) and can be used to pull up the logic pins for shutdown (SD) control, and fault detection (FAULT).

Table 2. Power Requirements

Description	Voltage Range	Current Requirement	Minimum Wire Size
PVCC	4.5 to 14.4 V	4 A	24 AWG

CAUTION

Applying voltages above the limitations given in Table 2 may cause permanent damage to your hardware.

2.4 Evaluation Module Preparations

Prepare the EVM in the following manner:

1. Ensure that the external power source is set to OFF.
2. Connect the external regulated power supply adjusted from 4.5 V to 14.4 V to the module PVCC and GND banana jacks taking care to observe marked polarity.

2.5 Inputs and Outputs

Configure the inputs and outputs on the EVM:

1. For a BTL configuration, connect a load or loads across the outputs (OUTL+ and OUTL–) and (OUTR+ and OUTR–).
2. For PBTL configuration, connect a single load from one of the left speaker jacks to one of the right speaker jacks, depending on how the filters are loaded. Apply a single input, differential or single-ended, to the RIN RCA phono plug and PBTL pin (pin 14) is tied high with J13 out.

2.6 Power Up

Use the following settings for power up:

1. Select the desired gain and mode of operation via J13 (IN = BTL, OUT = PBTL). Configure the input mode (J6/J10, OUT = Differential input mode, IN = Single-ended input mode).Verify correct voltage and input polarity and turn the external power supplies ON. The EVM should begin operation.
2. Adjust the audio source for the correct volume.

2.7 Recommended Settings

The following list provides the settings for two different configurations:

1. Single-ended input, auto-recovery mode, without Plimit, BTL (stereo output)

Table 3. TPA3136D2EVM Setting 1

Setting	Description
J4 (LIN)	L channel audio input
J9 (RIN)	R channel audio input
J6, set to IN	Single-ended input
J10, set to IN	Single-ended input
J7, set to IN	Able to change PLIMIT value with R6
R6	Change PLMIT voltage value (setting R6 = 0 Ω disables Plimit function)
J12 ($\overline{SD}$ = $\overline{FAULT}$) set to IN	Auto-recovery mode
J13 (PBTL) set to IN	BTL mode

2. Single-ended input, auto-recovery mode, PBTL (mono output)

Table 4. TPA3136D2EVM Setting 2

Setting	Description
J4 (LIN)	No audio input
J9 (RIN)	R channel audio input
J6, set to IN	Single-ended input
J10, set to IN	Single-ended input
J7, set to IN	Able to change PLIMIT value with R6
R6	Change PLMIT voltage value (setting R6 = 0 Ω disable Plimit function)
J12 ($\overline{SD}$ = $\overline{FAULT}$) set to IN	Auto recover mode
J13 (PBTL) set to OUT	PBTL mode

3 Board Layouts, Bill of Materials, and Schematic

3.1 TPA3136D2EVM Board Layouts

Figure 2 and Figure 3 illustrate the EVM board layouts.

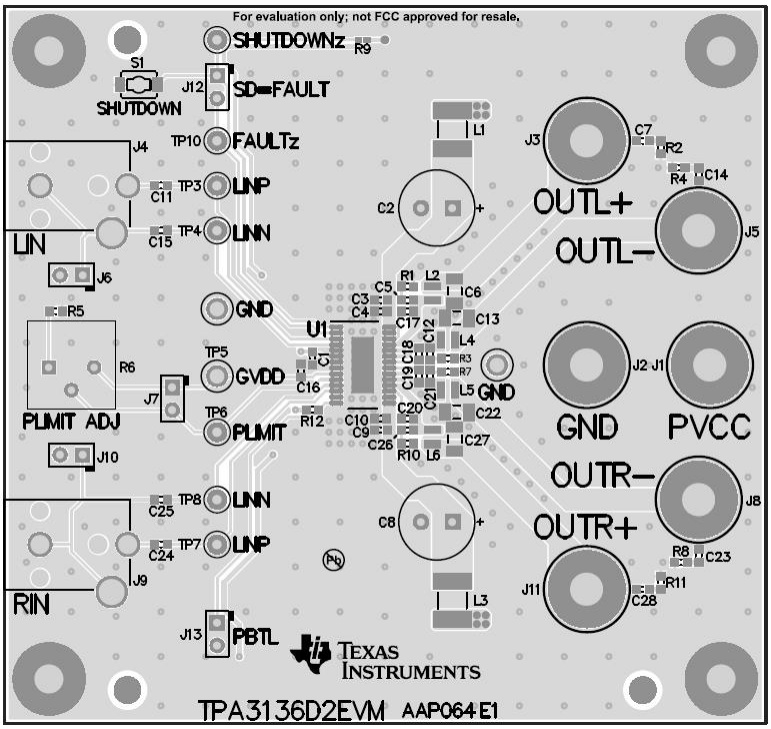

Figure 2. TPA3136D2EVM Top Composite Assembly

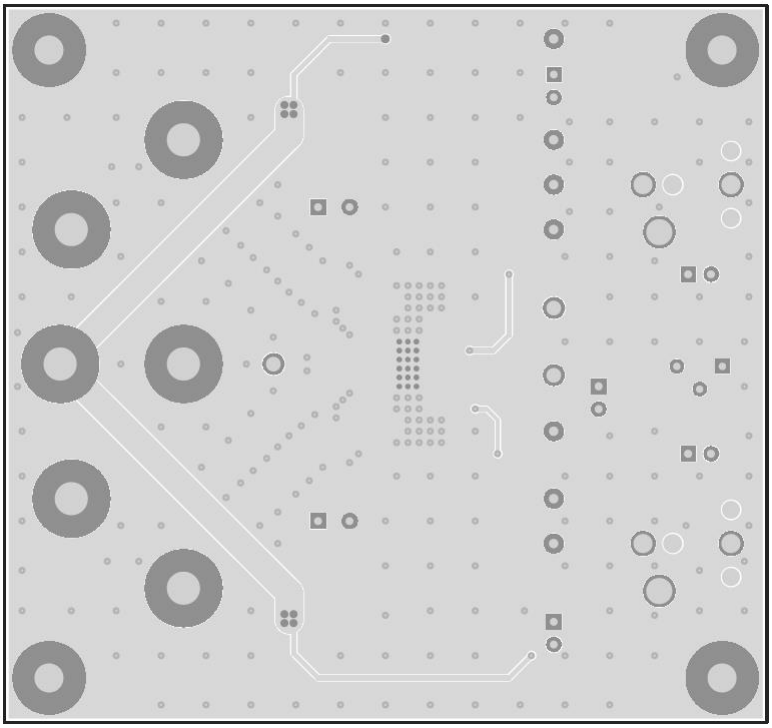

Figure 3. TPA3136D2EVM Bottom Composite Assembly

3.2 Bill of Materials

Table 5 displays the BOM for this EVM.

Table 5. TPA3136D2EVM Parts List

Designator	Qty	Value	Description	Package	Part Number	Manufacturer
C1	1	1uF	CAP, CERM, 1 µF, 35 V, +/- 10%, X5R, 0603	0603	GMK107BJ105KA-T	Taiyo Yuden
C2, C8	2	100uF	CAP, AL, 100uF, 50V, +/-20%, 0.17 ohm, TH	8.0x10.5mm	UHE1H101MPD	Nichicon
C3, C9	2	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	0603	GRM188R71H104KA93D	Murata
C4, C10	2	1000pF	CAP, CERM, 1000pF, 50V, +/-5%, C0G/NP0, 0603	0603	GRM1885C1H102JA01D	Murata
C5, C12, C21, C26	4	330pF	CAP, CERM, 330pF, 50V, +/-5%, C0G/NP0, 0603	0603	GRM1885C1H331JA01D	Murata
C6, C13, C22, C27	4	1000pF	CAP, CERM, 1000 pF, 100 V, +/- 10%, X7R, 1206	1206	12061C102KAT2A	AVX
C7, C14, C23, C28	4	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 10%, C0G/NP0, 0603	0603	06035A102KAT2A	AVX
C11, C15, C16, C24, C25	5	1uF	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	0603	GRM188R71C105KA12D	Murata
C17, C18, C19, C20	4	0.22uF	CAP, CERM, 0.22 µF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E224KA88D	Murata
J1, J3, J11	3		Binding Post, RED, TH	11.4x27.2mm	7006	Keystone
J2, J5, J8	3		Binding Post, BLACK, TH	11.4x27.2mm	7007	Keystone
J4	1		RCA Jack, White, R/A, TH	PC Mount Phono Jack-White, TH	970	Keystone
J6, J7, J10, J12, J13	5		Header, 100mil, 2x1, TH	Header, 2x1, 100mil, TH	800-10-002-10-001000	Mill-Max
J9	1		RCA Jack, Red, R/A, TH	PC Mount Phono Jack-Red, TH	971	Keystone
L1, L3	2	100 ohm	Ferrite Bead, 100 ohm @ 100 MHz, 8 A, 2-Pin SMD, Body 4.5 x 3.2 mm, Height 2.55 mm	2-Pin SMD, Body 4.5 x 3.2 mm, Height 2.55 mm	HI1812V101R-10	Laird-Signal Integrity Products
L2, L4, L5, L6	4	300 ohm	Ferrite Bead, 300 ohm @ 100 MHz, 3.1 A, 0806	0806	NFZ2MSM301SN10L	Murata
R1, R3, R7, R10	4	10.0	RES, 10.0, 1%, 0.25 W, 0603	0603	CRCW060310R0FKEAHP	Vishay-Dale
R2, R4, R8, R11	4	68	RES, 68, 5%, 0.1 W, 0603	0603	CRCW060368R0JNEA	Vishay-Dale
R5	1	10.0k	RES, 10.0k ohm, 0.1%, 0.1W, 0603	0603	RG1608P-103-B-T5	Susumu Co Ltd
R6	1	100k	TRIMMER, 100k ohm, 0.5W, TH	375x190x375mil	3386P-1-104LF	Bourns
R9	1	100k	RES, 100k ohm, 1%, 0.063W, 0402	0402	CRCW0402100KFKED	Vishay-Dale
R12	1	100k	RES, 100k ohm, 1%, 0.1W, 0603	0603	RC0603FR-07100KL	Yageo America
S1	1		Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	Switch, 4.4x2x2.9 mm	TL1015AF160QG	E-Switch
SHUNT1,SHUNT2, SHUNT3,SHUNT4, SHUNT5	5	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2	2	Black	Test Point, Compact, Black, TH	Black Compact Testpoint	5006	Keystone
TP3, TP4, TP6, TP7, TP8, TP9, TP10	7	Orange	Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone
TP5	1	Red	Test Point, Compact, Red, TH	Red Compact Testpoint	5005	Keystone
U1	1		15-W Filter-Free Stereo Class-D Audio Power Amplifier With Speakerguard, PWP0028E	PWP0028E	TPA3136D2PWP	Texas Instruments

3.3 TPA3136D2EVM Schematic

Figure 4 illustrates the EVM schematic.

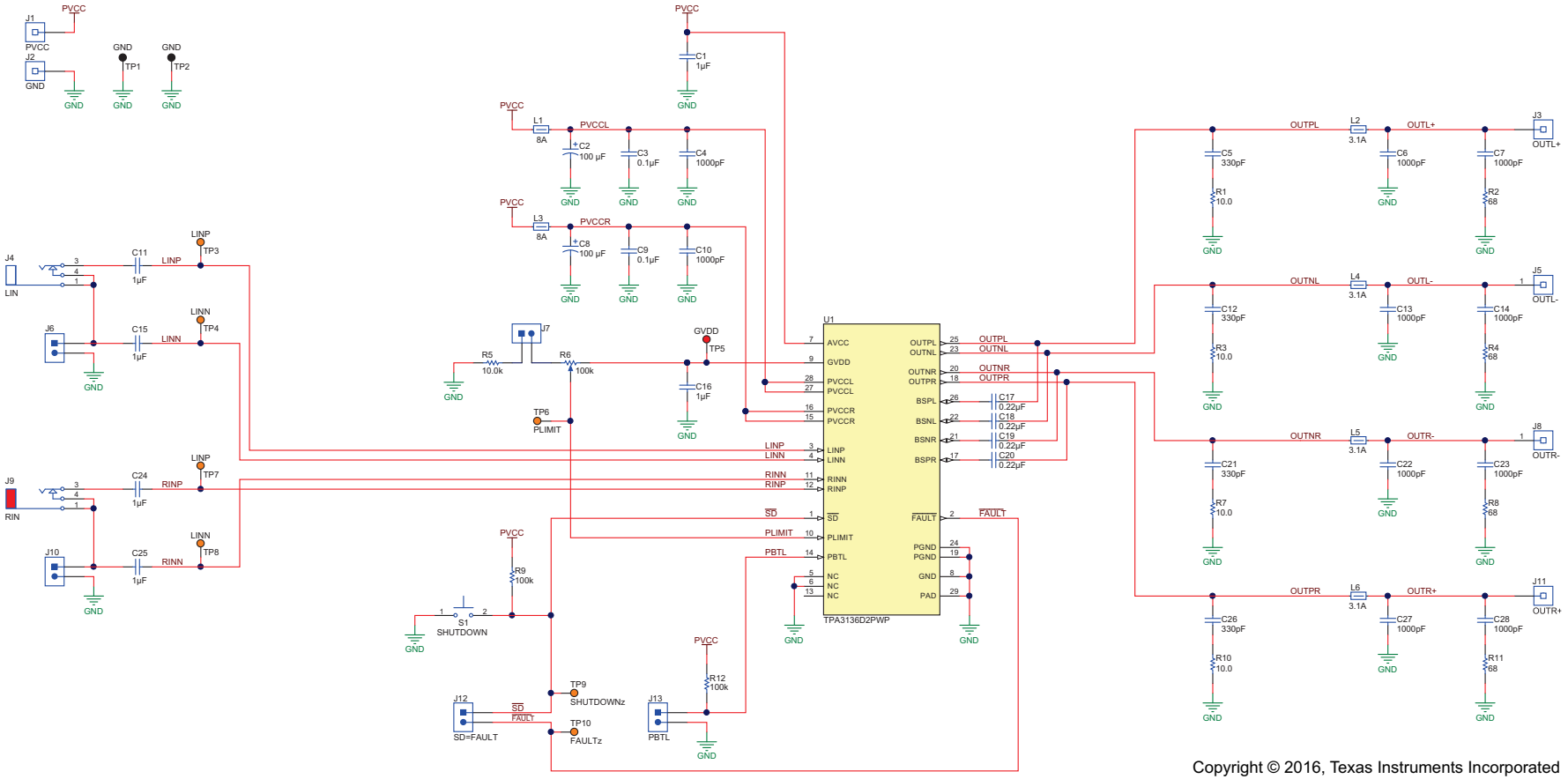

Figure 4. TPA3136D2EVM Schematic

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2016) to A Revision	Page
• Changed board image.	2

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      CAUTION

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      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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