TSW1250EVM: High-Speed LVDS Deserializer and Analysis System

Contents

List of Figures

List of Tables

1 Introduction

The Texas Instruments TSW1250 EVM is designed to evaluate the performance of high-speed ADC with serial LVDS output data format. Currently the TSW1250EVM supports the hi-speed ADS52XX series devices and Ultrasound AFE580X series devices from MHR group of Texas Instruments Inc. In the following paragraphs the ADS52XX series devices and AFE58XX series devices from MHR group will be called MHR_ADC for simplification and clearness purpose.

The TSW1250 includes a High-Speed LVDS Deserializer and Analysis System which provide a comprehensive set of hardware and user interface software to effectively evaluate the performance of a MHR_ADC.

The TSW1250 hardware has a high-speed connector that plugs into the MHR_ADC EVM. TSW1250EVM has FIFO memory sufficient to capture as much as 64K samples of data. A USB connection transfers the captured data to a personal computer for post-processing. The user Interface software controls the hardware of both TSW1250 and displays the FFT and important statistics related to the performance of the MHR_ADC.

2 Functionality

The TSW1250EVM connects to MHR_ADC EVM through a Samtec high-speed connector. The data format for the LVDS data is presented in a serialized format, where individual bits of the output data are presented on an LVDS line one bit at a time. The current MHR_ADC data is serialized onto a single LVDS pair at a rate that is 12/14/16 times the sample rate with 12/14/16-bit resolution. A DDR LVDS bit clock is used to strobe the serial data bits and to desterilize the data. An additional clock pair provided at the sample rate of the MHR_ADC identifies the sample-word boundaries in the serial data. A single-bit clock and a single sample-rate clock (frame clock) are used for all of the LVDS data channels. The sample rate is up to 65 MHz.

The FPGA firmware for the TSW1250 consists of two major functions: the LVDS interface and the FIFO capture. The LVDS interface code in the FPGA reformats the data into a standard single-ended parallel data word with sample clock. This parallel sample word plus clock is output continuously to header posts on the TSW1250 for capture by a logic analyzer. The TSW1250 FPGA has enough FIFO buffer to capture as much as a 65536-sample record length from the continuous sample data stream coming from the LVDS interface.

The TSW1250EVM includes a UART function that can transfer data to and from a USB interface device on the TSW1250 board. The USB interface device on the TSW1250EVM connects to a personal computer (PC) running Windows™ over a standard USB cable. The operation of the FIFO capture logic is controlled by writes from the PC USB port to a register map defined within the FPGA. The user interface software on the PC selects by register operations such things as record length of data to capture, which channel of a MHR_ADC to capture from, and then the user interface software downloads the captured data from the TSW1250 for processing in the form of an FFT or time-domain display.

3 Hardware Configurations

In this section, the various portions of the TSW1250EVM hardware are described.

3.1 Power Connections

The TSW1250EVM hardware is designed to operate from a single-supply voltage of greater than 6 Vdc. For convenience, two options can supply power to the TSW1250EVM. A bench power supply can supply power to banana jack connections on the TSW1250EVM, or a laptop-style power module that is included with the TSW1250 hardware can supply power. Figure 1 shows the relative position of the power connections on the TSW1250EVM.

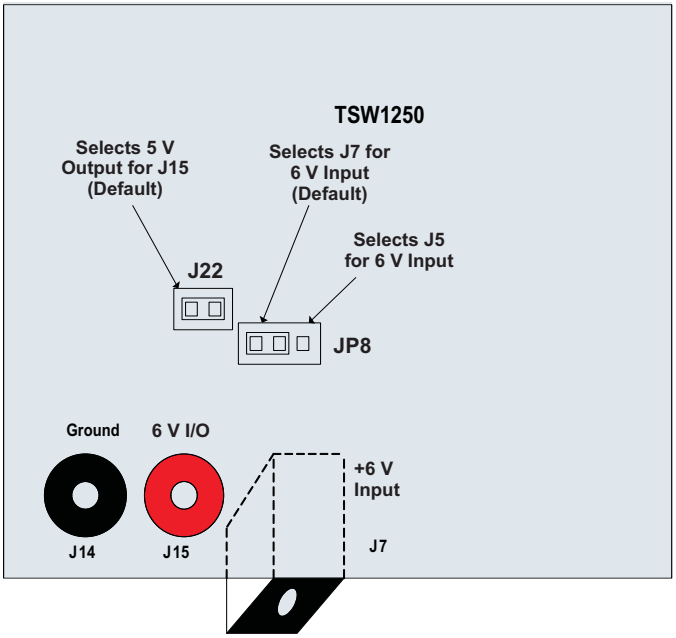


Figure 1. Position of Power Connections

CAUTION

TI recommends that the black banana jack J14 be connected to a bench ground even if the 6-V external power brick is connected to J7. Intermittent loss of the USB connection can sometimes be observed without a good ground from the TSW1250EVM to the bench ground reference.

Care must be taken in the selection of the input power supply. One jumper selects whether the 6-V input power comes from the banana jack, or whether it comes from the external power module. Another jumper selects whether to connect the onboard regulated 5 V to the red banana jack for output. If the red banana jack is used to input 6 V from a bench power supply, the onboard regulated 5 V must not be connected to the red banana jack for output at the same time. Doing so causes the onboard 5-V regulator to fail over time.

3.2 Switches and Jumpers

3.2.1 Pushbuttons

Four pushbutton switches are mounted on the TSW1250EVM. Two pushbutton switches currently have defined functions; two of the switches are reserved for future use.

Switches	Description
SW3	Causes the FPGA to reload its bit file from the FPGA EEPROM.
SW4	Causes the FPGA to clear the FIFO storage, but does not clear any of the register settings in the FPGA. Any configuration of the FPGA done through register operations such as setting the UART baud rate will persist after pushing the RESET pushbutton.
SW2,SW5	Reserved for future use

3.2.2 Jumpers

Jumpers	Description
J10, J11	Select the bit file to be programmed into the FPGA. Always set as the Figure-3. Other settings are for future development.
JP8	Selects the source of the power supply to the TSW1250EVM.
	Jump Left sides: Select the external 6-V power module through power jack J7. (Default).
	Jump Right sides: Select an external 6-V bench power supply through the red banana jack J15. J15 is an input for this selection.
J22	Jump to connect the onboard regulated clean, low-noise 5 V to the red banana jack J15 as an output.
J16	For factory to program the USB EEPROM. Installs always.
J17	Disable the 1.2-V power regulator for the FPGA core logic. Always OPEN.
J1, J12	JTAG chain. Set is as default.

CAUTION

It is possible to select the red banana jack J15 as an input to be connected to a 6-V bench supply and at the same time install jumper J22 to connect the regulated 5 V to the red banana jack as an output. However, this causes the 5-V regulator on the TSW1250 to fail over time.

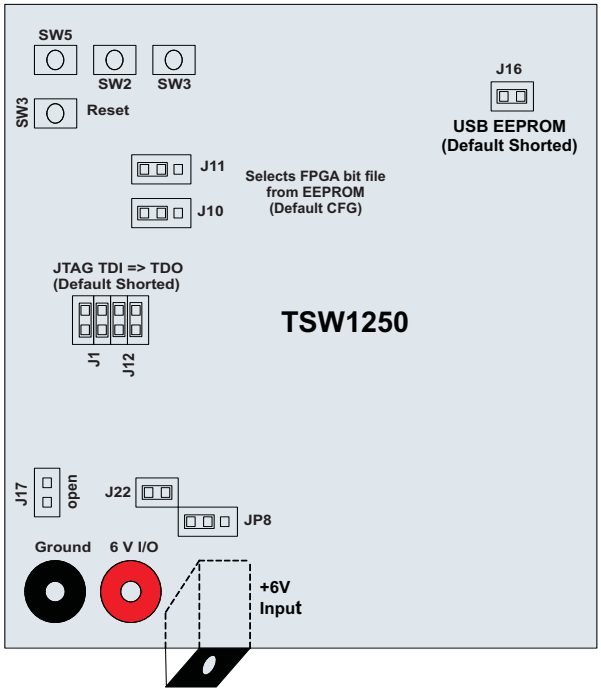


Figure 2. Position of Switches and Jumpers

3.3 LEDs

Six LEDs are on the TSW1250EVM to indicate the presence of power and the state of the FPGA. See Figure 3.

LED D16 illuminates to indicate the presence of a 6-V power supply to the board.

The rest of the LEDs are mainly for internal development reference.

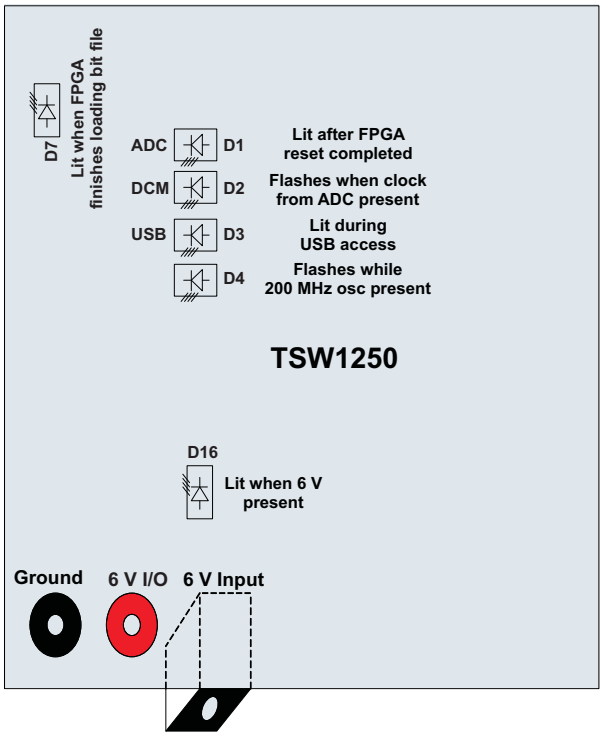


Figure 3. Position of LEDs

3.4 Input Connections

3.4.1 Samtec LVDS Connector

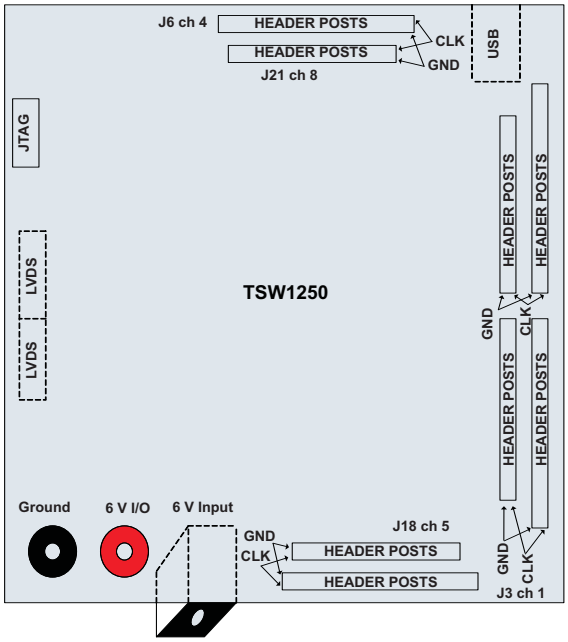


Figure 4. Position of Input, Output, and USB Connections

Figure 4 illustrates the position of the various input and output connections on the TSW1250EVM. The connection between the TSW1250EVM and the MHR_ADC EVM to be tested is through a 120-pin Samtec connector. Sixteen LVDS data pairs plus two LVDS clock pairs have a defined position in the connector pinout that is common between the TSW1250EVM and MHR_ADCEVMs. The bit clock runs at a higher multiple of the MHR_ADC sample clock and is used to strobe the serial data into the TSW1250EVM and then deserializes the data. A second clock is provided, called the frame clock or FCLK, that runs at the sample rate and is used to delineate the sample boundaries in the serial data stream. There are 16 extra LVDS pairs defined in the connector and routed to the TSW1250EVM FPGA for future expansion. The data direction for the LVDS data pairs is always defined as the MHR_ADC EVM driving the signal through the connector to the TSW1250EVM FPGA, with integrated 100-Ω termination in the FPGA.

Five extra CMOS single-ended signals are defined in the Samtec connector that are sourced from the FPGA through the connector to the MHR_ADC EVM. These signals are optionally defined to allow the FPGA (under control of the TSW1250 user interface software) control the SPI serial programming of the MHR_ADC EVMs that support this feature. The supported SPI signals SEN (SPI Enable), SCLK (SPI Clk), SDATA (SPI Data) and SPI Reset and SPI Power Down are sourced by the TSW1250EVM FPGA to allow the TSW1250 user Interface to configure the operational mode of the MHR_ADC under evaluation.

The Samtec connectors snap together with no screws or other mechanism to hold the TSW1250EVM and the MHR_ADC EVM together. The TSW1250EVM comes with standoff posts for setting the TSW1250EVM flat on a bench or table. The MHR_ADC EVM has shorter standoff posts so that the TSW1250EVM and MHR_ADC EVM will lay flat on a bench or table and stay snapped together during use.

3.4.2 JTAG Connector

The TSW1250EVM includes an industry-standard JTAG connector that loops the JTAG ports of the FPGA and the FPGA EEPROM. Jumpers on the TSW1250EVM allow for either the FPGA or the FPGA EEPROM to be removed from the JTAG chain. The most frequent use for the JTAG connector is to program the TSW1250EVM FPGA. An FPGA programming pod can be purchased inexpensively from Xilinx™ to program the FPGA or the FPGA EEPROM. The FPGA programming pod can be used to load a programming bit file directly into the FPGA for debug and development. However, once the FPGA is power-cycled or programmed by the PROGRAM pushbutton, this loaded FPGA bit file will be lost and the FPGA will revert to the bit file that is stored in the FPGA EEPROM. The FPGA programming pod also can be used to store a new FPGA programming bit file in the FPGA EEPROM so that the TSW1250 can be upgraded as new revisions of FPGA firmware become available. The part number of the Xilinx Platform Cable USB programming pod that can be used to program or upgrade the TSW1250EVM is **DLC9G**. The programming pod operates from a USB port of a PC and connects directly with the TSW1250 JTAG connector through a ribbon cable supplied with the programming pod.

3.5 Output Connections

(This feature is in the process of development)

Two ways are available to output the parallel clock and sample data from the TSW1250EVM. The MHR_ADC sample data can be presented as a continuous stream of CMOS single-ended data on output header posts, or a set record length of MHR_ADC parallel data samples can be captured in the TSW1250EVM FIFOs and output to a PC through the USB serial port. The data capture by the FIFOs and TSW1250 user interface is the most convenient way to capture data from an MHR_ADC, but sometimes the continuous stream of data is desirable. For example, an application may require a larger capture depth for an FFT on a million continuous data samples or more. For this, the output header posts are available so that a logic analyzer can be used to capture MHR_ADC data in real time.

The pinout of the output data headers is shown in Figure 5. In all cases, the output header is a standard two-row header of square 0.025-inch posts on 0.1-inch centers. One of the two rows of posts are connected to ground down the whole row of posts, whereas the other row of posts are signal. The sample-rate clock is presented on the first post, and after skipping one no-connect post (or three posts for Channel 1) the parallel data bus is presented from the least-significant bit (bit D0) through the most-significant bit.

During the test; the selected channel is always exporting the parallel data to the primary header J5. Users can choose any other channel to export to Auxiliary Header J4.

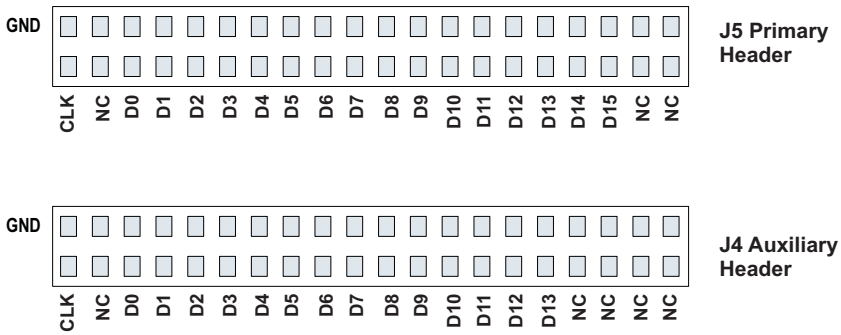


Figure 5. Pinout of Header Posts for Parallel Output Data

3.6 USB I/O Connection

Control of the TSW1250EVM is through an USB connection to a PC running Windows operating system. For the computer, the drivers needed to access the USB port are included on the TSW1250 are installed during the installation process. The USB is accessed as a virtual communication port (VCP) and shows up in the Hardware Device Manager as TSW1250. On the TSW1250EVM, the USB port acts as a bridge to UART control of the FPGA. Control of the FPGA is managed by reads and writes to a register map of control registers defined in the design of the FPGA. Normally, register writes from the TSW1250 user interface software sets up the mode of operation of the FPGA. These register writes define such things as the depth of FIFO to use for data capture or from which channel of a MHR_ADC to capture data. Then, a single register access triggers the filling of the capture FIFOs. Immediately after the capture FIFOs have captured the desired amount of data, the FIFO data is streamed back up the USB connection to the TSW1250 user interface software. The UART data rate between the FPGA and the USB port can be set to 115K, 230K, or 460K baud. On first connection of the USB port to a computer, the Microsoft Found New Hardware Wizard appears. Follow the dialog box prompts as covered in the Software Installation section of this User's Guide.

4 Software Installation

The TSW1250EVM GUI (SLOC231) can be downloaded from the TI Web site. Open the **"Read me first.pdf**" follow the directions to install the GUI and drivers.

5 Graphics User Interface (GUI)

TSW1250 provides a GUI for easier control of the EVM and the device under test. When the TSW1250 GUI is started, the screen of Figure 6 appears. Five groups comprise the GUI.

1. Toolbar
2. Message Window
3. Device Specific Selections
4. Test Parameters
5. Central Pane Display

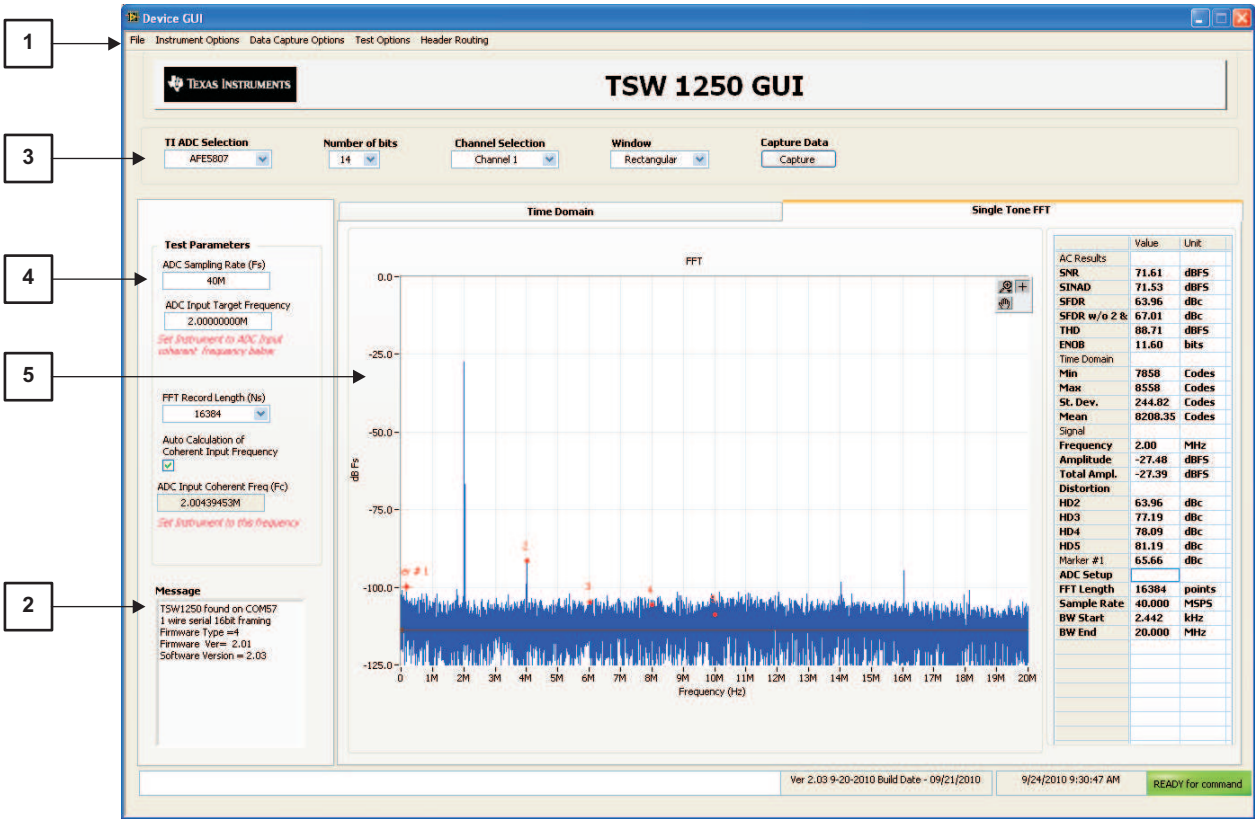


Figure 6. TSW1250 GUI

5.1 Toolbar

The toolbar contains options and settings that are independent of the device selected for test or the test to be performed, such as configuration options and save/recall operations. The operations available under the toolbar are grouped in categories of:

File
Instrument Options
Data Capture Options
Test Options

5.1.1 File

1	Save Binary File	Save the data in binary format.
2	Save Single Tone Data	Save the FFT data and its associated frequency. Only the data of the active channel is saved.
3	Save Time Domain data	Save the Time Domain data. Only the data of the active channel is saved.
4	Save Measurement to CSV	Save the measurement data. The data can be in frequency domain or time domain whichever is active. Multiple channels data are allowed. The targeted channels must complete the CAPTURE process before this save command. (1)

(1) Save Measurement to CSV.
This function allows the user to save multiple channels simultaneously. For example, if the user intends to save channel 1 and channel 3, then the following steps must be done.

1. Apply the signal input to channel 1.
2. From the GUI, select channel 1 in the Channel Selection box.
3. Press Capture button to complete data capture.
4. Repeat the preceding steps for Channel 3.
5. Select Save Measurement to CSV, and choose the items intended to save. The example chooses every item.

5	Save Capture as JPENG, BMP, or PENG	Save the image in the file. If the Single Tone FFT test is active, then the FFT plot is being saved, along with the performance statistics and setup information. If the Time Domain test is active, then the Time Domain plot is saved along with the time domain statistics. The saved data plot can be saved in jpeg, png, or bmp format

The result is shown in the following table.

Single Tone FFT	Unit	Channel 1	Channel 3
SNR	dBFS	71.7	71.68
SINAD	dBFS	71.61	71.65
SFDR	dBc	64.72	68.74
SFDR w/o 2 and 3	dBc	67.22	68.74
THD	dBFS	88.89	93.74
ENOB	bits	11.62	11.61
Time Domain			
Min	Codes	7856	7835
Max	Codes	8560	8543
St. Dev.	Codes	245.59	247.96
Mean	Codes	8208.81	8189.18
Signal			
Frequency	MHz	2	2
Amplitude	dBFS	–27.45	–27.37
Total Ampl.	dBFS	–27.34	–27.29
Distortion			
HD2	dBc	64.72	70.52
HD3	dBc	78.21	80.34
HD4	dBc	77.98	79.06
HD5	dBc	86.33	80.59
Marker #1	dBc	0	64.72
ADC Setup			
FFT Length	points	16384	16384
Sample Rate	MSPS	40	40
BW Start	kHz	2.442	2.442
BW End	MHz	20	20

5.1.2 Instrument Options

The Instrument Options menu tab are reserved for future development:

5.1.3 Data Capture Options

The Data Capture menu tab contains four options as shown in the following.

1	Continuous Capture	Default is non-continuous. Allows to switch to continuous mode.
2	External Trigger	Default is internal, check to switch to external.
3	LSB First	Default is MSB First, check to change to LSB First
4	UART Baud Rate	Default is 460800 bps. Options are available to go to slower rate.

5.1.4 Test Options

The Test Options menu tab has two options : Time Domain and Single Tone.

Time Domain is reserved for future development.

Single Tone has the following options:

1	Number of Harmonics	The number of harmonics to be displayed. Default is 5.
2	dBFS	Check for dBFS, unchecked for dBC. Default is dBFS.
3	RMS	Check to enable RMS line in the display.
4	Nullify Bins	Specify the start/stop bins to null the spectrum.
5	Nullify Bands	Specify the start/stop frequency to null the spectrum.

RMS
For a Single Tone FFT test, the RMS line may be enabled or disabled. When enabled, a horizontal marker is displayed over the FFT plot to indicate the RMS average of the noise floor of the FFT plot. The RMS average is computed over all of the FFT bins except the bin containing the input frequency. More precisely,

RMS line = SINAD + FFT Record Length Process Gain
FFT Record Process Gain = 10log(number of points/2)

dBFS
SNR, SFDR, and SINAD can be expressed in either dBc or dBFS as selected by the dBFS selection under the Single Tone FFT options. By default, the noise calculations for SNR and SINAD do not include the five FFT bins around the expected input frequency or the first five FFT bins at DC. The rest of the FFT bins out to the Nyquist frequency are included in the calculation of the total noise. Vertical marker cursors are present in the FFT display that indicate the beginning and the end of the bandwidth of interest for noise calculations. Because these vertical markers are located at the extreme left-most and right-most positions on the FFT display, these vertical markers often are not noticeable. It is possible to compute the total noise power over a narrower range than the default DC through Nyquist band of frequencies. An integration band for the noise calculations can be set in two ways.

- **First,** click the mouse on one of the vertical cursors and drag it to a new desired location.
- **Second,** the Cursor Band Location window under the Single Tone FFT Test Option in the tool bar can be used to set a new frequency band of integration for the calculation of the total noise power.

Also excluded from calculation of the SNR is the power in the first five harmonics of the input frequency.

These first five harmonics are included in calculation of SINAD (signal to noise and distortion) and thus this is the principal difference between SNR and SINAD. (SINAD is sometimes called SNDR, signal to noise and distortion ratio.) The number of harmonics to exclude from SNR can be set to a value other than the default 5 in the Number of Harmonics window in the Single Tone FFT Test Option in the toolbar.

5.2 Message Window

The lower left portion of the TSW1250 user interface software window under the TI logo is reserved for reporting status, warnings, errors, and informational output. When the TSW1250 software is first run, it queries the TSW1250EVM and displays the revision of the FPGA firmware and the type of MHR_ADC interface the TSW1250EVM is expecting to see based on jumper settings J10 and J11. At any time, this initial information can be displayed again by selecting the Reinitialize Instrument option in the Instrument Options tab of the toolbar.

5.3 Device-Specific Selections

Drop-down menus that are specific to a particular MHR_ADC device selection are located along the top of the display under the toolbar. Users can select a MHR_ADC device from the device selection drop-down menu. Once a MHR_ADC device part number is selected, the MHR_ADC Channel can be selected in the Channel selection drop-down menu. The format for display of the captured data is chosen in the Test Selection drop-down menu. Single Tone FFT displays the power spectrum of the captured data with calculated AC performance statistics. Time Domain displays the raw captured data in the format of a logic analyzer display and output level over time. In the Window Display drop-down menu, the user chooses a windowing function to be applied to the captured data. A Rectangular Window applies a unity gain to all data points of the captured data. A Hanning Window, Hamming Window, or Blackman-Harris Window function can be applied to the captured data for situations where the sample rate and the input frequency are not or cannot be set precisely to capture an integer number of cycles of the input frequency (sometimes called coherent frequency). The Capture button initiates a data capture once all other selections are made. The data capture can be a single capture and display, or a continuous repeating capture.

5.4 Test Parameters

The six test parameters are: Sampling Rate (FS), ADC Input Target Frequency, FFT Record Length (Ns), Auto Calculation of Coherent Input Frequency, Overlay Unwrap Waveform, and ADC Input Coherent Frequency (FC).

The sampling rate is called the Sampling Frequency FS. The number is entered in Hertz (Hz), although the letter M may be appended to represent the sampling rate in MHz. For example, 125M = 125 MHz or 125,000,000 Hz.

The expected input frequency is entered in the ADC Input Target Frequency input box.

If the Auto Calculation of Coherent Input Frequency mode is enabled, then this input frequency is adjusted up or down slightly away from the input frequency automatically to derive a coherent frequency called ADC Input Coherent Frequency (FC). If coherent input frequency is required, the signal generator used to source the input frequency must be set to this exact calculated coherent frequency. The coherent frequency calculation takes the sampling frequency, the input frequency as entered by the user and the FFT record length and adjusts the input frequency so that the captured data starts and ends on the same place of the sine wave of the input frequency. This avoids an artifact of the FFT calculation from presenting a *smeared* power spectrum due to the fact that the FFT presumes the sample of the input is part of a continuous input signal. If the input and sampling frequency is not coherent, and the sampled data is appended end to end to form a continuous input signal, then an apparent phase discontinuity at the beginning and the end of the sampled data occurs. Making the sampling and input frequencies coherent avoids this apparent discontinuity. If the input frequency cannot be made coherent, then the windowing functions other than Rectangular can be used to process out this effect to some degree.

The FFT record length can be set in the FFT Record Length (NS) input text box. The TSW1250EVM supports FFT record lengths of as much as 65536 samples, or as little as 4096 samples.

The sampling rate is entered in the ADC Sampling Rate text box, also called the Sampling Frequency FS. The expected input frequency is entered in the ADC Input Frequency input box.

The Overlay Unwrap Waveform check box is used in the Time Domain test. It allows a calculated normalized waveform to be overlaid over the sample data. If the sample and input frequencies are coherent, the sampled data is normalized into a calculated representation of a single period of a sine wave. Errors in the sampled data for any reason become immediately apparent as spikes on the unwrapped waveform.

5.5 Central Pane Display

The large central pane display area includes two Tabs.

Tab1	Time Domain Test
Tab2	Single Tone FFT Test

They are described in the Time Domain Test and Single Tone FFT Test.

5.5.1 Time Domain Test

The Time Domain test is shown in Figure 7. The larger central pane displays the raw sampled data whereas the calculated statistics are grouped into categories on the right of the screen. Settings and inputs relevant to the test are entered in drop-down menus or text input boxes on the left portion of the window.

5.5.2 Time Domain Results

The captured sample data is displayed in two formats in the Time Domain results window. In the upper half of the window, the arithmetic value of the sample is represented on the vertical scale. In the lower half of the window the individual bits of the data are displayed as if it were captured by a logic analyzer. If Unwrap Waveform is enabled, the normalized calculation of one period of a sine wave is overlaid over the time domain data in the upper half of the display.

The Time Domain display automatically scales the horizontal display to represent the full data capture to the amount specified by the FFT Record Length. The horizontal scale may be manually adjusted by highlighting the minimum and maximum sample limits and typing in new scale limits. The Time Domain display automatically scales the vertical display according the bit resolution of the selected MHR_ADC. For example, for a 12-bit AFE58xx, the vertical scale is represented as values from 0 through 4000. For a 14-bit AFE58xx, the vertical scale is represented as values from 0 through 16000. The vertical scale can also be adjusted manually by highlighting limits of the scale and typing in new limits.

5.5.3 Time Domain Statistics

For the Time Domain test, sample statistics are displayed on the right of the display. The minimum and maximum sample values are displayed, as is the median sample and the mean, standard deviation, and RMS value of the samples.

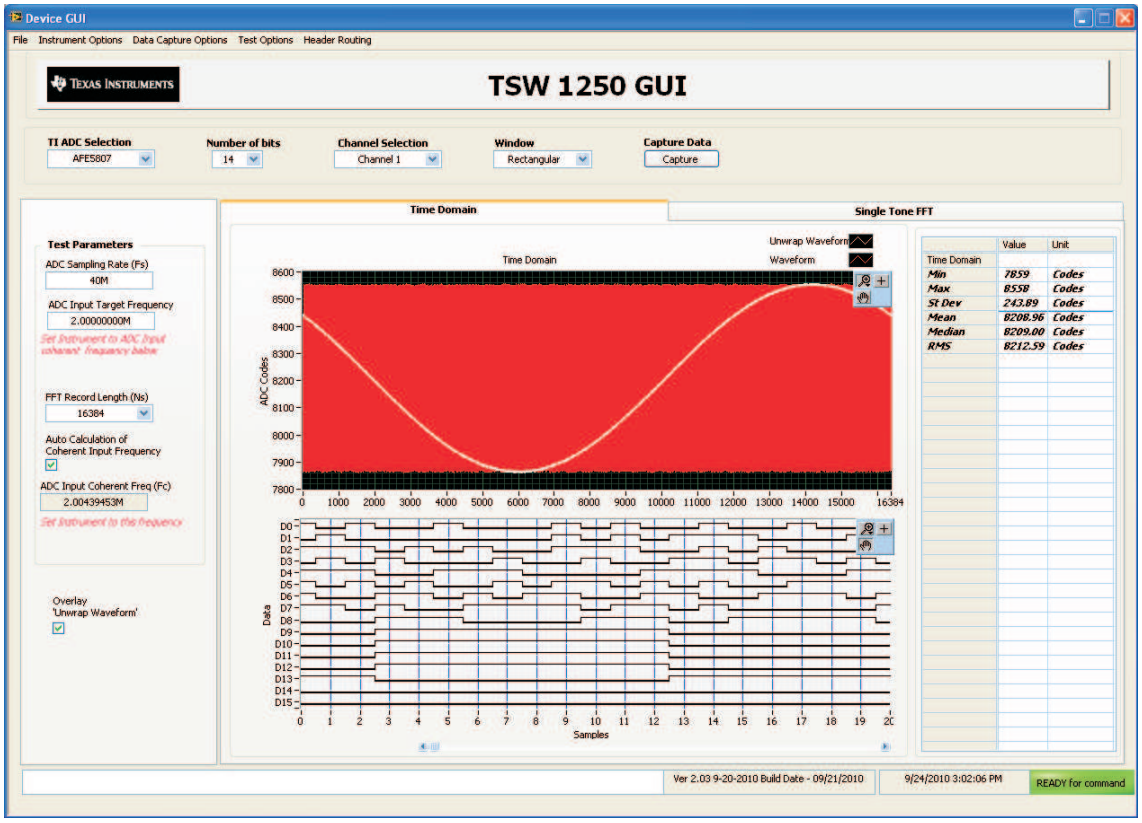


Figure 7. Time Domain Test

5.5.4 Single Tone FFT Test

The Single Tone FFT test is shown in Figure 8. The larger central pane displays the FFT power spectrum, whereas the calculated statistics are grouped into categories on the right of the screen. Settings and inputs relevant to the test are entered in drop-down menus or text input boxes on the left portion of the window.

5.5.5 FFT Power Spectrum

The FFT power spectrum of the captured data is displayed in the major center portion of the window. The TSW1250 software automatically scales the horizontal axis from DC through the Nyquist frequency, although the scale of the horizontal axis can be changed simply by highlighting the text and typing in a new value. For example, the display in Figure 8 can be used to zoom in on the input frequency by highlighting the 0MHz and typing 25M, and then highlighting the 62.5M and typing in 35M. This causes the portion of the power spectrum from 25 MHz through 35 MHz to fill the power spectrum display. The vertical scale of the power spectrum is automatically scaled to display the noise floor of the FFT result up through 0 dBFS. The vertical scale can also be manually adjusted by highlighting the limits of the vertical scale and typing in new limits.

By default, the first few harmonics of the input frequency are marked in the display, as well as an additional marker that can be placed by dragging the marker to any place in the power spectrum, such as a noise spur that is not already marked as a harmonic. By default this additional marker initially goes to the highest spur that is not identified as a harmonic.

Display properties can be edited by using the mouse to right-click in the power spectrum display. Visible properties such as the graph palette or plot legend can be edited, and auto-scale of the vertical and horizontal axises can be enabled or not.

5.5.6 Single FFT Statistics

For the Single FFT test, a number of calculated statistics and AC performance measurements are displayed to the right of the power spectrum display, grouped into several categories.

AC

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) or input frequency to the noise floor power (P_N), excluding the power at DC and the first five harmonics. SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

$$SNR = 10Log\ 10\ \frac{P_S}{P_N} \tag{1}$$

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding DC.

$$SINAD = 10Log\ 10\ \frac{P_S}{P_N + P_D} \tag{2}$$

Spurious-Free Dynamic Range (SFDR) – SFDR is ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

SFDR w/o 2,3 – Spurious-Free Dynamic Range without the second or third harmonic. Commonly, the largest spectral components after the fundamental are the second and third harmonics of the input frequency, and the input frequency can commonly contain significant power in the second and third harmonics. SFDR w/o 2,3 reports the SFDR with these two harmonics ignored.

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power in the first five harmonics (P_D). THD is typically given in data sheets in units of dBc (dB to carrier).

$$THD = 10Log\ 10\ \frac{P_S}{P_D} \tag{3}$$

Effective Number of Bits (ENOB) – The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (4)$$

Time Domain
Several of the statistics of the Time Domain test are repeated here, particularly the minimum and maximum sample values in the FFT record length, as well as the mean and standard deviation of the sample values

Signal
The frequency of the expected input signal is reported, as well as the power level of the signal in either dBc or dBFS. The amplitude of the input frequency for typical data sheet measurements is commonly set externally to be about 1 dB below Full Scale, or –1 dBFS.

Distortion
The power values for the second, third, fourth, and fifth harmonics of the input frequency and the user-selectable marker are displayed in either dBFS or dBc.

Test setup
Input parameters relevant to the test are repeated, particularly FFT record length, sample rate, and the end points of the bandwidth of integration for noise calculations. The lower end point for the bandwidth of integration is normally not zero because the first few FFT bins are not included to remove any DC biasing component of the signal.

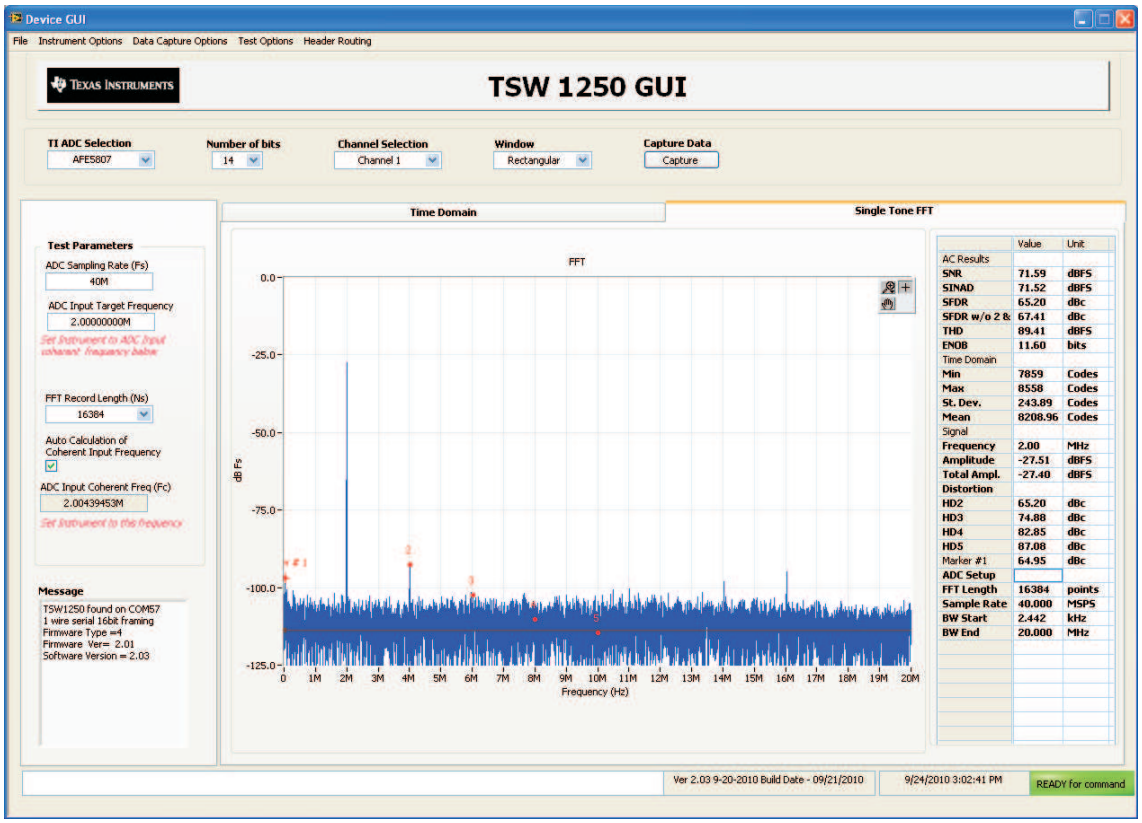


Figure 8. Single FFT Test

6 Schematics and Bill of Materials

6.1 Schematics

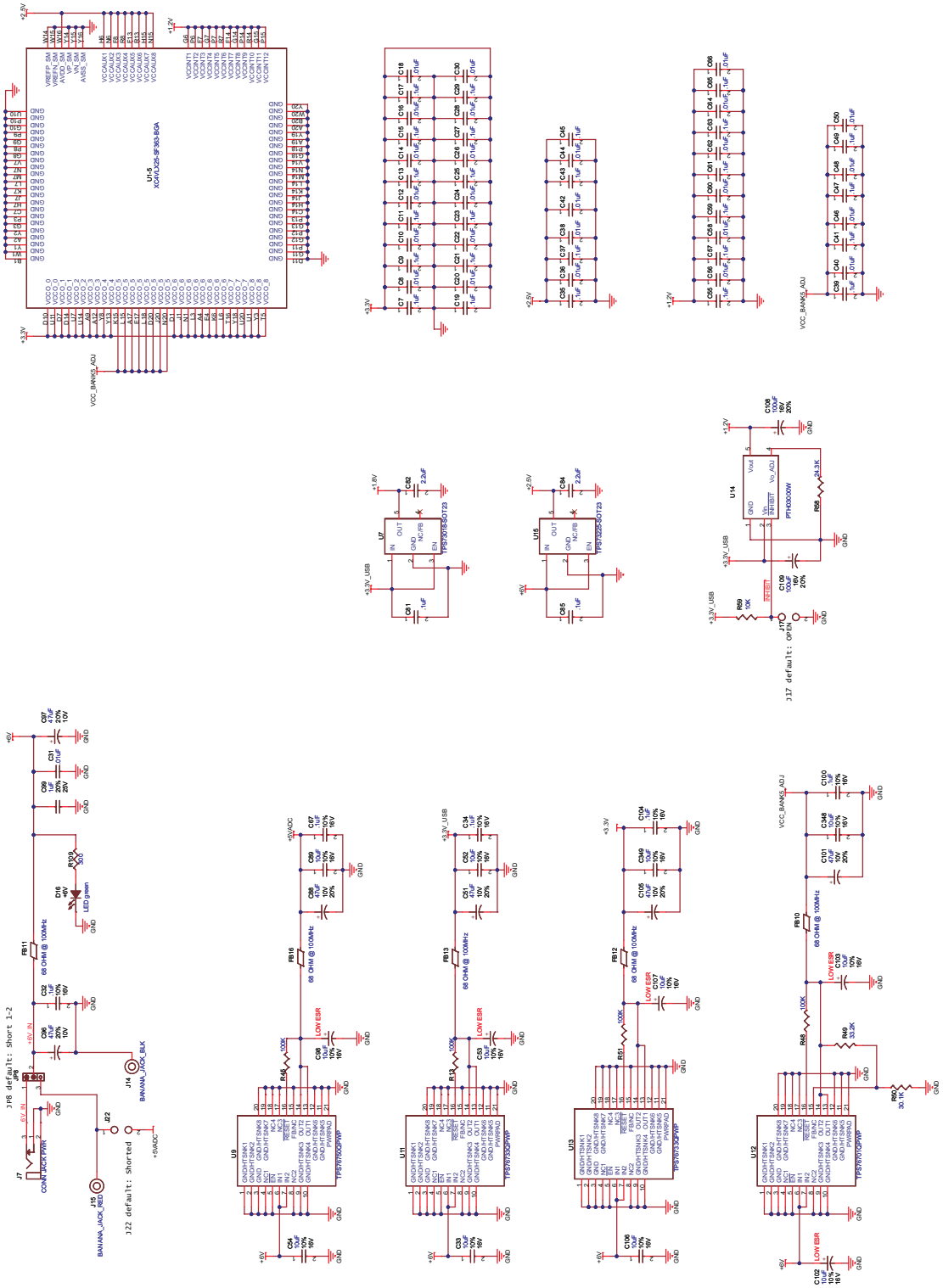


Figure 9. Schematic Diagram Page 1

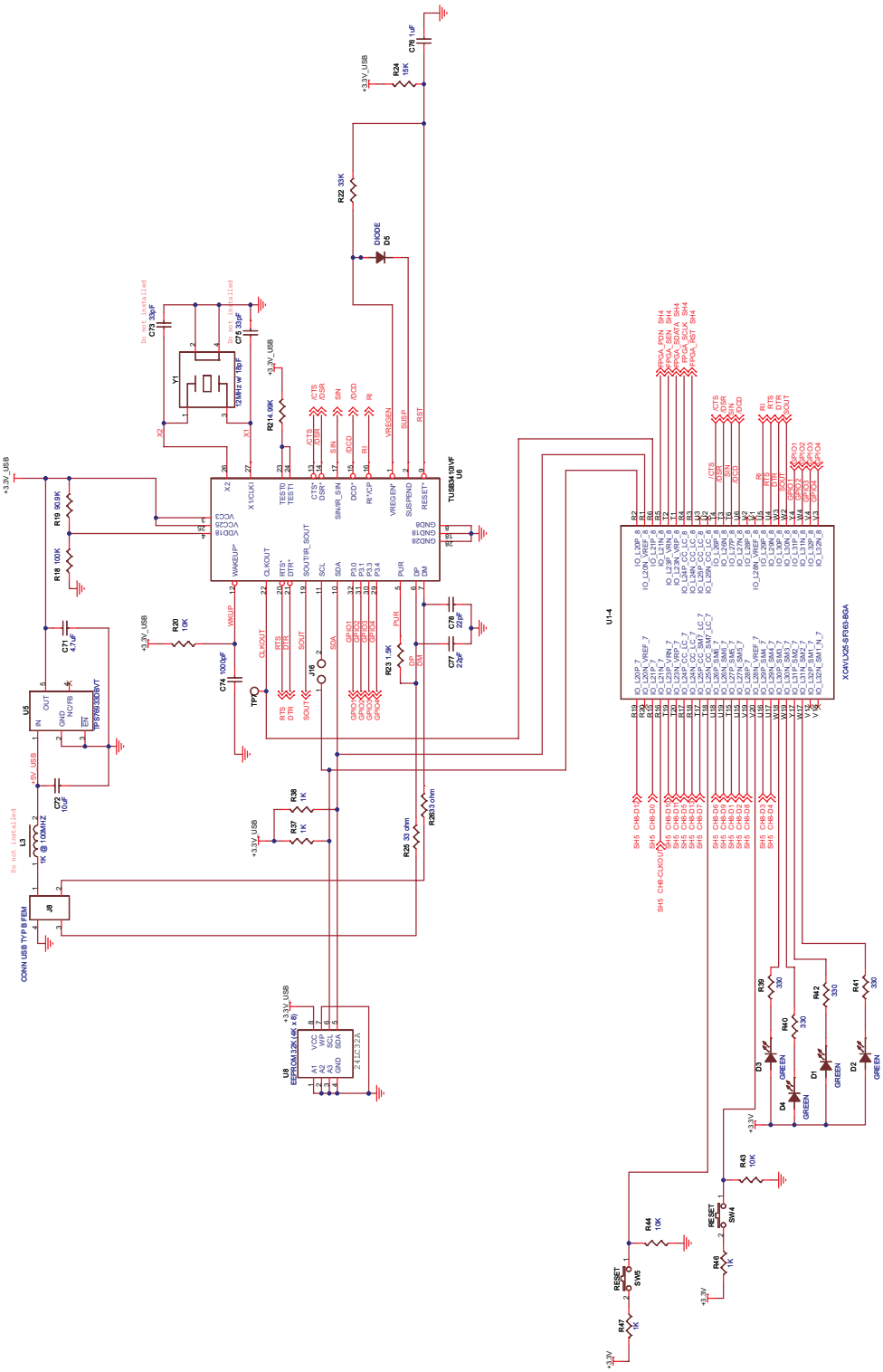


Figure 10. Schematic Diagram Page 2

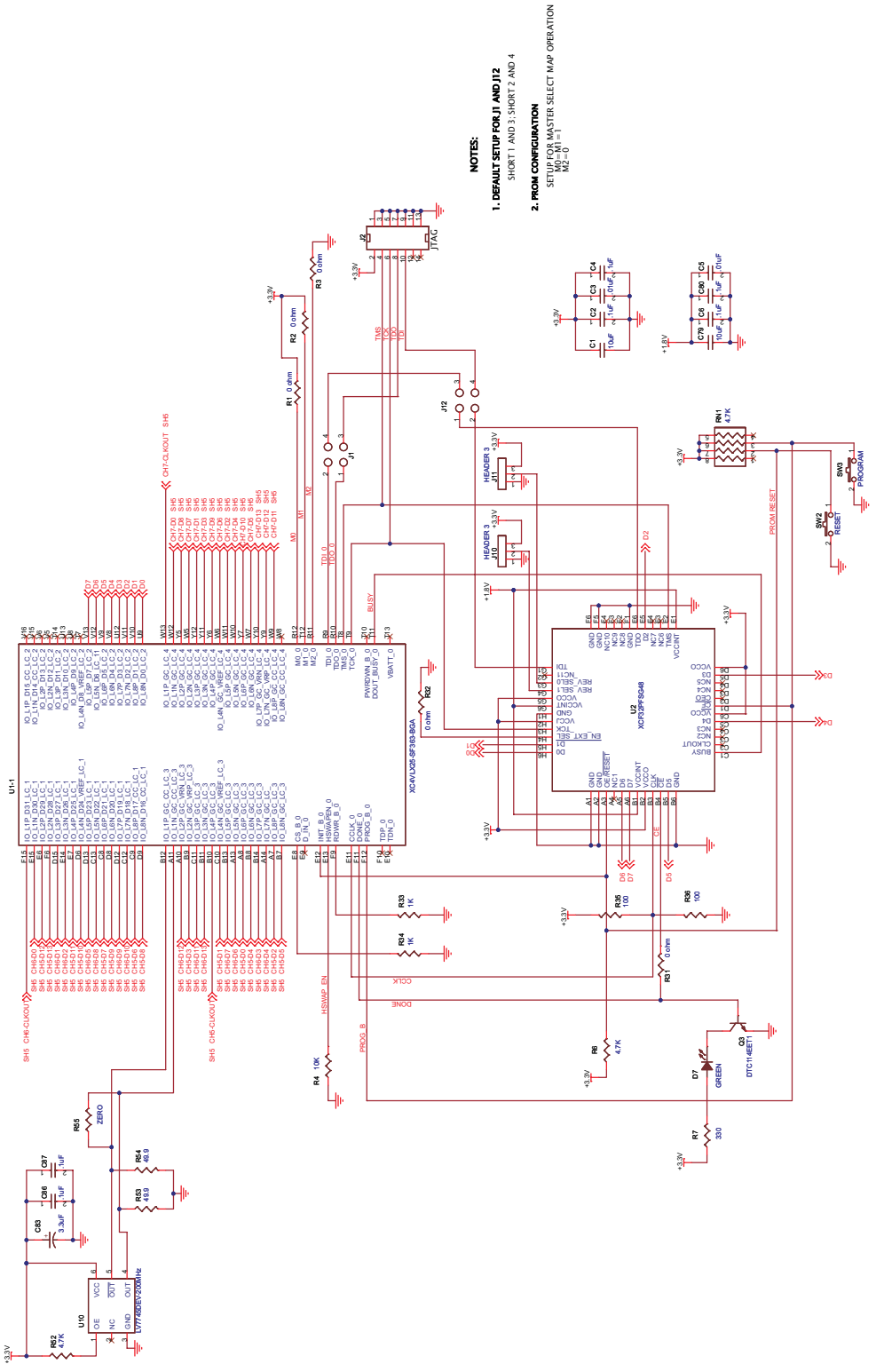


Figure 11. Schematic Diagram Page 3

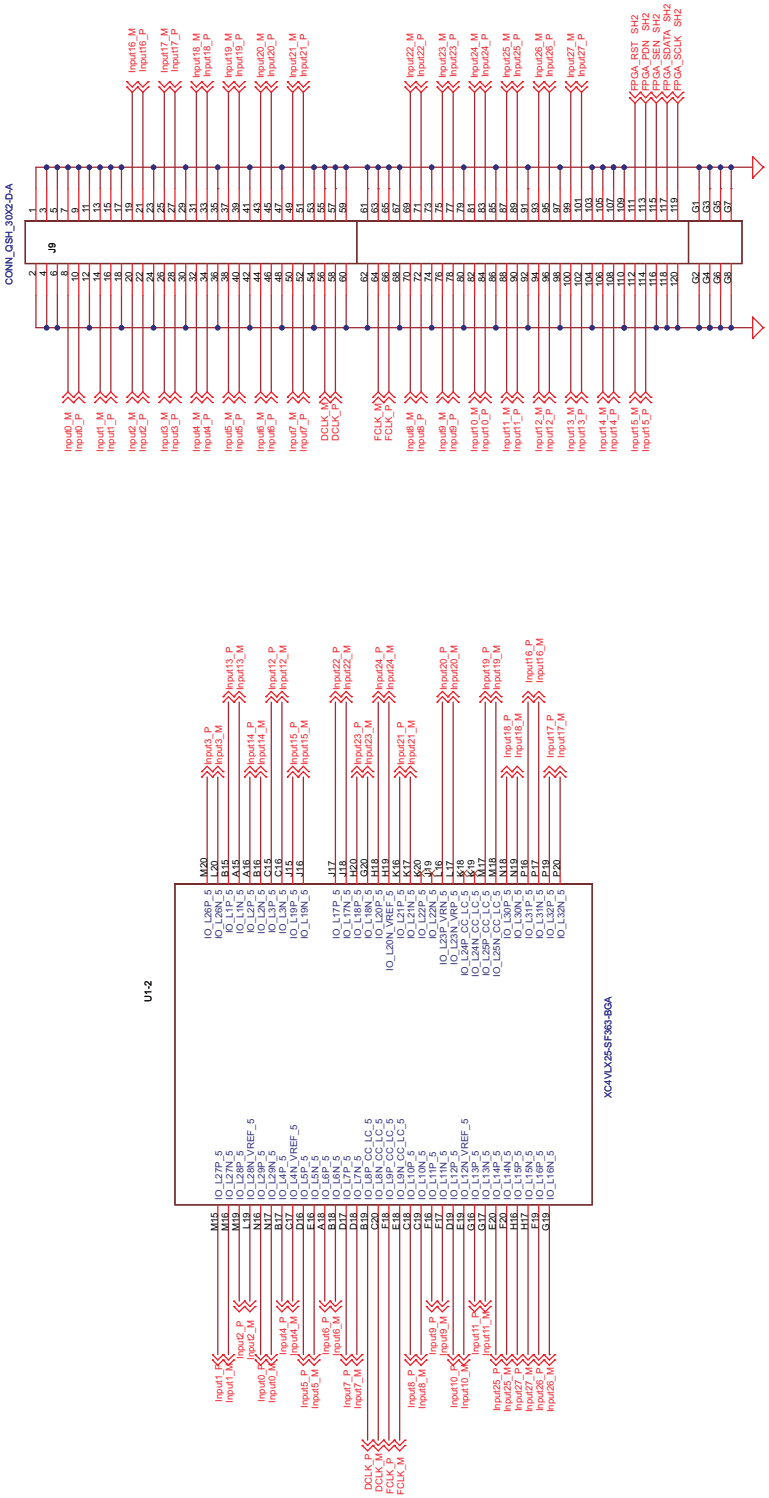


Figure 12. Schematic Diagram Page 4

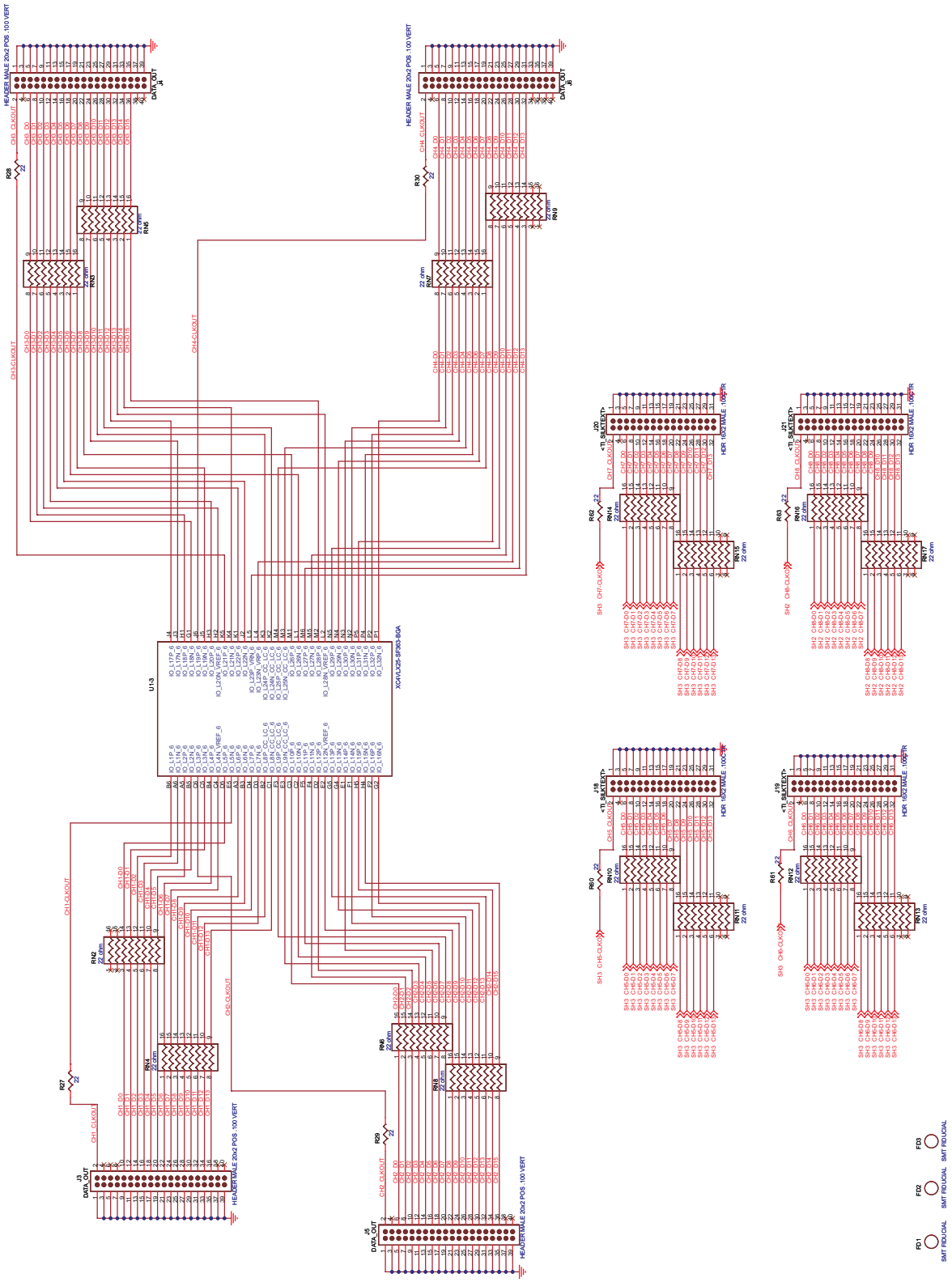


Figure 13. Schematic Diagram Page 5

6.2 Bill of Materials

Table 1. Bill of Materials

TSW1200EVM BOM – Revision: C									
QTY	Reference	Not Installed	Part	Foot Print	Part Number	Manufacturer	Tol	Volt	Wat
3	C1, C72, C79		10 µF	603	ECJ-1VB0J106M	Panasonic	20%	6.3V	
4	C2, C4, C6, C80		0.1uF	603	GRM188R71H104KA93D	Murata	5%	50V	
2	C3, C5		0.01 µF	603	C0603C103K5RACTU	Kemet	10%	50V	
26	C7, C9, C11, C13, C15, C17, C19, C21, C23, C25, C27, C29, C35, C37, C39, C41, C43, C45, C47, C49, C55, C57, C59, C61, C63, C65		0.1 µF	201	ECJ-ZEBFJ104K	Panasonic	5%	50V	
26	C8, C10, C12, C14, C16, C18, C20, C22, C24, C26, C28, C30, C36, C38, C40, C42, C44, C46, C48, C50, C56, C58, C60, C62, C64, C66		0.01 µF	201	ECJ-ZEB1A103K	Panasonic	5%	50V	
1	C31		0.01 µF	402	ECJ-0EB1E103K	Panasonic	10%	25V	
1	C32		0.1 µF	402	ECJ-0EB1C104K	Panasonic	10%	16V	
11	C33, C52, C53, C89, C98, C102, C103, C106, C107, C348, C349		10 µF	1206	Panasonic ECJ-3YB1C106K		10%	16V	
4	C34, C67, C100, C104		0.1 µF	402	Panasonic ECJ-0EB1C104K		10%	16V	
5	C51, C88, C96, C101, C105		47 µF	tant_b	Kemet T494B476M010AS		20%	10V	
1	C54		10 µF	1206	ECJ-3YB1C106K	Panasonic	10%	16V	
1	C71		4.7 µF	603	GRM188F51A475ZE20D	Murata	0.6	10V	
0	C73, C75	NOT INSTALLED	33 pF	603	GRM1885C2A330JA01D	Murata	5%	100V	
1	C74		1000 pF	603	ECJ-1VB1H102K	Panasonic	10%	50V	
1	C76		1 µF	603	ECJ-1VB1A105K	Panasonic	10%	10V	
2	C77, C78		22 pF	603	GRM1885C2A220JA01D	Murata	5%	100V	
2	C81, C85		0.1 µF	603	ECJ-1VB1H104K	Panasonic	10%	50V	
2	C82, C84		2.2 µF	603	ECJ-1VB1A225K	Panasonic	10%	10V	
1	C83		3.3 µF	TANT_B	TAJB335K016R	AVX	10%	16V	
2	C86, C87		0.1 µF	603	GRM188R71H104KA93D	Murata	10%	50V	
1	C97		47 µF	tant_b	T494B476M010AS	Kemet	20%	10V	
1	C99		1 µF	603	ECJ-1V41E105M	Panasonic	20%	25V	
2	C108, C109		100 µF	smd_cap_elec_TCE	EEE-TG1C101P	Panasonic	20%	16V	
5	D1–D4, D7		GREEN	diode_0805	DC1112H-TR	Stanley			
1	D5		DIODE	SOT23_DIODE	BAS21TA	Zetec Inc.			
1	D16		LED green	LED_0805	LNJ306G5UUX	Panasonic			
5	FB10–FB13, FB16		68 Ω at 100MHz	1206	EXC-ML32A680U	Panasonic	Short pins 1-2 with shunt connector DigiKey # S9000-ND		
1	JP8		HEADER 3POS 0.1 CTR	JUMPER3	HTSW-103-07-F-S	Samtec	Short pins with shunt connector DigiKey # S9000-ND (as shown on silkscreen)		
2	J1, J12		HEADER 2×2	hdr2X2_100ctr_alt	90131-0122	Molex			
1	J2		CONN 7×2	CON_2X7_2mm_M	87831-1420	Molex			
4	J3–J6		HEADER MALE 20×2 POS 0.100 VERT	CON20X2_100ctr_M_tsw1100_mate	HTSW-120-07-L-D	Samtec			
1	J7		CONN JACK PWR	PWRJACK	RAPC722	Switchcraft			
1	J8		CONN USB TYP B FEM	conn_usb_typb_fem	897-43-004-90-000	Milmax			
1	J9		CONN_QSH_30×2-D-A	conn_QSH_30X2-D-A	QSH-060-01-F-D-A	Samtec			
2	J10, J11		HEADER 3	jumper3	22-28-4030	Molex	Short pins 1-2 with shunt connector DigiKey # S9000-ND		

Table 1. Bill of Materials (continued)

TSW1200EVM BOM – Revision: C									
QTY	Reference	Not Installed	Part	Foot Print	Part Number	Manufacturer	Tol	Volt	Wat
1	J14		BANANA_JACK_BLK	banana_jack	ST-351B BLK	Alectron Connectors			
1	J15		BANANA_JACK_RED	banana_jack	ST-351B RED	Alectron Connectors			
2	J16, J22		HEADER 2	JUMPER2	22-28-4020	Molex	Short pins with shunt connector DigiKey # S9000-ND		
1	J17		HEADER 2	JUMPER2	22-28-4020	Molex			
4	J18–J21		HDR 16×2 MALE 0.100CTR	CON16X2_100ctr_M_alt	TSW-116-07-L-D	Samtec			
0	L3	NOT INSTALLED	1K at 100 MHz	smd_0805	BLM21AG102SN1D	Murata			
1	Q3		DTC114EET1	sc75	DTC114EET1	ON SEMI			
1	RN1		4.7K	RNET4_8_0603	EXB-V8V472JV	Panasonic	5%		
16	RN2, RN17		22 Ω	rnet8_16_0603	742C163220JTR	CTS	5%		.063W
5	R1–R3, R31, R32		0 Ω	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
5	R4, R20, R43, R44, R59		10K	603	ERJ-3EKF1002V	Panasonic	1%		1/10W
1	R6		4.7K	603	ERJ-3GEYJ472V	Panasonic	5%		1/10W
5	R7, R39–R42		330	603	RC0603FR-07330RL	Yageo			
3	R13, R48, R51		100K	603	ERJ-3EKF1003V	Panasonic	1%	1/10W	
1	R18		100K	603	ERJ-3EKF1003V	Panasonic	1%		1/10W
1	R19		90.9K	603	ERJ-3EKF9092V	Panasonic	1%		1/10W
1	R21		4.99K	603	ERJ-3EKF4991V	Panasonic	1%		1/10W
1	R22		33K	603	RC0603FR-0733KL	Yageo	1%		1/10W
1	R23		1.5K	603	ERJ-3EKF1501V	Panasonic	1%		1/10W
1	R24		15K	603	ERJ-3EKF1502V	Panasonic	1%		1/10W
2	R25, R26		33 Ω	603	RC0603FR-0733RL	Yageo	1%		1/10W
8	R27–R30, R60–R63		22	603	RC0603FR-0722RL	Yageo	1%		1/10W
6	R33, R34, R37, R38, R46, R47		1K	603	ERJ-3EKF1001V	Panasonic	1%		1/10W
2	R35, R36		100	603	ERJ-3EKF1000V	Panasonic	1%		1/10W
1	R45		100K	603	ERJ-3EKF1003V	Panasonic	1%	1/10W	
1	R49		33.2K	603	ERJ-3EKF3322V	Panasonic	1%	1/10W	
1	R50		30.1K	603	ERJ-3EKF3012V	Panasonic	1%	1/10W	
1	R52		4.7K	603	ERA-V15J472V	Panasonic	5%		1/16W
2	R53, R54		49.9	603	ERJ-3EKF49R9V	Panasonic	1%		1/10W
0	R55	NOT INSTALLED	ZERO	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
1	R58		24.3K	603	ERJ-3EKF2432V	Panasonic	1%	1/10W	
1	R109		300	603	ERJ-3EKF3000V	Panasonic			
1	SW2		RESET	SW_RESET_PTS635	PTS635SL43	ITT Industries/C&K Div			
3	SW3–SW5		PROGRAM	SW_RESET_PTS635	PTS635SL43	ITT Industries/C&K Div			
1	TP7		T POINT R	testpoint	5002	Keystone			
1	U1		XC4VLX25-SF363-BGA	MBGA_PT8MM_363	XC4VLX25-SF363-11-BGA	Xilinx			TI Provide
1	U2		XCF16P/FSG48	MBGA_FS48_PT8MM	XCF16PFSG48	Xilinx			TI Provide
1	U5		TPS76933DBVT	dbv5	TPS76933DBVT	TI			TI Provide
1	U6A		TUSB3410IVF	pqfp32	TUSB3410IVF	TI			TI Provide
1	U7		TPS73018-SOT23	DBV5	TPS73018DBVT	TI			TI Provide
1	U8		EEPROM 32K (4K x 8)	DIP8_3	24LC32A-I/P	Microchip			
1	XU8		Socket, dip 8	DIP8_3	ED58083-ND	DigiKey			
1	U9		TPS76750QPWP	HTSSOP_20_260x177_26_pwrpad	TPS76750QPWP	TI			TI Provide
1	U10		LV7745DEV-200MHz	SMD_XTAL_7X5MM_6PIN	LV7745DEV-200MHz	PLETRONICS			
2	U11, U13		TPS76733QPWP	HTSSOP_20_260x177_26_pwrpad	TPS76733QPWP	TI			TI Provide

Table 1. Bill of Materials (continued)

TSW1200EVM BOM – Revision: C									
QTY	Reference	Not Installed	Part	Foot Print	Part Number	Manufacturer	Tol	Volt	Wat
1	U12		TPS76701QPWP	HTSSOP_20_260x177_26_pwrpad	TPS76701QPWP	TI			TI Provide
1	U14		PTH03000W	SMD_PWRMOD_EUT5	PTH03000WAS	TI			TI Provide
1	U15		TPS73225-SOT23	DBV5	TPS73225DBVT	TI			TI Provide
1	Y1		12MHz w/ 18pF	smd_xtal_AMB3B	ABM3B-12.000MHZ-10-1-U-T	Abracon			
4			SCREW 4-40 X 3/8"		PMS 440 0038 PH	Building Fasteners	PCB legs		
4			STANDOFF RD 4-40THR .875" ALUM		1846	Keystone			

7 Circuit Board Layout and Layer Stackup

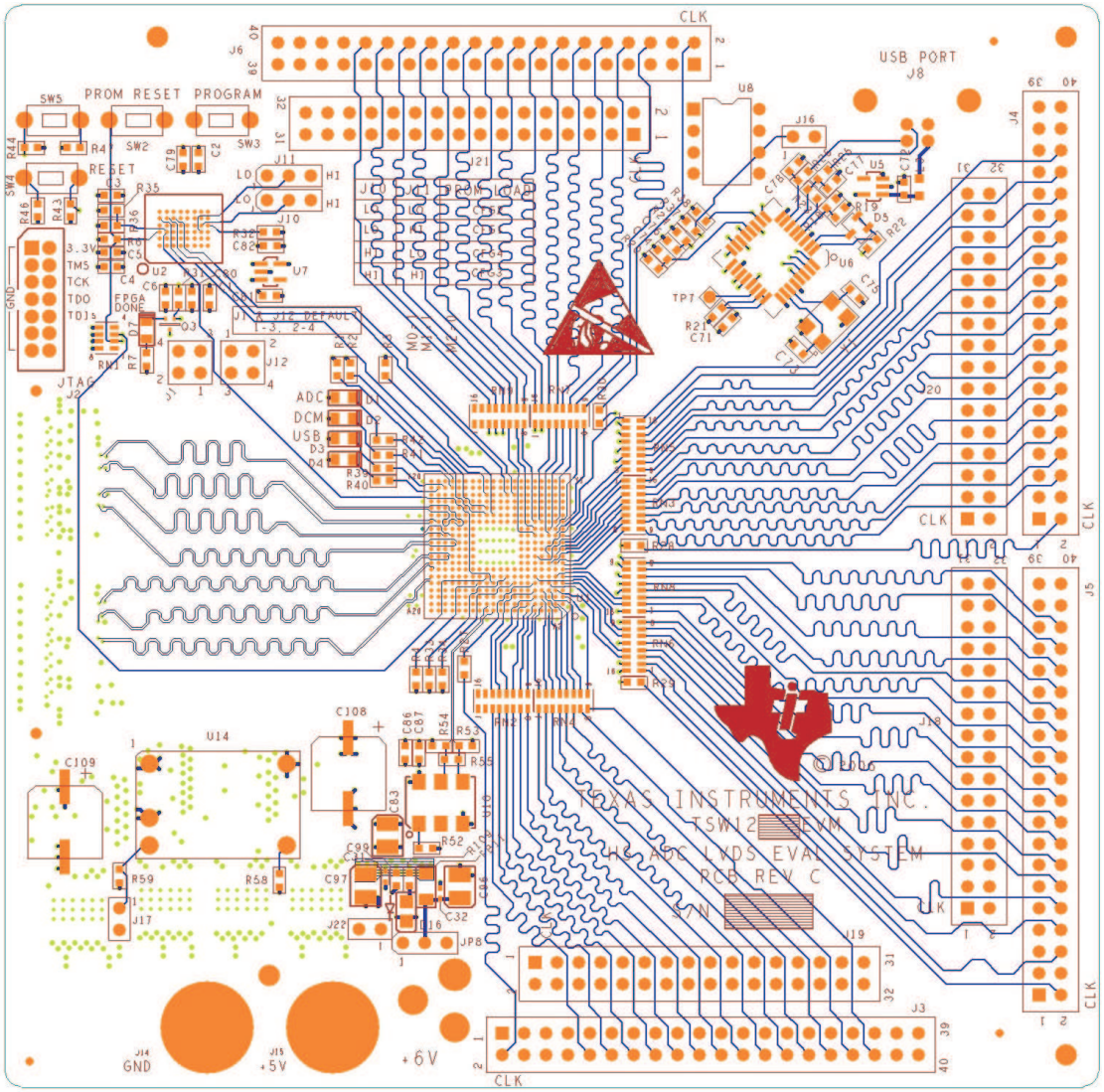


Figure 14. TSW1250C Layout Top Layer – Signal

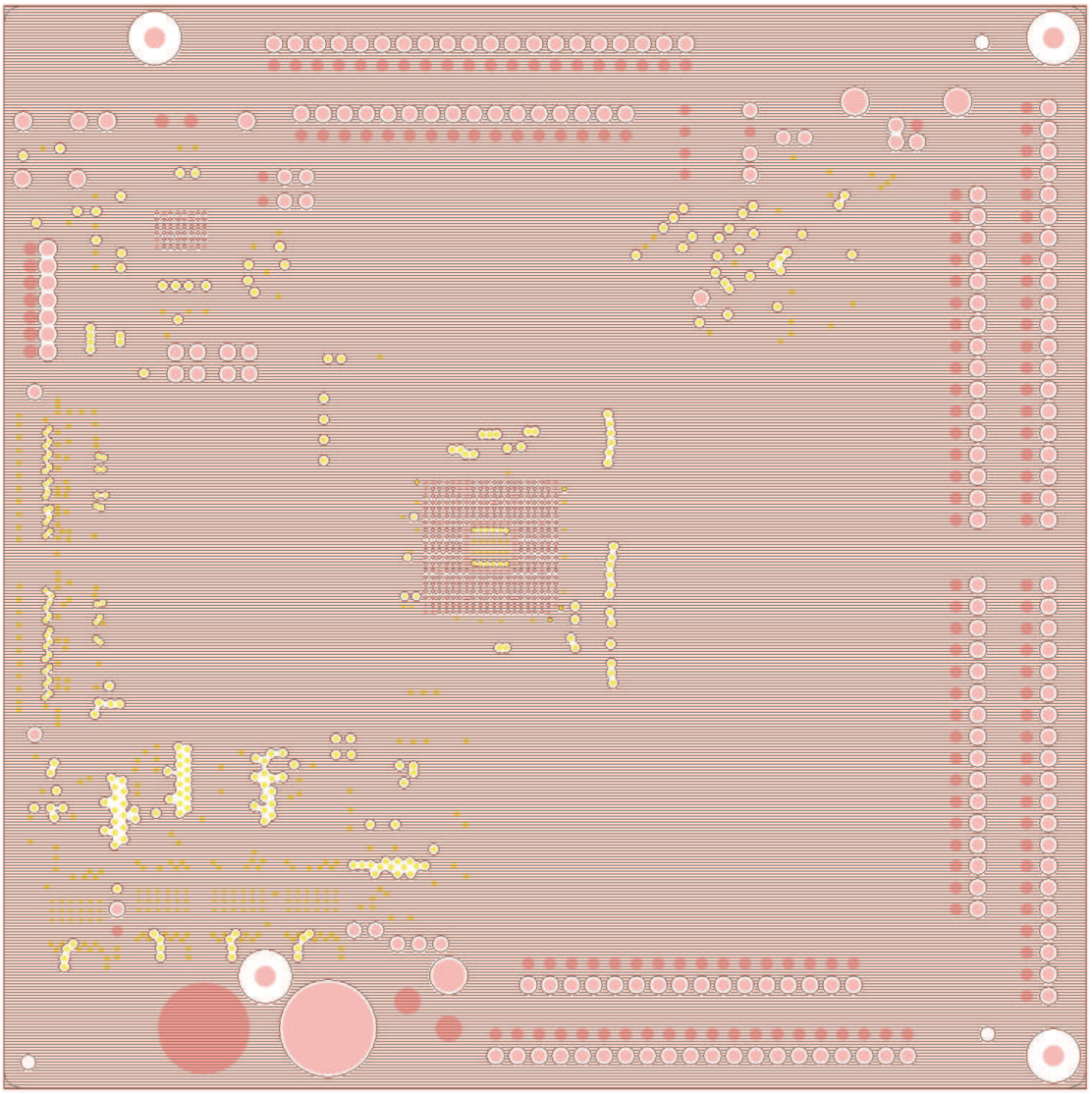


Figure 15. TSW1250C Layout Layer Two – GND1

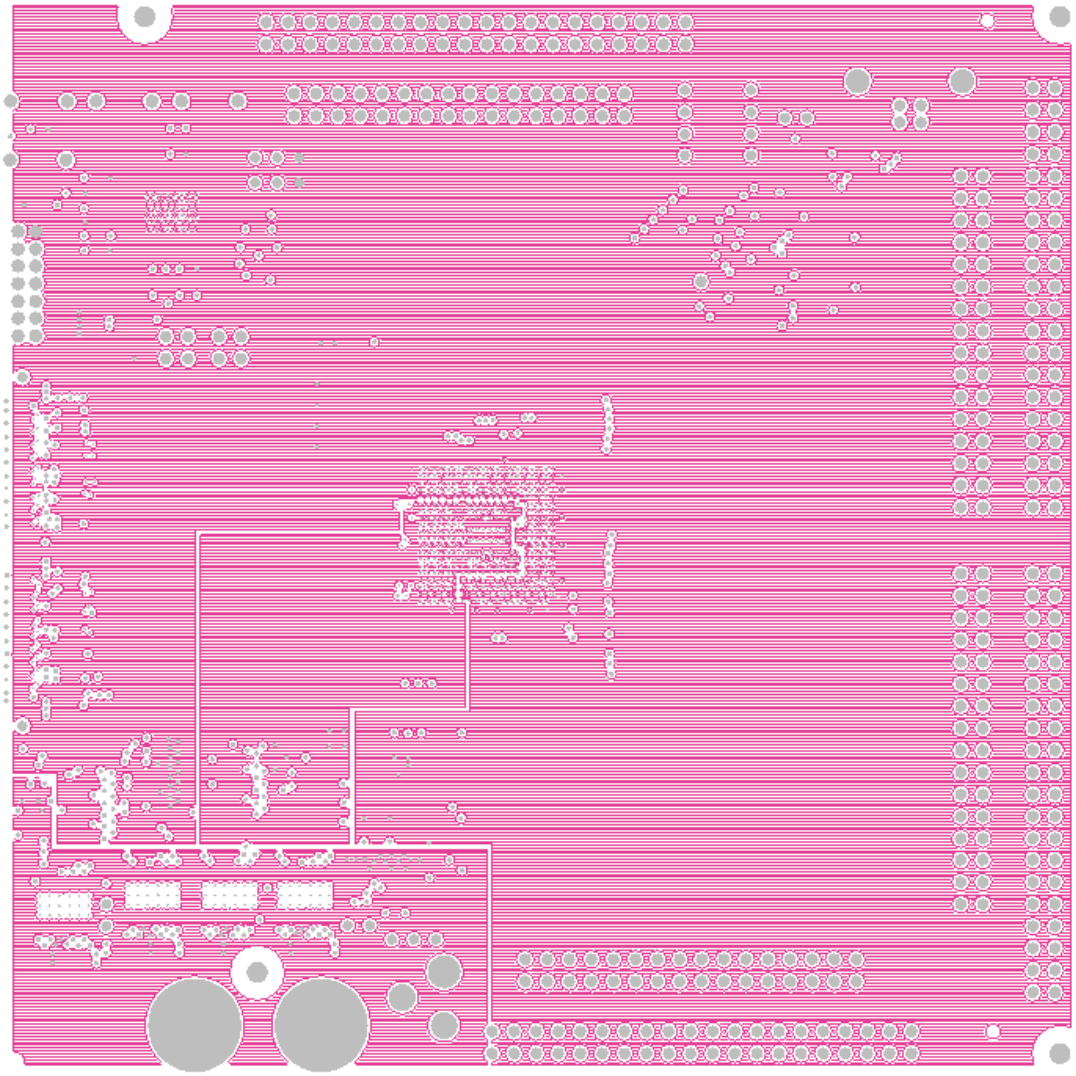


Figure 16. TSW1250C Layout Layer 3 – PWR1

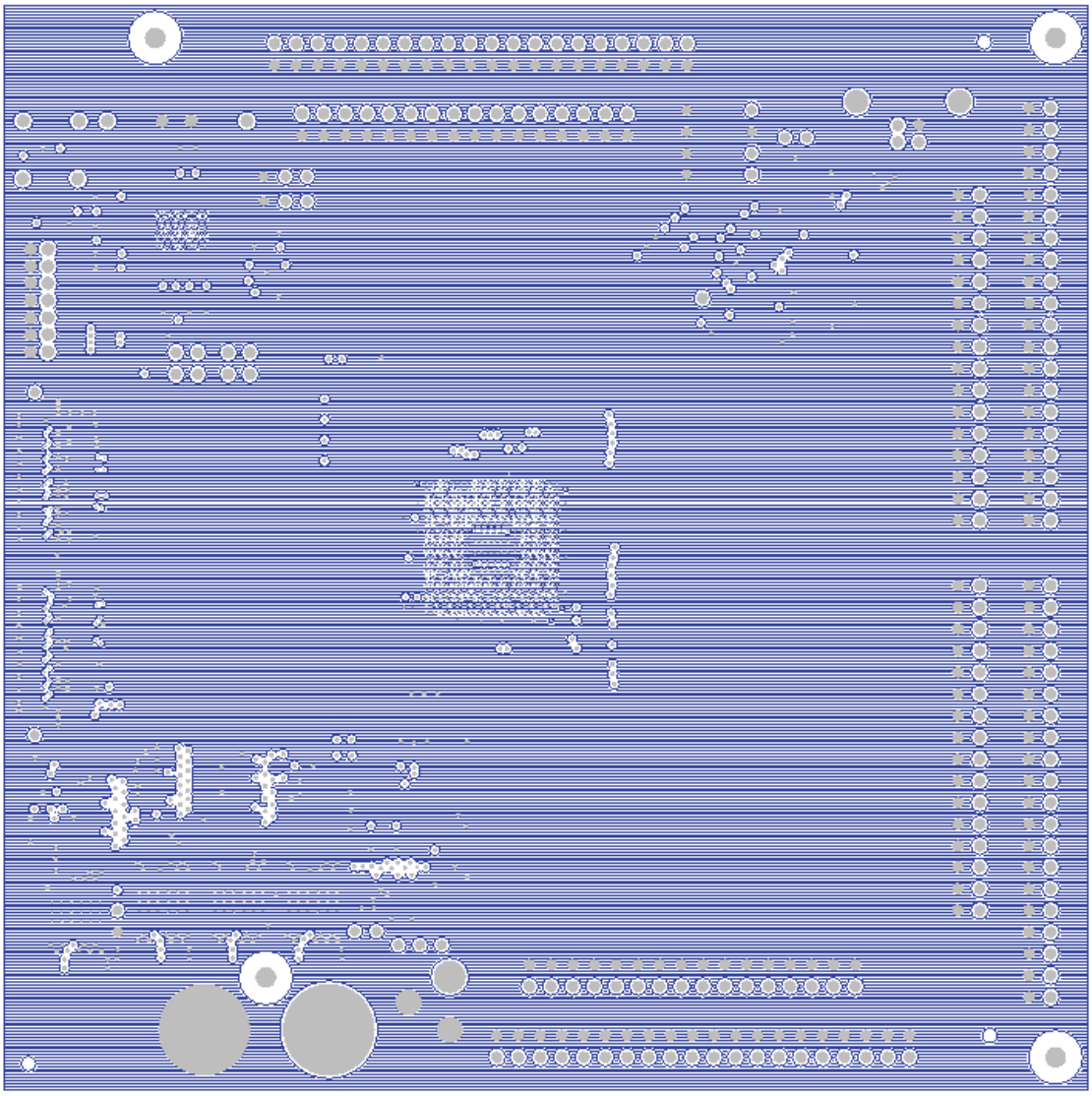


Figure 17. TSW1250C Layout Layer 4 – GND2

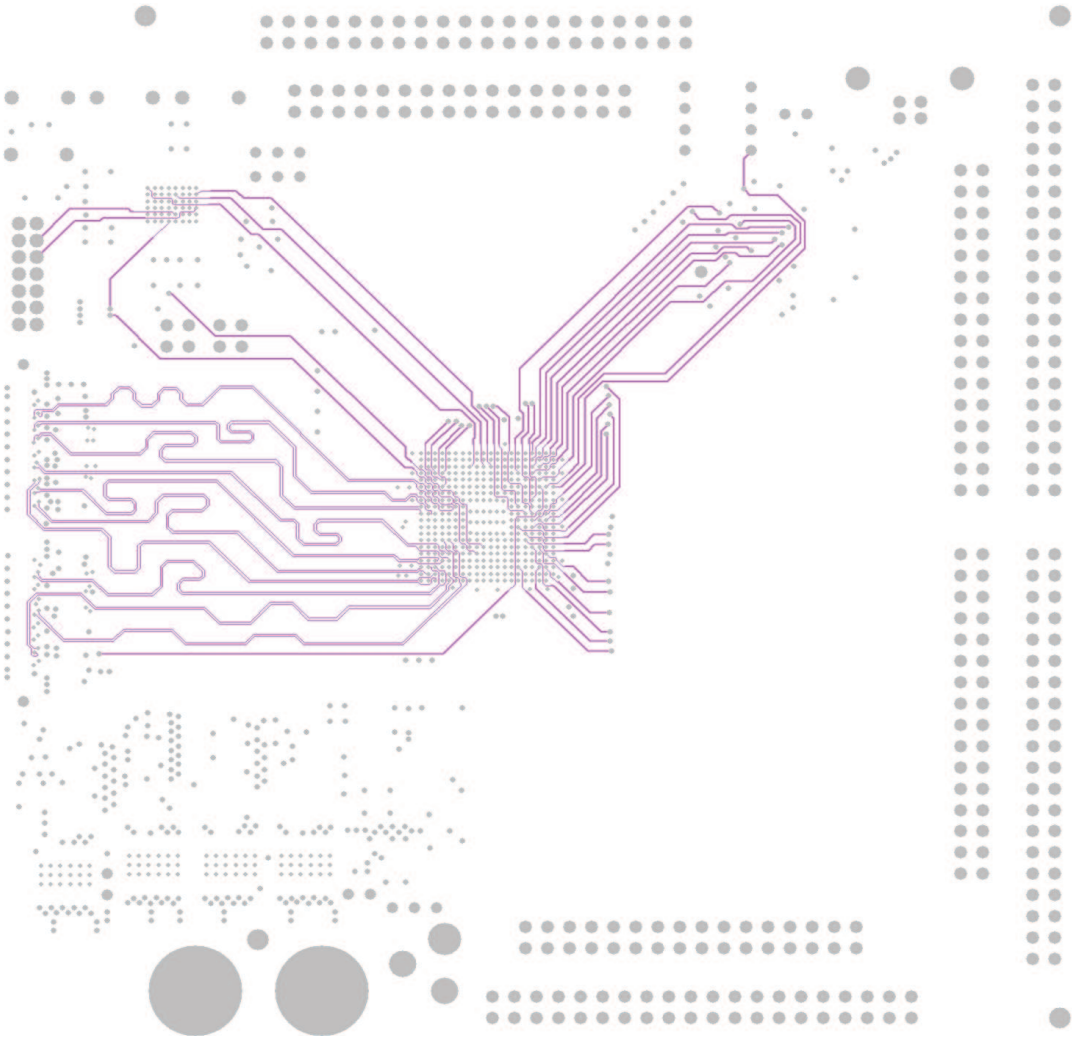


Figure 18. TSW1250C Layout Layer 5 – Signal

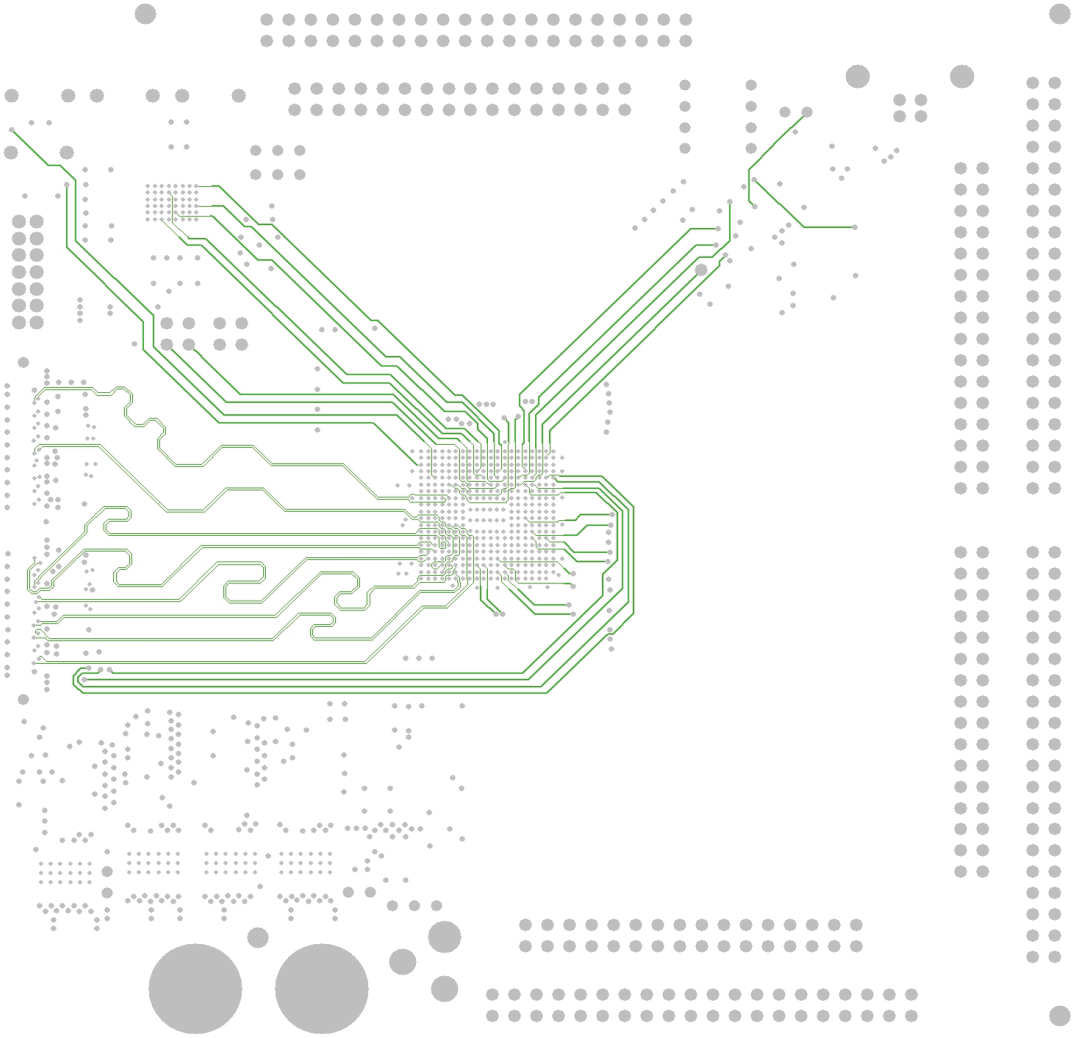


Figure 19. TSW1250C Layout Layer 6 – Signal

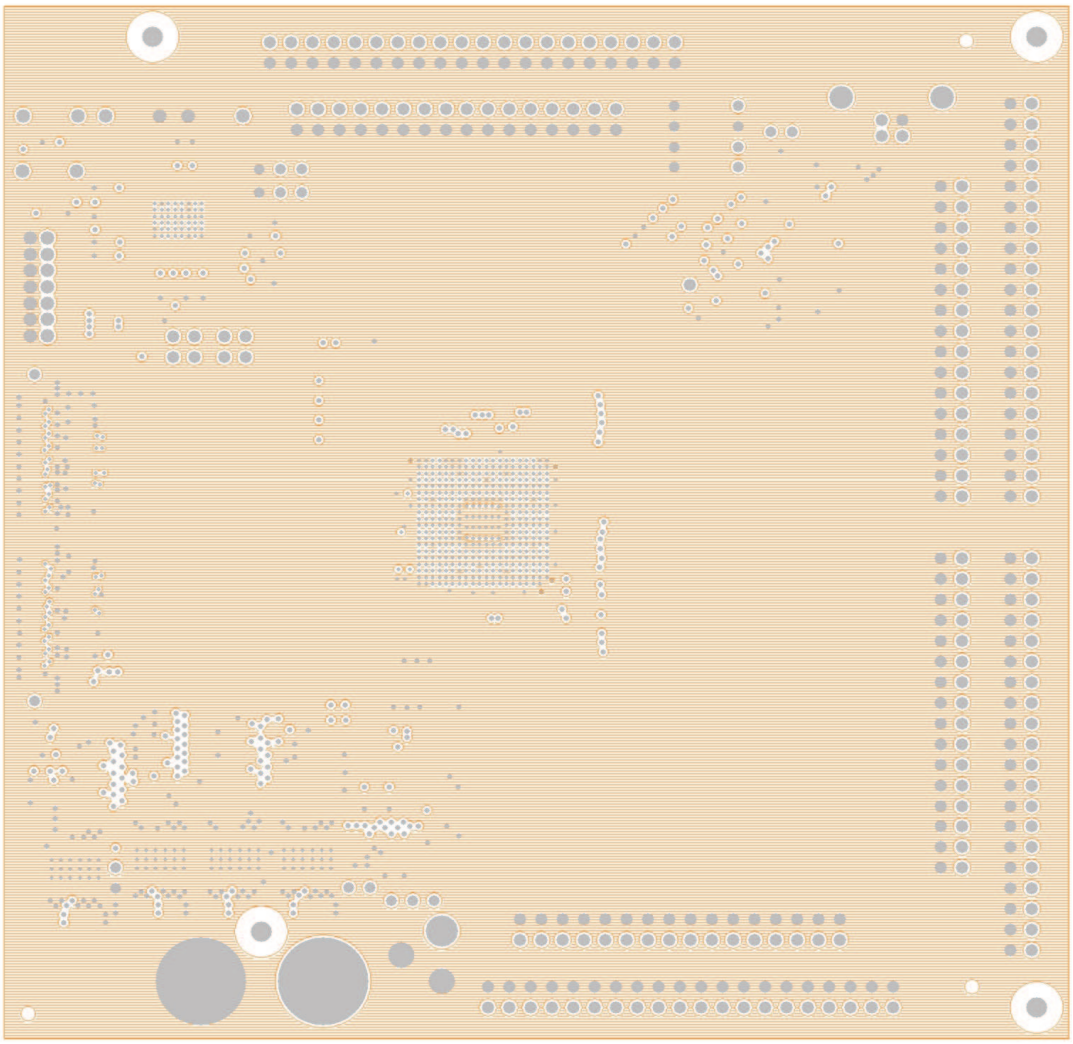


Figure 20. TSW1250C Layout Layer 7 – GND3

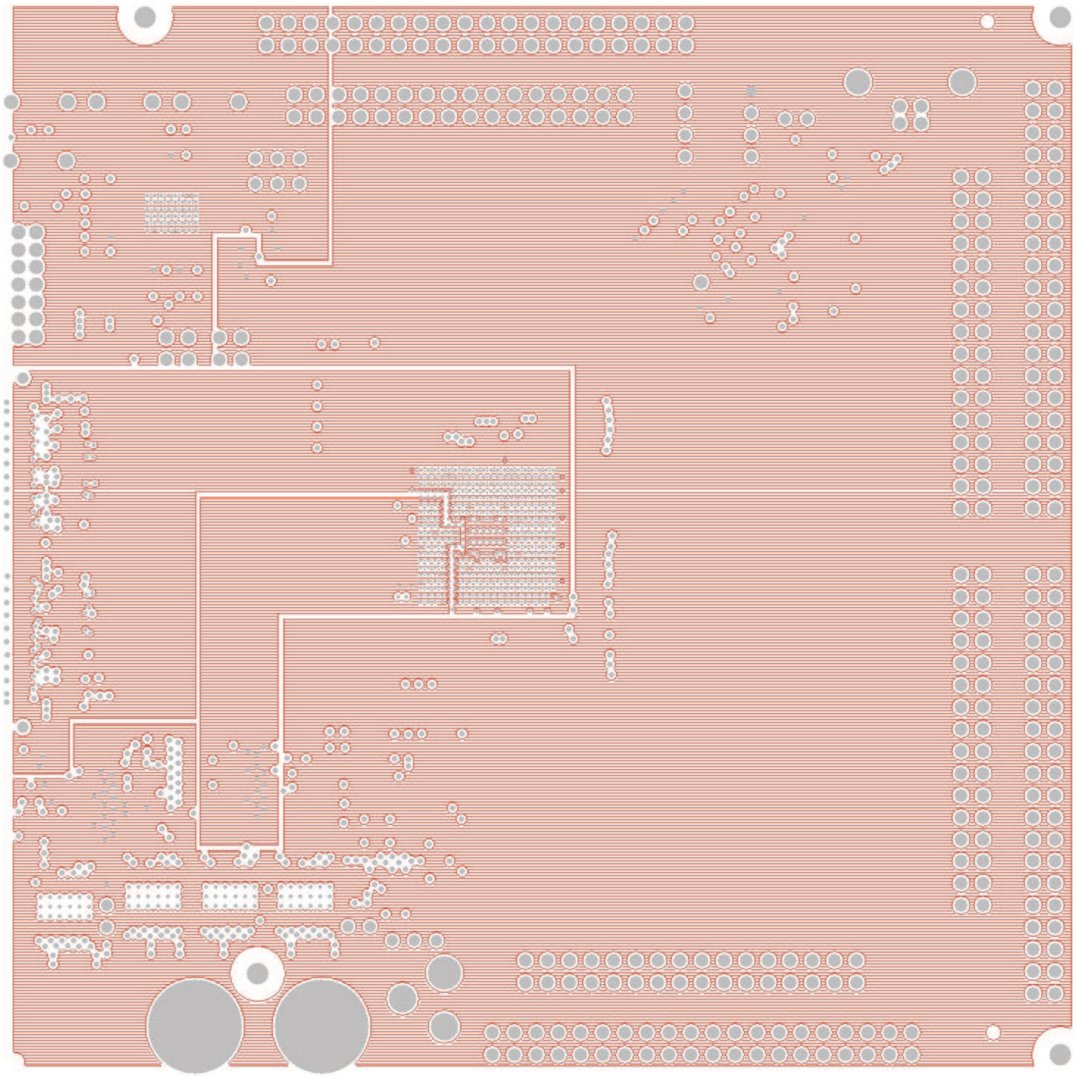


Figure 21. TSW1250C Layout Layer 8 – PWR2

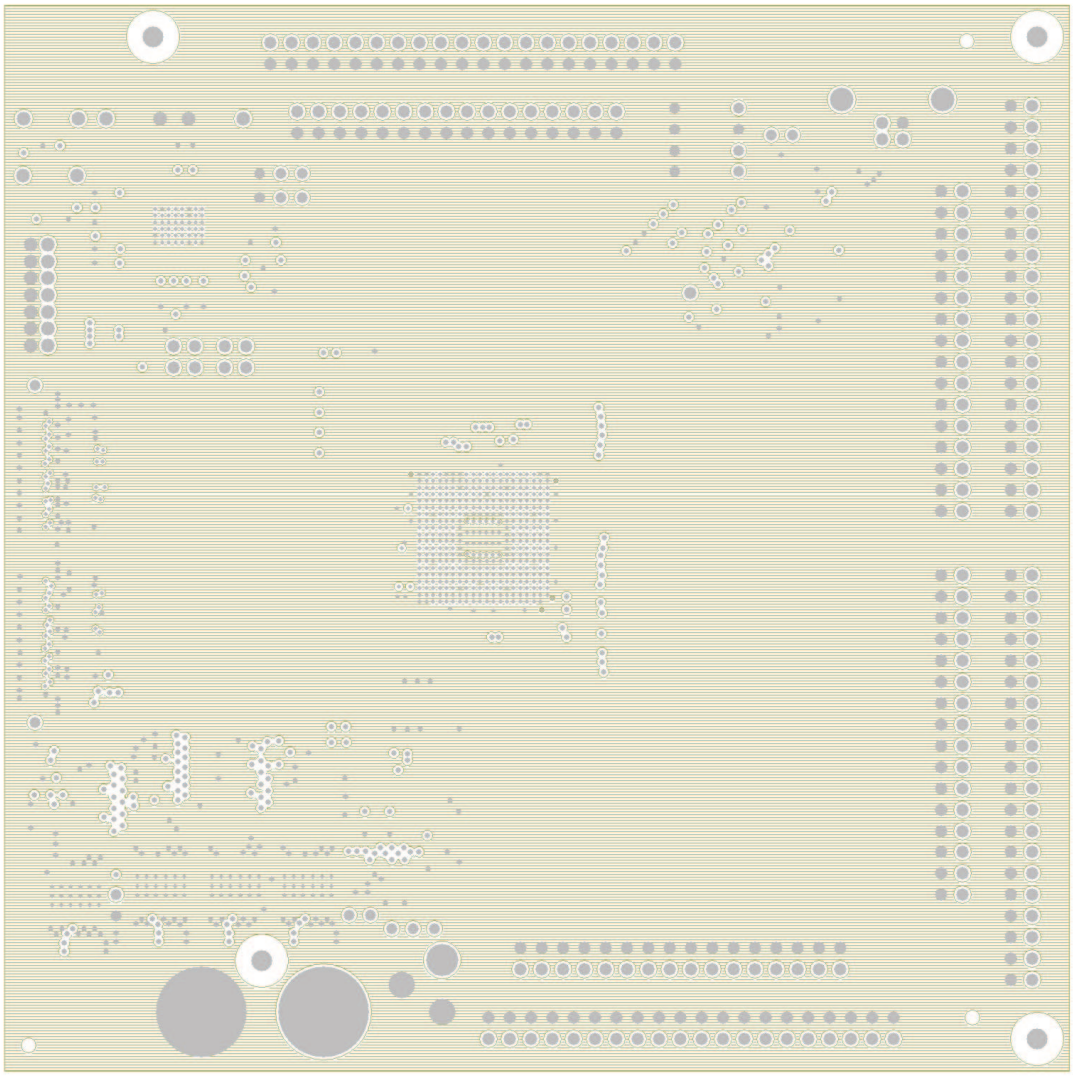


Figure 22. TSW1250C Layer 9 – GND4

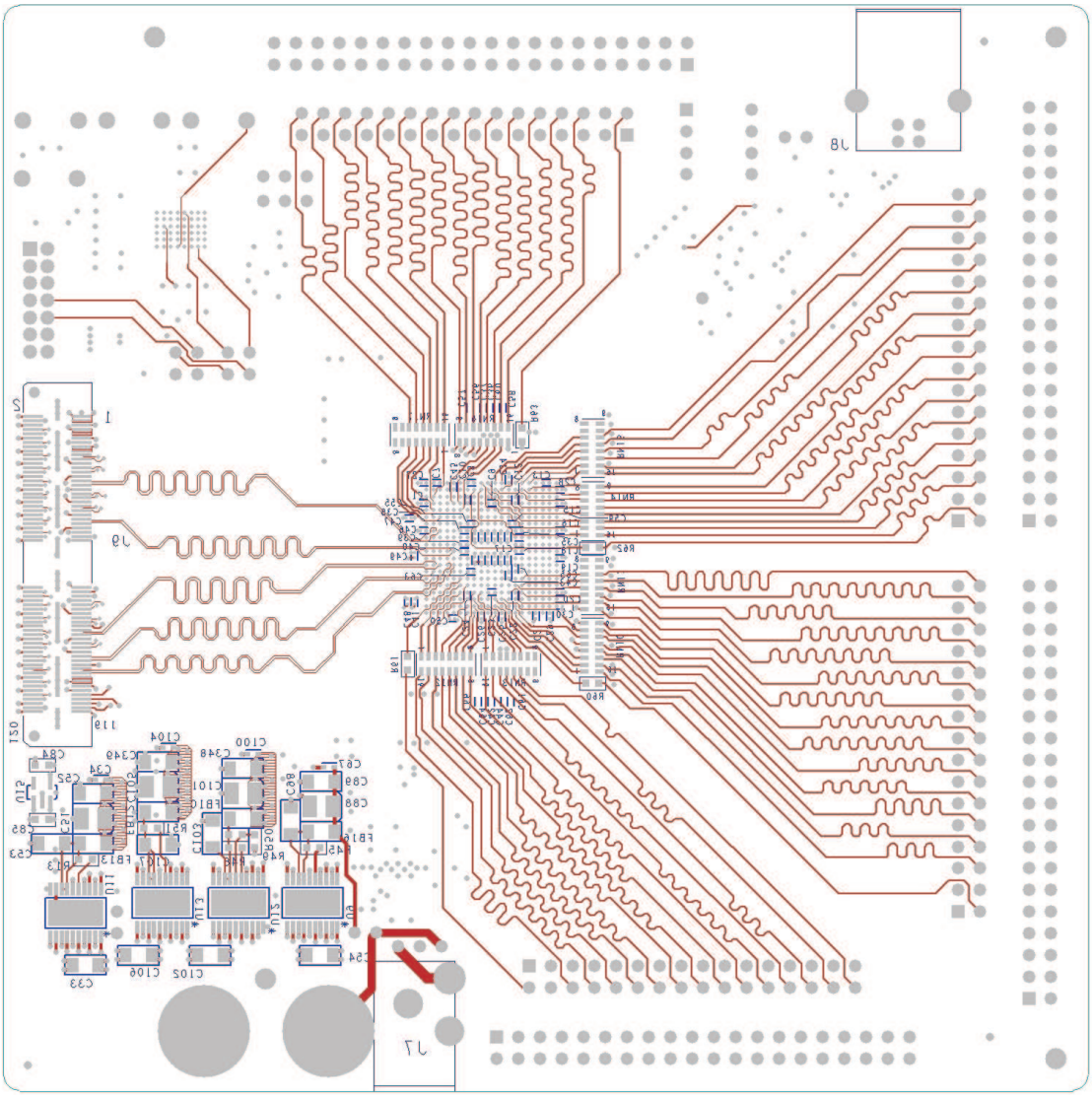
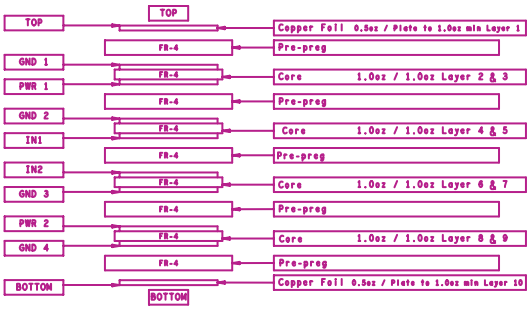
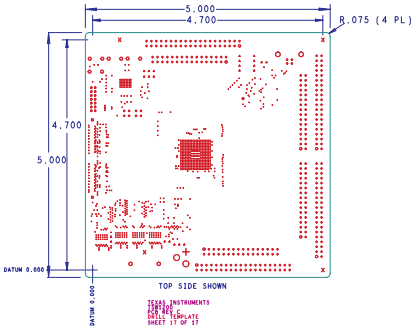


Figure 23. TSW1250C Bottom Layer – Signal



UNLESS OTHERWISE SPECIFIED, ALL NOTES ARE APPLICABLE.
NOTES PRECEDED BY AN UNMARKED '☐' ARE NOT APPLICABLE.

1. APPLICATION DESIGN, MANUFACTURING AND INSPECTION DOCUMENTS.
   IPC-2221A & IPC-2222 / DESIGN STANDARD FOR RIGID PRINTED CIRCUIT BOARDS AND RIGID PRINTED BOARD ASSEMBLIES.
   IPC-6012B / QUALIFICATION AND PERFORMANCE SPECIFICATION FOR RIGID PRINTED BOARD.
   IPC-A-600G / ACCEPTABILITY OF PRINTED BOARDS.
2. HOLE SIZE APPLY AFTER PLATING. TOLERANCE TO BE +/-.003.
3. REGISTRATION TOLERANCE: ARTWORK +/-.002
   ALL HOLE CENTERS +/-.005 FROM DIMENSION DATUM.
4. MINIMUM COPPER WALL THICKNESS SHALL BE .001 INCH.
   FOR ALL PLATED THROUGH HOLES. BREAKOUT NOT ALLOWED.
5. PROCESS AND MATERIAL MUST CONFORM TO UL 796. MATERIAL MUST MEET OR EXCEED UL FLAMMABILITY RATING 94V-0.
   MATERIAL:☐SINGLE SIDED,☐DOUBLE SIDED,☒MULTI-LAYER
   COPPER THICKNESS: .062 +/- .006
   BOARD THICKNESS: 062 +/-.006
   NUMBER OF FINISHED LAYERS: 10
6. ☒MANUFACTURE'S UL MARKING, FLAMMABILITY RATING, ☒ LOGO AND DATE CODE TO BE PLACED IN COPPER ON BOTTOM SIDE OF THE BOARD.
7. SOLDERMASK: LPI, COLOR = GREEN
8. SILKSCREEN ☐TOP SIDE ☒BOTH SIDES, USING ☐ YELLOW ☒ WHITE NPI LEADFREE.
   REGISTRATION TOLERANCE TO BE +/-.005.
9. P.C. BOARD TO BE FREE OF DIRT, OIL, FINGER PRINTS, ETC.
10. BOARD WARPAGE: WARP AND TWIST SHALL NOT EXCEED .007 INCH PER INCH MEASURED AT ANY LOCATION OR DIRECTION ON THE BOARD.
11. BOARD MUST BE 100% ELECTRICALLY TESTED TO ENSURE NO SHORTS OR OPEN CIRCUITS.
12. GOLD PLATING (FULL BODY): 5-15 uIN OVER 100-200 NICKEL.
    IMMERSION GOLD.
13. PADS MAY BE TEAR-DROPPED TO MEET THE ANNUAL RING REQUIREMENTS.
14. FILL VIAS UNDER BGA'S (U1, U2) WITH CONDUCTIVE EPOXY.
15. 5 MIL DIFFERENTIAL PAIRS ON LAYER 1, 5, 6, AND 10 ARE TO BE 100 OHM IMPEDANCE.
16. GROUND ETCH EXTENDED TO BOARD EDGE IS INTENTIONAL, DO NOT PULL BACK.



DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	PLATED	QTY
·	8.0	PLATED	412
·	10.0	PLATED	87
·	10.0	PLATED	81
·	12.0	PLATED	435
·	13.0	PLATED	1
*	35.0	PLATED	14
◇	35.0	PLATED	8
*	35.0	PLATED	292
*	36.0	PLATED	23
*	40.0	PLATED	1
◇	55.0	PLATED	8
○	94.0	PLATED	2
○	120.0	PLATED	2
+	140.0	PLATED	1
◇	250.0	PLATED	2
▫	40.0	NON-PLATED	2
x	125.0	NON-PLATED	4

Figure 24. Circuit Board Stackup

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/ kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this is strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

REGULATORY COMPLIANCE INFORMATION (continued)

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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