Application Brief

Automatic Power Control for Laser Diodes Using LMH13000

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Automatic power control (APC) in laser drive systems is designed for a stable and efficient laser operation by continuously regulating optical output power of the Laser. Fluctuations in temperature, aging effects, and variations in external conditions can cause instability in laser performance. APC uses a feedback mechanism to dynamically adjust the laser's drive current based on feedback from a photodiode, maintaining a consistent optical output. This enhances reliability and optimizes performance in applications which require precise control of the optical output.

This article presents the design and implementation of an Automatic Power Control (APC) loop in laser system which uses LMH13000 for driving the laser diode.

System Overview

The setup uses a laser diode which has an integrated back-facet photodiode for feedback. The back-facet diode typically refers to a photodiode or integrated sensor that monitors light emitted from the back facet of a laser diode and are generally a small fraction of the total light emitted by the laser. This small fraction of this light is sensed by the photodiode, generating current (I_{PD}) proportional to the laser's optical output. The current is converted to a voltage and compared with the reference voltage (V_{REF}) using an error amplifier (here TLV9001). This error signal also referred as the output of the error amplifier is then fed back to the laser driver LMH13000 to adjust the laser output to the set optical power.

The feedback mechanism in the system counteract any deviations from a desired state, reduce errors, and maintain stability through a feedback signal that opposes the change in the optical strength of the laser output.

The system supports both DC and pulsed laser operation. The following section explains how the APC can be achieved in both the cases.

DC Operation

In DC operation mode, as the name suggest, the laser output is a constant DC and the APC system makes sure the output power is maintained at the set DC level and does not deviate. To achieve this, the system continuously monitors the laser optical power and keep feeding this signal back to the laser driver. Figure 1 shows connection of the laser driver, laser diode, back facet diode, and the error amplifier to achieve the negative feedback loop needed for APC.

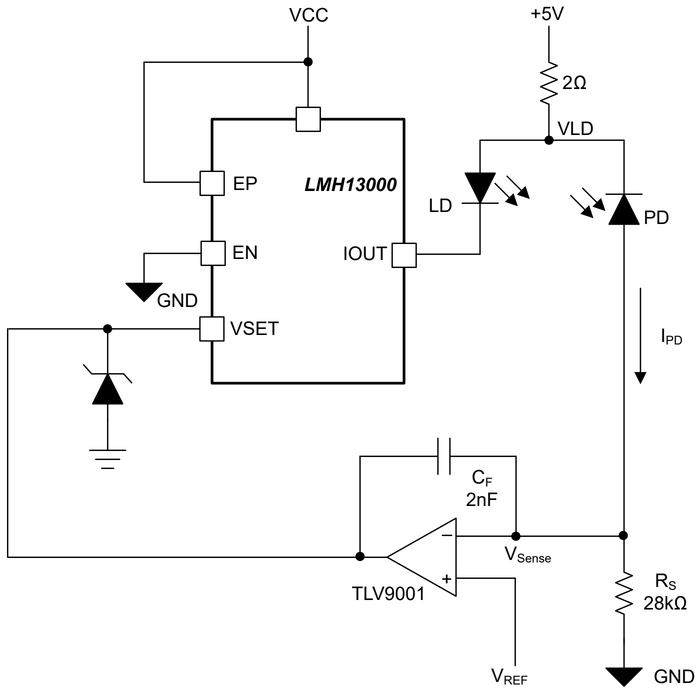


Figure 1. DC Operation Block Diagram

To set a particular output power from the laser we need the relation between the photodiode current of back facet diode (I_{PD}) and Laser optical power (P_O). This can be found in the data sheet of the laser diode. With this knowledge, set the voltage at V_{REF} pin, which can be calculated as:

$$V_{REF(set)} = I_{PD(at\ desired\ optical\ power)} \times R_{Sense} \quad (1)$$

If the relation between the I_{PD} and P_O is not known, this can be derived by forcing an appropriate current (I_{OUT}) to the laser diode which results in the required optical power (P_O) and then measuring the I_{PD} from the photodiode.

The relation between the laser current and the optical power are generally given in the laser data sheet.

The error amplifier compares the feedback signal with V_{REF} signal to set the voltage at VSET for the desired optical output. Based on the difference (error) between the two, the amplifier adjusts the output voltage (VSET) in a way to bring the V_{Sense} voltage closer to the V_{REF} voltage. And as the error amplifier adjusts the VSET, the LMH13000 adjust the output current through laser accordingly.

The adjustment in laser current, brings the I_{PD} and hence the optical output power back to the set value. This feedback mechanism to adjust the laser's drive current makes sure of a consistent optical output is achieved in DC operation.

Pulsed Laser Operation

The APC loop for pulsed laser operation functions similarly to the DC mode described in the previous section. However, to enable the pulsed output two modification need to be introduced to the system:

- A mechanism to temporarily open the control loop during laser pulsing, this is achieved by adding a 2:1 mux switch (SPDT), S1
- A memory element to retain the VSET value when the loop is opened. This is achieved by adding C1

These enhancements make sure that the system does not attempt to compensate for error during the laser's off period during pulsed operation, when the drive current drops to zero.

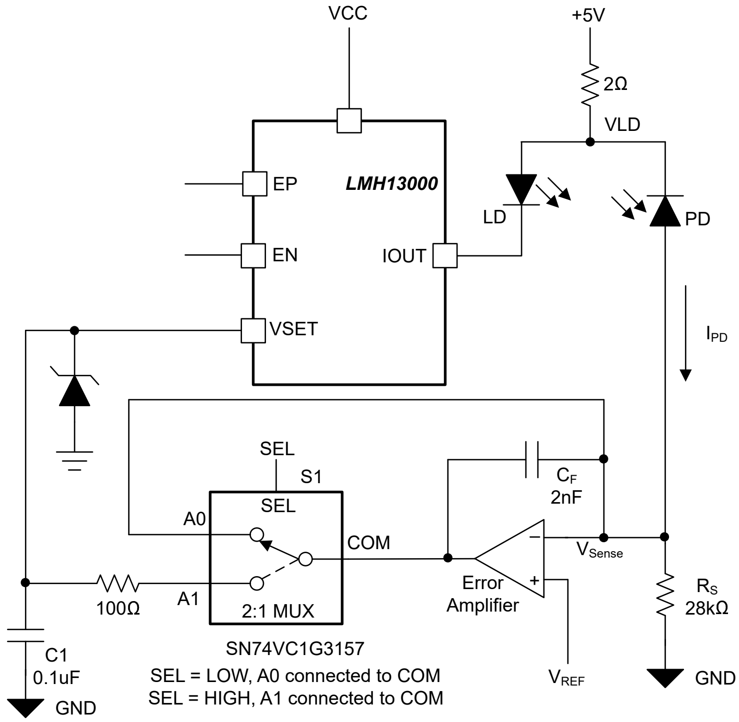


Figure 2. Pulsed Laser Operation Block Diagram

To configure the laser for the desired peak optical power, initiate the APC loop by closing switch S1—connecting COM to A1 as shown in Figure 2. This action engages the optical feedback path, and pulling the EP pin high enables the LMH13000 output. During this phase, the system operates as a conventional APC loop, as previously described for DC mode. Capacitor C1 charges to the appropriate VSET voltage as required for pulsed operation.

To transition into pulsed mode, feedback loop is opened by toggling switch S1 to connect COM to A0. In this configuration, the TLV9001 disconnects from the LMH13000, effectively breaking the feedback path. The TLV9001 loop closes locally and now functions as a buffer, preventing output from saturating to the supply rail. With the feedback loop disengaged, the system no longer attempts to regulate current or optical power deviations during this time.

This makes sure that during the laser's off period of the pulse mode—when the drive current drops to zero—the control loop does not erroneously respond to the absence of optical output. Pulsing is achieved by applying a signal to the EP/EN pins. The voltage across capacitor C1 determines the peak current during each pulse. Since C1 retains charge while switch S1 remains open, this continues to provide the necessary VSET. This sequence repeats cyclically to maintain consistent control over the laser's peak optical power.

Lab Results

For the experiment, the laser diode (here PLT5 518FB_P) is configured to deliver an optical output power of 32mW at room temperature. According to the laser's data sheet Po vs If plot (refer to Optical Output Power section *Optical Output Power*), this corresponds to a forward drive current of approximately 85mA.

To determine the corresponding photodiode current (I_{PD}), the laser is driven with 85mA, and the resulting I_{PD} is measured to be 2.5μA. Based on the transimpedance gain of 28kΩ, the required reference voltage (V_{REF}) is calculated as:

$V_{REF} = I_{PD} \times R_{Sense} = 2.5\mu A \times 28k\Omega = 70mV$

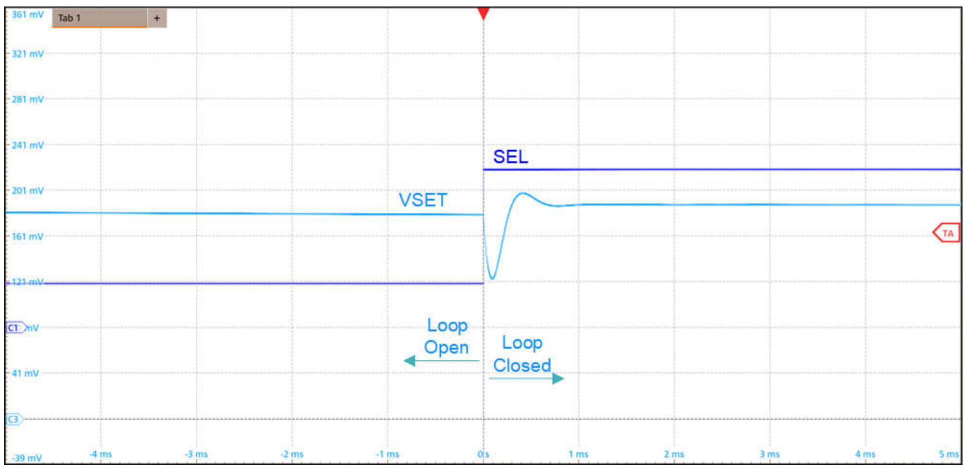
Once V_{REF} is set to 70mV, the APC loop stabilizes the laser current at 85mA, making sure the desired optical output is maintained.

Figure 3 and Figure 4 illustrate the system's dynamic response during the SPDT switching and the pulsed operation.

Figure 3 shows VSET voltage set by the error amplifier after the loop get closed. For 85mA of set IOUT current VSET settles at 171mV. This voltage is in accordance with the IOUT vs VSET relation of LMH13000 (refer to the device data sheet for more detail: *LMH13000 High-Speed, Pulsed- and Continuous-Output Current Driver*)

Figure 4 demonstrates the transition to pulsed operation mode. At t = –40µs, the SEL signal toggles to open the loop. Capacitor C1 retains charge, preserving the VSET voltage. This can be seen as the flat line in the VSET plot. During this time the laser current is maintained 85mA and this can be confirmed by the VLD voltage which is at 170mV (85mA x 2Ω) below 5V laser supply.

At t = 0s, a pulse signal is applied to the EP pin for 10 cycles, resulting in current pulses through the laser. These pulses manifest as voltage pulse signal at the VLD node (anode of the Laser) cause by the IR drop across the 2Ω resistor.



I_{OUT}= 85mA, V_{REF}= 70mV, LMH13000 MODE= 0

Figure 3. Output Waveform During Pulsed Operation

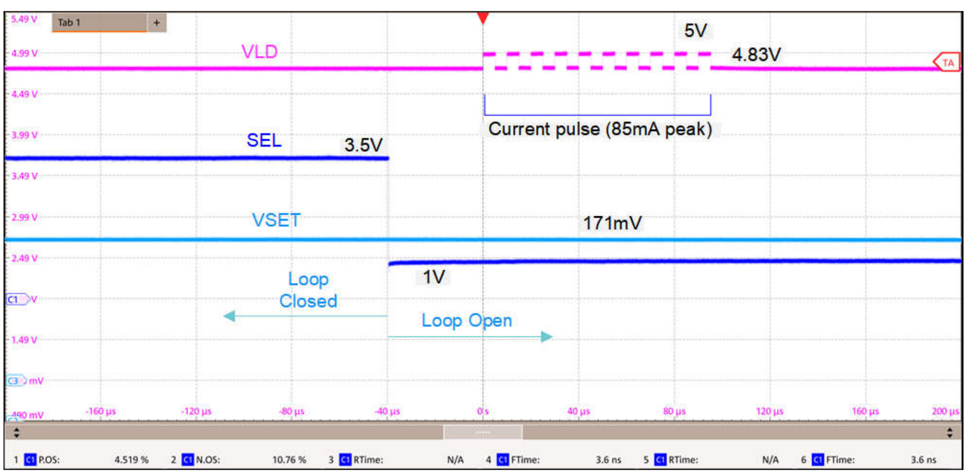


Figure 4. Output Waveform - Zoomed Positive SEL Transition

Parameters to Consider in the Design

Selecting the Value of Capacitor, C1

The capacitor C1 stores the charge required to generate the set voltage at the VSET pin of the LMH13000 when the APC loop is open during pulsed operation. Any leakage of charge from this capacitor results in drop in the voltage across this which directly introduces an error in the set current during pulse operation.

The primary leakage paths include the leakage from the zener diode, input/output pin of mux and the VSET bias current leakage

The voltage across C1 drops over time due to the total leakage current, I_{Leak}, and the value ΔV can be calculated as:

$$\Delta V = \left(\frac{I_{Leak}}{C1}\right) \times \Delta t \quad (2)$$

$$I_{Leak} = I_{Leak}(VSET) + I_{Leak}(Zener) + I_{Leak}(Mux) \quad (3)$$

Δ t = time when the loop remains open

To prevent this error from affecting the set current, the system must periodically close the loop and recharge the capacitor C1 before the voltage drops beyond the acceptable error range.

Selecting Zener Clamp Diode

The absolute maximum rating of the VSET pin in the LMH13000 is 2.5V. Applying a voltage above this limit can permanently damage the device. This situation can occur, for example, if the error amplifier becomes unstable and the output swings to the positive rail supply, causing the amplifier supply voltage to exceed 2.5V.

To prevent this, either:

1. Choose an amplifier that operates below 2.5V, or
2. Place a Zener diode clamp at the VSET pin with a breakdown voltage less than 2.5V.

This clamp make sure the VSET pin never exceeds the maximum rated voltage. For instance, the TLV9001 can operate from 1.8V to 5.5V, so if operated below 2.5V, does not require a Zener diode.

If using a Zener diode, make sure the diode has low reverse leakage, as high leakage can deplete charge from the capacitor C1 more quickly, introducing error as described earlier.

Selecting C_F

Place the capacitor C_F in the local feedback path of the error amplifier to improve both stability and transient response. This capacitor, combined with the resistor R_S, introduces a pole in the feedback loop which increases the phase margin, thus helping prevent oscillation or ringing. Choose the value of C_F precisely to balance stability and bandwidth performance.

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