Application Note

Optimizing EMI Performance in Buck Regulators for Medical Imaging Applications

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ABSTRACT

For low-noise medical imaging applications, reducing the effects of electromagnetic interference (EMI) becomes an increasingly critical system design consideration. Designing for low EMI can save you significant development cycle time while also reducing board area and design cost. Though component selection makes huge difference in reducing EMI, optimized layout plays a significant role in reducing EMI as well.

This application note discusses the improvements in conducted and radiated emissions of four latest buck devices from TI. Using the example of two buck converters (TPS543820 and TPS543A22) and two buck converter modules (TPSM843620 and TPSM843A22), the effects of PCB layout and input filtering are observed. Note that these converters and modules are related: the TPSM843A22 is the module version of the TPS543A22 converter, and the TPSM843620 is the 6A module version of the TPS543820 converter.

New EMI-friendly layouts are designed to test the effects of improved layout on EMI performance. Consequently, the boards were all tested with and without a 2nd order input pi filter to test the effects on EMI performance. In the redesigned PCBs optimized for EMI performance, layout techniques such as via stitching, minimized high di/dt current loops, and improved power density were used to minimize noise.

By the end of this article, the reader can have an idea of the extent to which PCB layout and proper input filtering can affect EMI performance of buck converter designs.

Table of Contents

Trademarks

1 Introduction

Electromagnetic interference (EMI) is an important topic within medical imaging applications (especially ultrasound scanners), as these devices are sensitive to noise within the ultrasound probe frequency range. EMI at these frequencies can reduce image quality, so minimizing the known causes of this noise in your design is critical for measurement accuracy and quality results.

While designing any ultrasound application, the probe frequency range (typically between 2MHz and 20MHz) and the third harmonic are important parameters to consider. The third harmonic can be calculated as three times the frequency of interest; for this article we are particularly interested in the switching frequency (fsw) which does not interfere with the ultrasound frequency range. To avoid any interference from the third harmonic of the switching frequency, calculate as: Equation 1 or Equation 2. Therefore, keeping the switching frequency at or less than 600kHz makes the design flexible and allows the power supply to be used with any probes ranging from 2MHz – 20MHz. For this purpose, all buck converters in this application note are operated at a switching frequency of 500kHz.

$$f_{sw} \leq \frac{2MHz}{3} \quad (1)$$

$$f_{sw} \leq 667kHz \quad (2)$$

2 Layout Techniques to Reduce EMI

2.1 Placement of Passive Components

Placing decoupling capacitors as close to the IC as possible is highly recommended in any power supply to minimize noise. This can reduce the distance that the high frequency currents have to travel, and can therefore minimize the loop antenna area that these frequencies can radiate through.

For output passive components, placing the highest frequency output capacitor close to the output side of the inductor can help to minimize ringing at the source. The farther away capacitors are away from the inductor, the more series resistance is introduced, and the less impact this can have to filter the high frequency switching noise. With this, larger capacitors need to be placed further away while the smaller capacitors need to be prioritized, as they typically have less equivalent series resistance (ESR).

2.2 Ground Flooding

By creating one solid ground plane around power and signal traces, a low impedance shield is created to protect against noise. All boards in this app note were four-layer PCBs. Ground pours were created around power and signal traces on every layer, with one middle layer being entirely ground plane with no power or signal traces. This prevents unwanted interference from both entering and leaving sensitive areas of the circuit due to a decreased return-path resistance. Note that when flooding the ground planes, do not use thermal reliefs. Flood over all same net holes and vias.

2.3 Minimize Number of Antennas

Having exposed traces of copper or any sort of conductor that has current or voltage running through it can cause it to act as an antenna and can radiate. Therefore, the first step taken to minimize EMI on this layout was to remove any unpopulated footprints and test points.

2.4 Via Stitching

The via stitching technique consists of using via connections between outer ground layers. By creating these evenly spaced vias around the circuit, a ground loop connection shown in Figure 2-1 is avoided and you end up with Figure 2-2. This direct connection to ground further lowers the impedance and parasitic in the PCB.

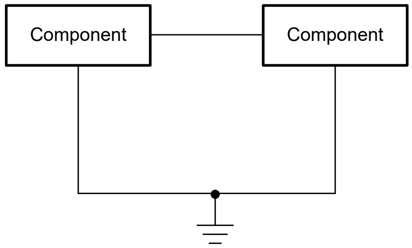

Figure 2-1. Ground Loop Connection

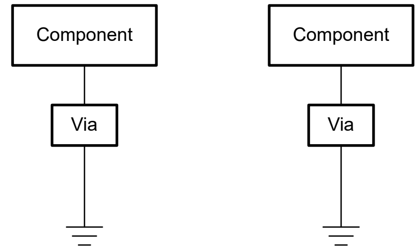

Figure 2-2. Avoided Ground Loop Connection With Vias

2.5 Additional Steps to Minimize Impedance or Noise

Additional ways to minimize impedance and reduce EMI in your PCB are listed below:

- Placing extra vias near all ground pins can further minimize impedance in a similar manner as described previously.
- Avoid open space with no ground pours around. Avoid big power/signal pours generally.
- Reduce PCB height as much as possible. You can do this by adjusting the center dielectric so the current between layers has less distance to travel.

3 Designing for EMI-Optimized Layout

Four different layouts are created for the four different buck regulators:

1. TPS543820
2. TPSM843620
3. TPS543A22
4. TPSM843A22

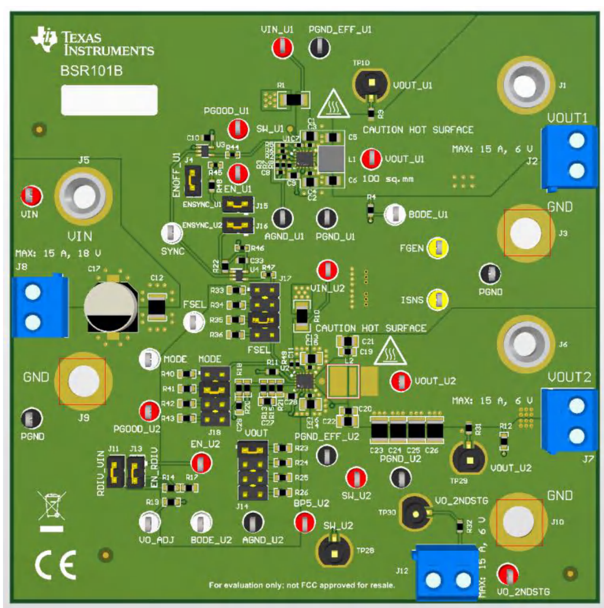

Figure 3-1. TPS543620 EVM Standard Layout

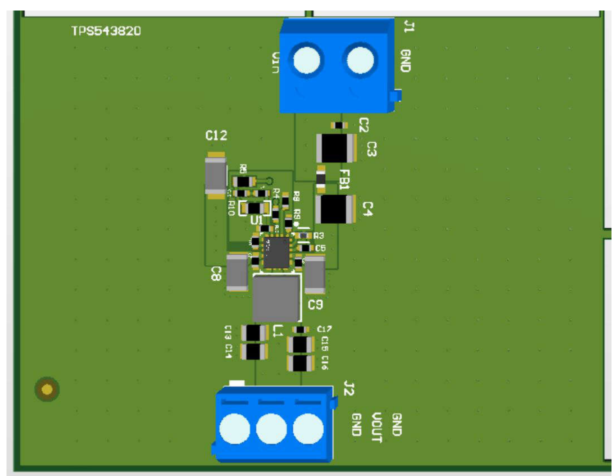

Figure 3-2. TPS543820 EMI-Optimized Layout

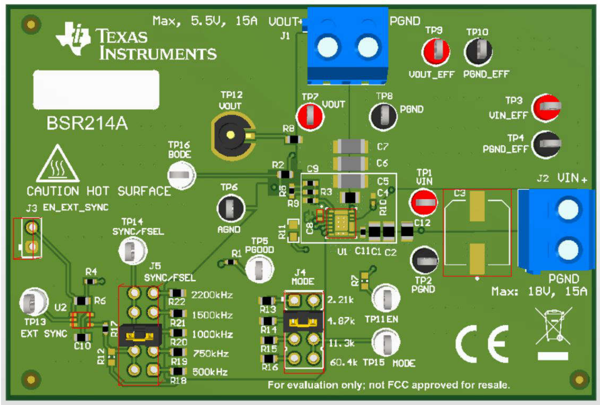

Figure 3-3. TPSM843620 EVM Standard Layout

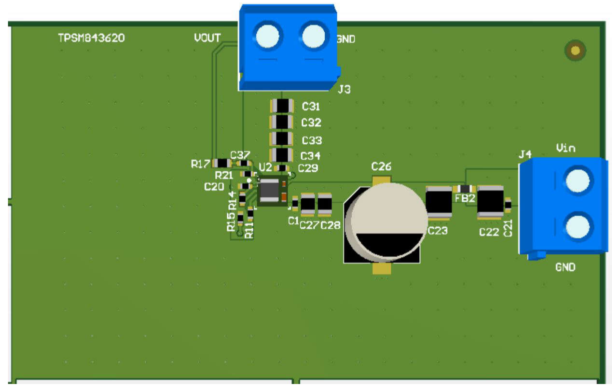

Figure 3-4. TPSM843620 EMI-Optimized Layout

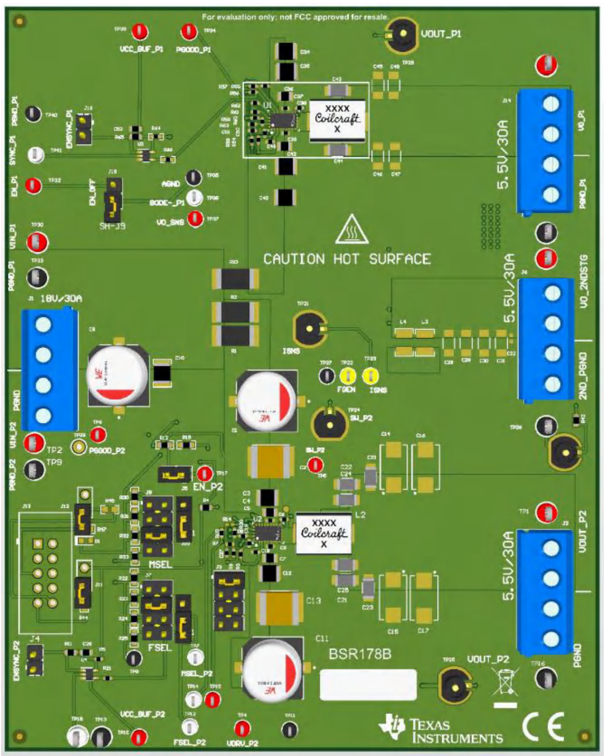

Figure 3-5. TPS543B22 EVM Standard Layout

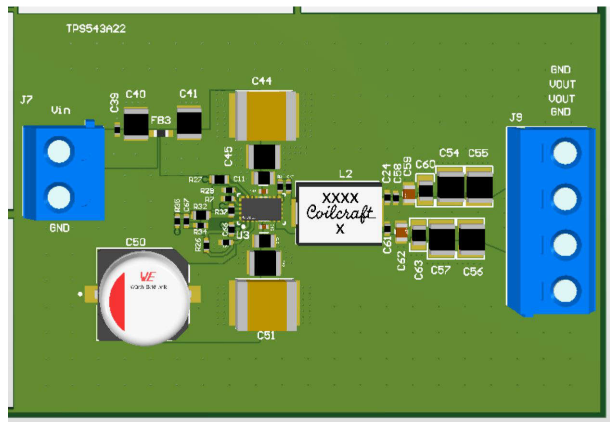

Figure 3-6. TPS543A22 EMI-Optimized Layout

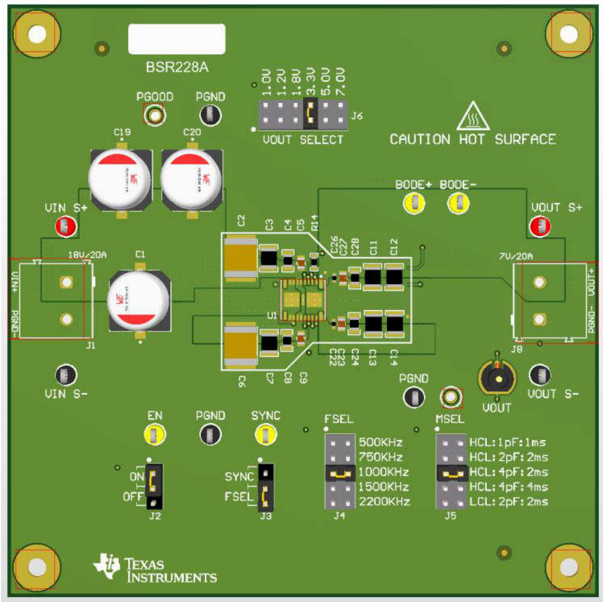

Figure 3-7. TPSM843B22 EVM Standard Layout

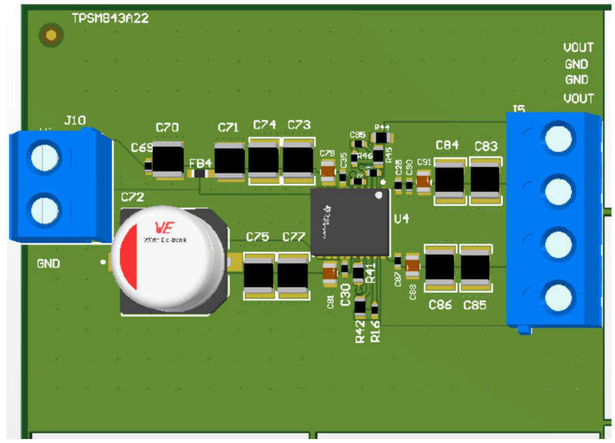

Figure 3-8. TPSM843A22 EMI-Optimized Layout

4 Test Results for Radiated Interference

The following data was taken in the CISPR Chamber with CISPR32 pre-compliant setup. These results are not officially CISPR certified. The table below shows a summary of the experimental setup for each set of tests. A photo of the setup is shown in Figure 4-1. The results show a significant improvement in the radiated emissions, showing that EMI can be heavily reduced by changing only the layout.

Table 4-1. Testing Conditions

IC	Vin	Vout	Iout	Switching Frequency
TPS543820	12V	1.2V	8A	500kHz
TPSM843620	12V	1.2V	6A	500kHz
TPS543A22	12V	1.2V	10A	500kHz
TPSM843A22	12V	1.2V	10A	500kHz

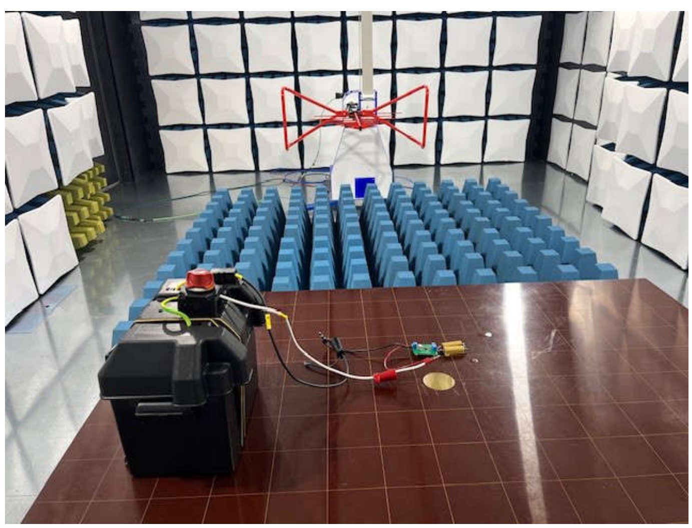

Figure 4-1. Radiated Emissions Testing Setup

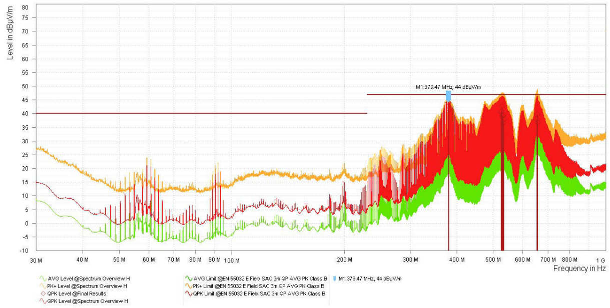

Figure 4-2. TPS543620 EVM Results

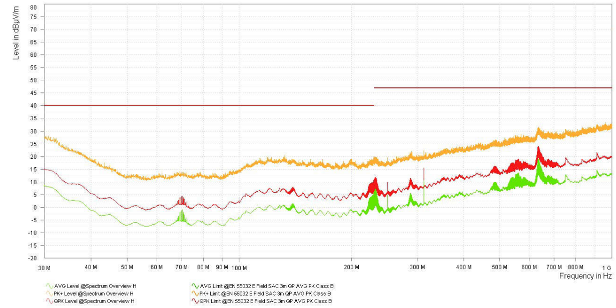

Figure 4-3. TPS543820 EMI-Optimized Results

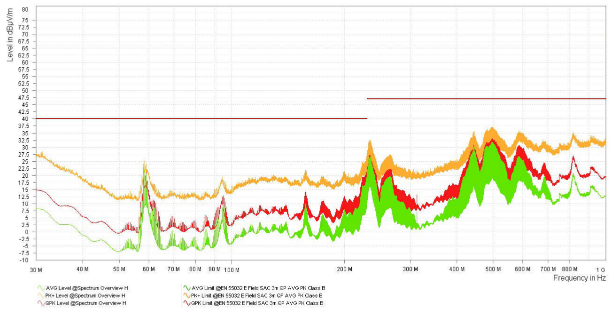

Figure 4-4. TPSM843620 EVM Results

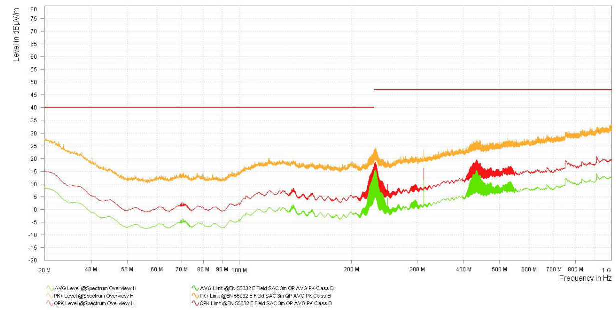

Figure 4-5. TPSM843620 EMI-Optimized Results

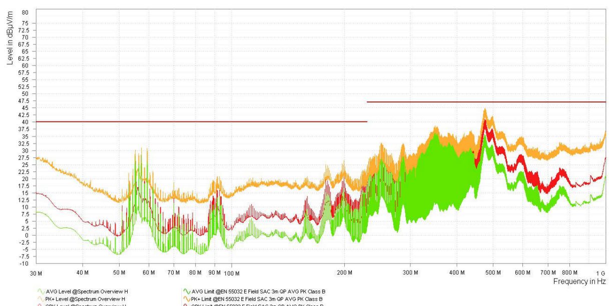

Figure 4-6. TPS543B22 EVM Results

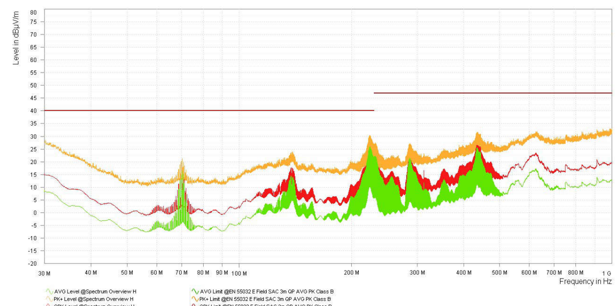

Figure 4-7. TPS543A22 EMI-Optimized Results

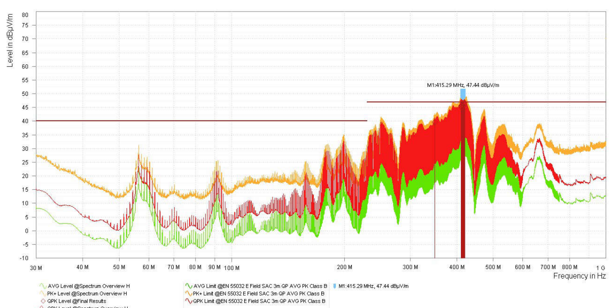

Figure 4-8. TPSM843B22 EVM Results

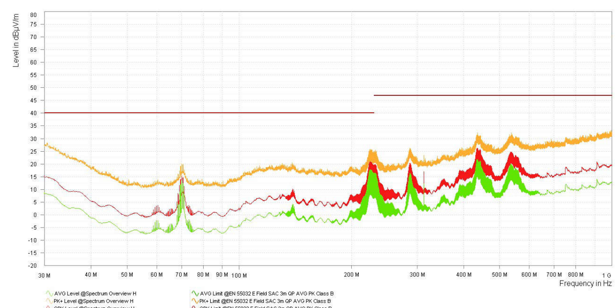

Figure 4-9. TPSM843A22 EMI-Optimized Results

5 EMI Filtering

To help reduce conducted EMI at the switching frequency of our boards, we tested the effects of two different input filter types:

- A ferrite bead-based pi filter
- An Inductor-based pi filter

The pi filter is shown in Figure 5-1, with the ferrite bead or inductor between two capacitors.

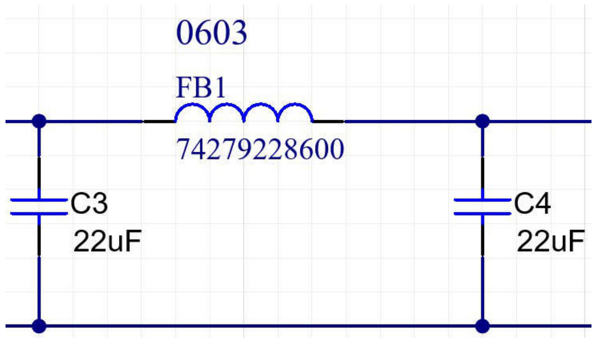

Figure 5-1. Example pi Filter With Ferrite Bead

Simulated bode plots for the ferrite bead pi filter are shown in (Figure 5-2) and inductor pi filter (Figure 5-3).

Figure 5-3 shows that the ferrite bead filter has the max attenuation occurring at just over 1MHz, after which the attenuation begins to flatten out, while the inductor filter similarly has the max attenuation occurring at just over 1MHz, after which the attenuation begins to flatten out.

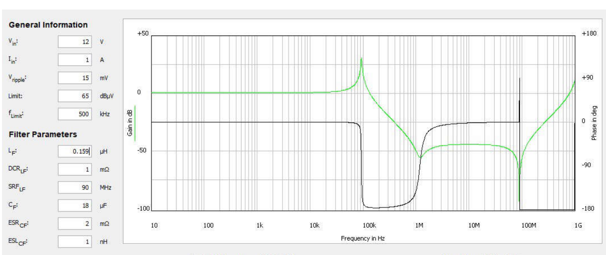

Figure 5-2. Bode Plot for Ferrite Bead pi Filter

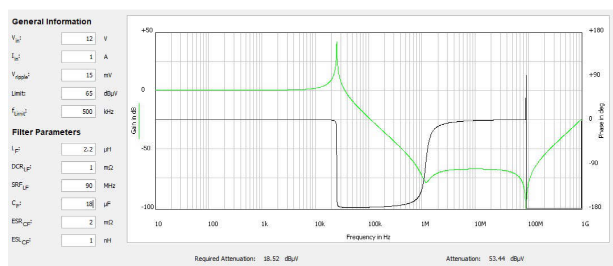

Figure 5-3. Bode Plot for Inductor pi Filter

We tested the simulation results with a series of conducted emissions tests, with the test setup shown in Figure 5-4. In the following conducted EMI data, for the frequencies below 2MHz, the inductor filter caused significantly more improvement to the conducted EMI than the ferrite bead filter. At the switching frequency of 500khz, the 2.2uH inductor filter created 35dB more attenuation.

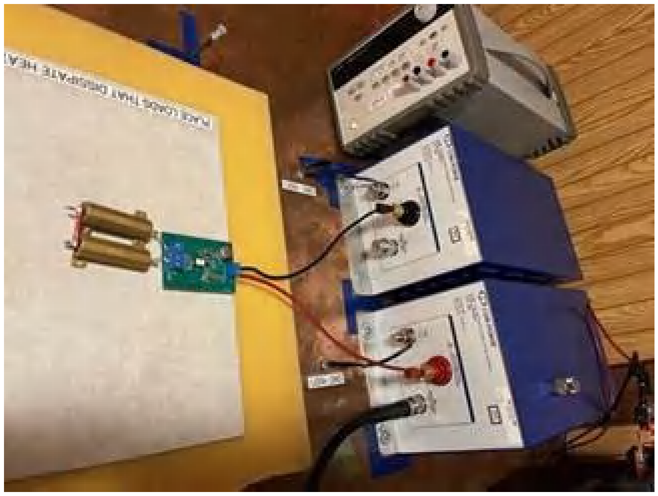

Figure 5-4. Conducted Emissions Test Setup

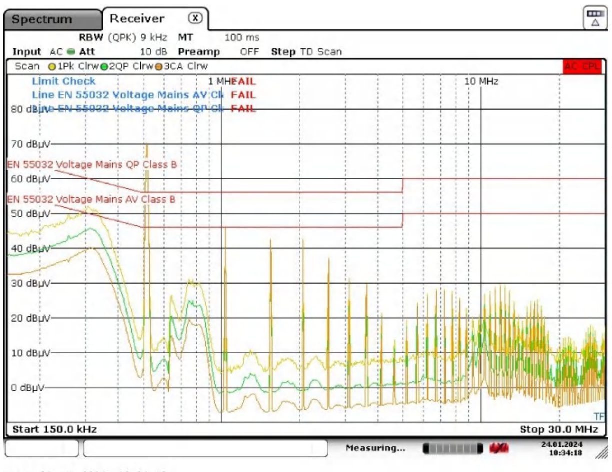

Figure 5-5. TPS543820 Conducted EMI Results With Ferrite Bead Filter

Figure 5-6. TPS543820 Conducted EMI Results With Inductor Filter

Figure 5-7. TPSM843620 Conducted EMI Results With Ferrite Bead Filter

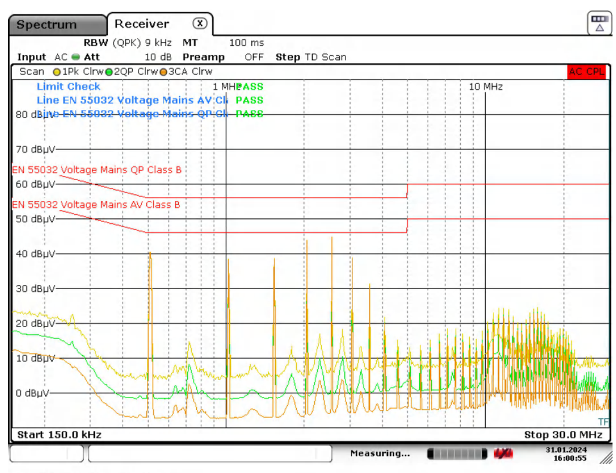

Figure 5-8. TPSM843620 Conducted EMI Results With Inductor Filter

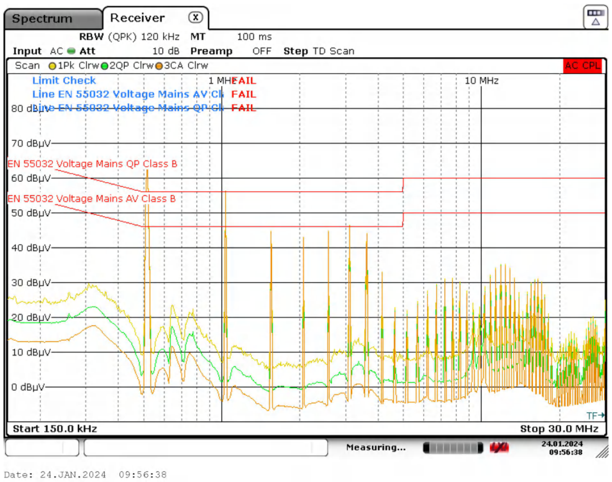

Figure 5-9. TPS543A22 Conducted EMI Results With Ferrite Bead Filter

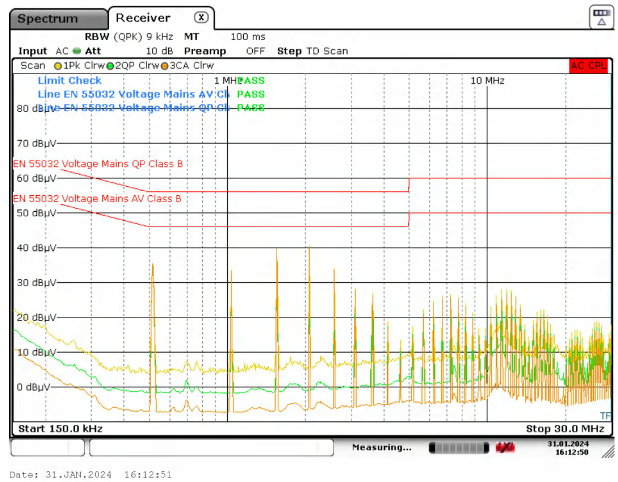

Figure 5-10. TPS543A22 Conducted EMI Results With Inductor Filter

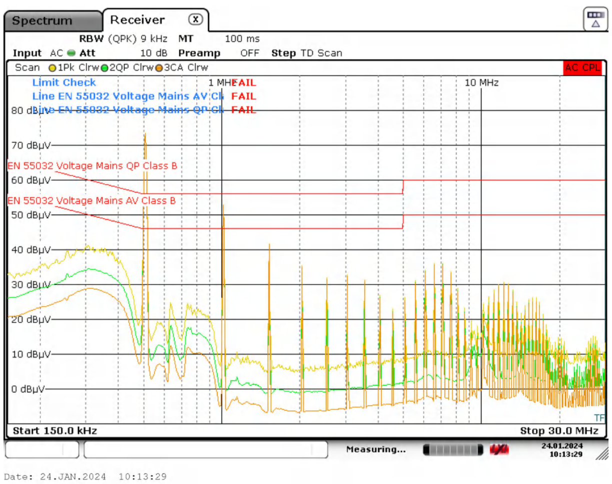

Figure 5-11. TPSM843A22 Conducted EMI Results With Ferrite Bead Filter

Figure 5-12. TPSM843A22 Conducted EMI Results With Inductor Filter

6 Summary

As discussed in this application note, changes in PCB layout and input filtering are shown to improve both radiated and conducted emissions. Considering these optimizations is critical in the next circuit design for lowered EMI performance and quality results in the final product.

7 References

- Texas Instruments, *AN-2155 Layout Tips for EMI Reduction in DC / DC Converters,* application note.
- Texas Instruments, *EMI Mitigation Techniques Using the LMZM23601,* application note.
- Texas Instruments, *Low EMI.*
- Texas Instruments, *Medical and Healthcare.*