Application Report
SLOA255–October 2017

Piezo Haptics With Integrated Waveforms: DRV2605L-Q1 and DRV2700

ABSTRACT

The DRV2700 is a high-voltage piezo driver with an analog input. This device is one of the many haptic feedback drivers that Texas Instruments™ offers. One design challenge many customers face using the DRV2700 is the analog input. Generating an analog input signal can burden the processor and be undesirable. This application note addresses this challenge and provides a solution.

Contents

1 Introduction 2
2 Bandwidth 3
3 DRV2605L-Q1 Setup 4
4 DRV2700 Setup 4
5 Test Results 5

List of Figures

1 Block Diagram 2
2 Amp Gain Bandwidth VBST 30 V 3
3 Am Gain Bandwidth VBST 55 V 3
4 Amp Gain Bandwidth VBST 80 V 3
5 Amp Gain Bandwidth VBST 105 V 3
6 Final Test Setup 5
7 6
8 6
9 6
10 6

List of Tables

1 DRV2605L-Q1 Settings 4
2 Programmable Gains 4

Trademarks

1 Introduction

The DRV2605 family of drivers (including the DRV2605L and DRV2605L-Q1) offer integrated waveforms that ship with the device. These drivers use a Class-D output stage that switches around 20 kHz. With the use of a simple low-pass filter, the DRV2605L-Q1 can be used as an input to the DRV2700. Figure 1 shows the block diagram for this solution.

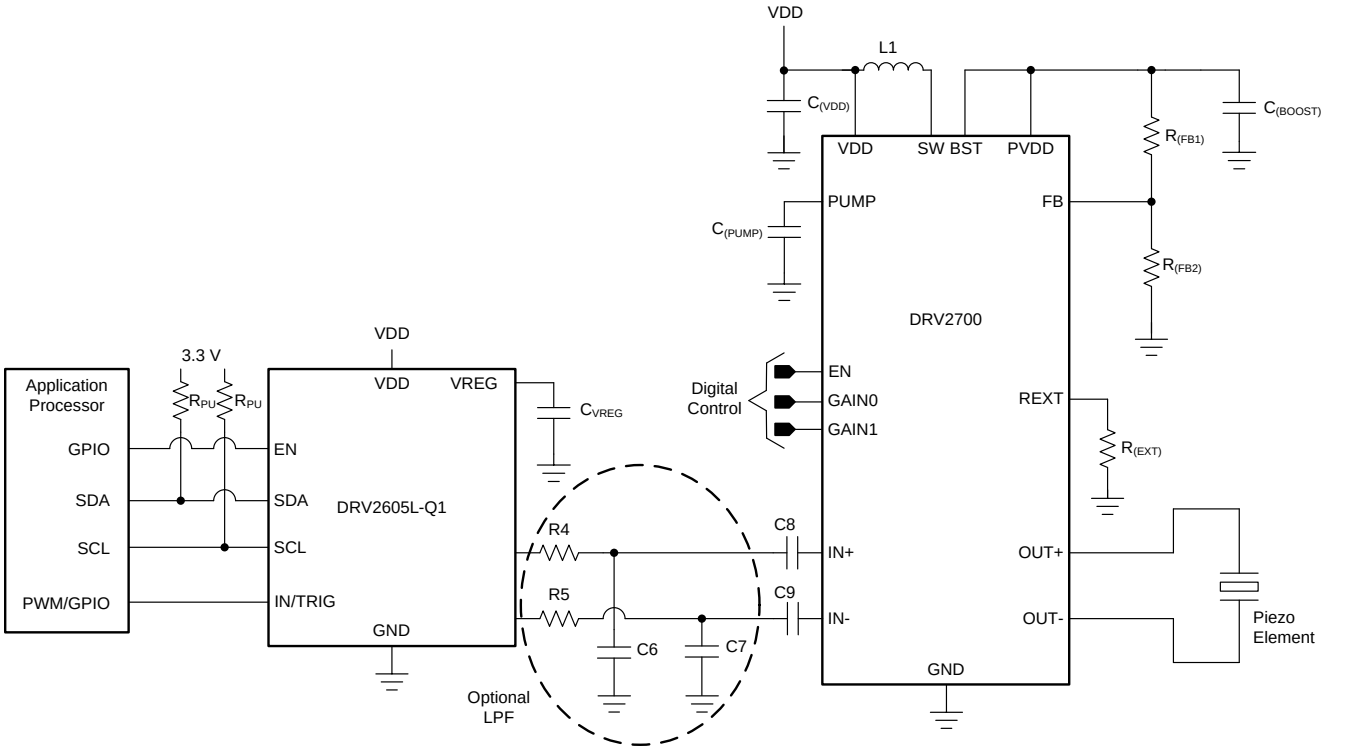

Figure 1. Block Diagram

This configuration (see Figure 1) makes it possible to play waveforms through I^2C from the DRV2605L-Q1 to the DRV2700. The DRV2700 amplifies the input signal to the desired voltage to drive the piezo element. This voltage can be 200 Vpp differentially or 500 Vp with the use of a flyback. There are a few configuration details that must be considered when using this setup.

2 Bandwidth

The bandwidth for the DRV2700 is a function on the piezo load capacitance. Figure 2, Figure 3, Figure 4, and Figure 5 show the relationship between the DRV2700 output voltage and frequency. For most cases, the frequency will be well below the 20-kHz level. In this case, the low-pass filter between the DRV2605L-Q1 and DRV2700 is optional. For best practice, TI recommends using a simple first order low-pass filter along with DC blocking capacitors (C8 and C9 in Figure 1).

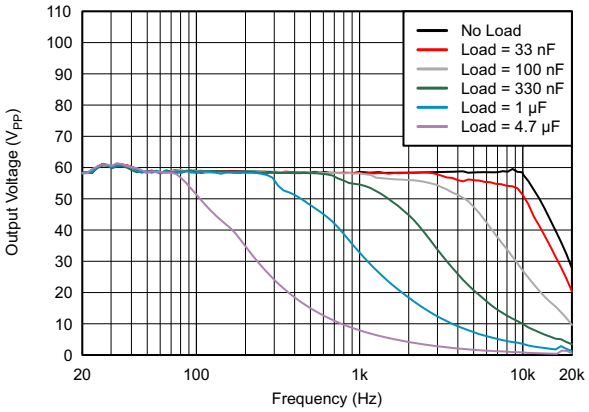

Figure 2. Amp Gain Bandwidth VBST 30 V

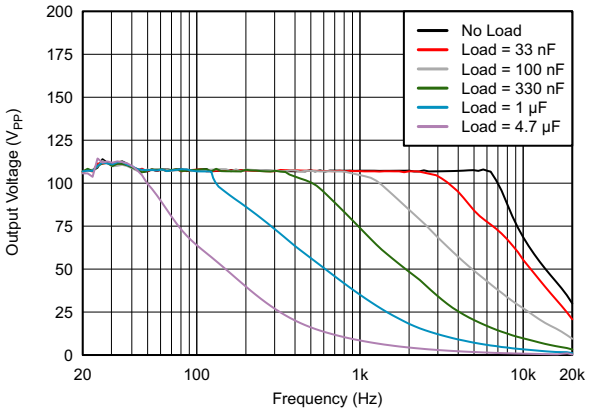

Figure 3. Am Gain Bandwidth VBST 55 V

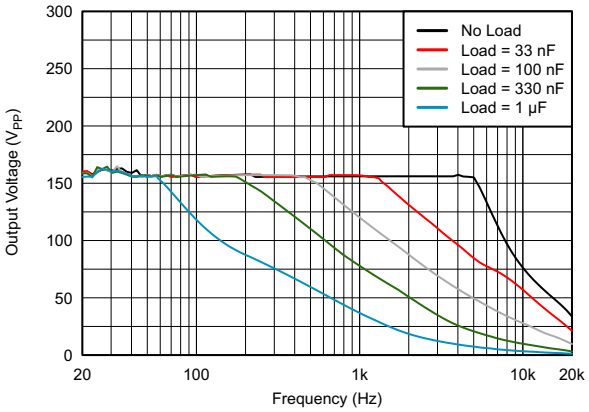

Figure 4. Amp Gain Bandwidth VBST 80 V

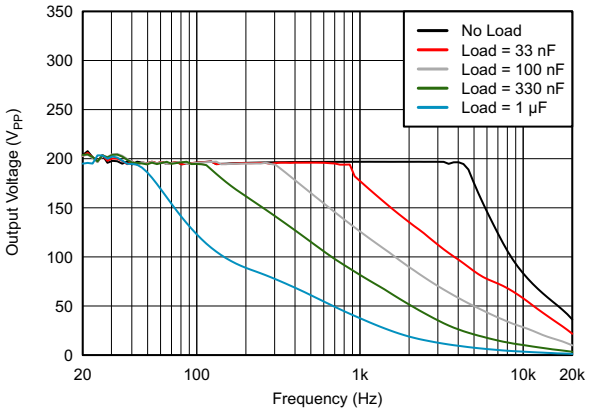

Figure 5. Amp Gain Bandwidth VBST 105 V

3 DRV2605L-Q1 Setup

The DRV2605L-Q1 can be configured in closed or open-loop mode. The closed-loop mode is used to track the BEMF voltage when driving LRAs and ERMs. For this use case, the DRV2605L-Q1 should be configured in open-loop mode by changing the register 0x1D. Next, users should select the appropriate frequency using register 0x20. The output voltage will be based on the OD_Clamp setting (register 0x17). The DRV2700 gain settings are optimized for 1.8-V_P input signal. Therefore, the OD_Clamp should be set near 1.8 V_P. Finally, the waveform must be selected using the waveform sequencer. Refer to *DRV2605L-Q1 Automotive Haptic Driver for LRA and ERM with Effect Library and Smart-Loop Architecture* for a list of the available waveforms. To trigger the waveform, there are a wide variety options including: external level trigger, external pulse trigger, and internal trigger mode. External trigger modes uses the TRIG pin, and the internal trigger activates through I^2C. Table 1 lists a summary of these settings.

Table 1. DRV2605L-Q1 Settings

DRV2605L-Q1 Setting	Register	Value
Open-loop output voltage	0x1D	0x5C
Open-loop frequency	0x20	240 Hz (0x2A)
OD_Clamp (V_{OUT})	0x17	0x55
Waveform sequencer 1	0x04	User choice

4 DRV2700 Setup

The DRV2700 should be set to the appropriate boost voltage and gain setting based on the piezo being driven. Table 2 lists four gain settings that are tuned to four configurations for the boost voltage. The gain settings are hardware selected through the two gain pins. The boost voltage should be set by configuring the feedback resistors between VBST, FB, and GND.

Table 2. Programmable Gains

GAIN1	GAIN0	Gain (dB)
0	0	28.8
0	1	34.8
1	0	38.4
1	1	40.7

5 Test Results

For the final test results, connect the DRV2605LEVM-CT and the DRV2700EVM as shown in Figure 6. For this test, a few different waveforms from the DRV2605L library were selected. The piezo element being tested is a piezo bender with the following dimensions: 38 mm × 3.8 mm × 3.2 mm. The piezo is attached to a 100-g metal block, and the acceleration is tested using the DRV-ACC16-EVM (see DRV-ACC16-EVM Accelerometer User 's Guide).

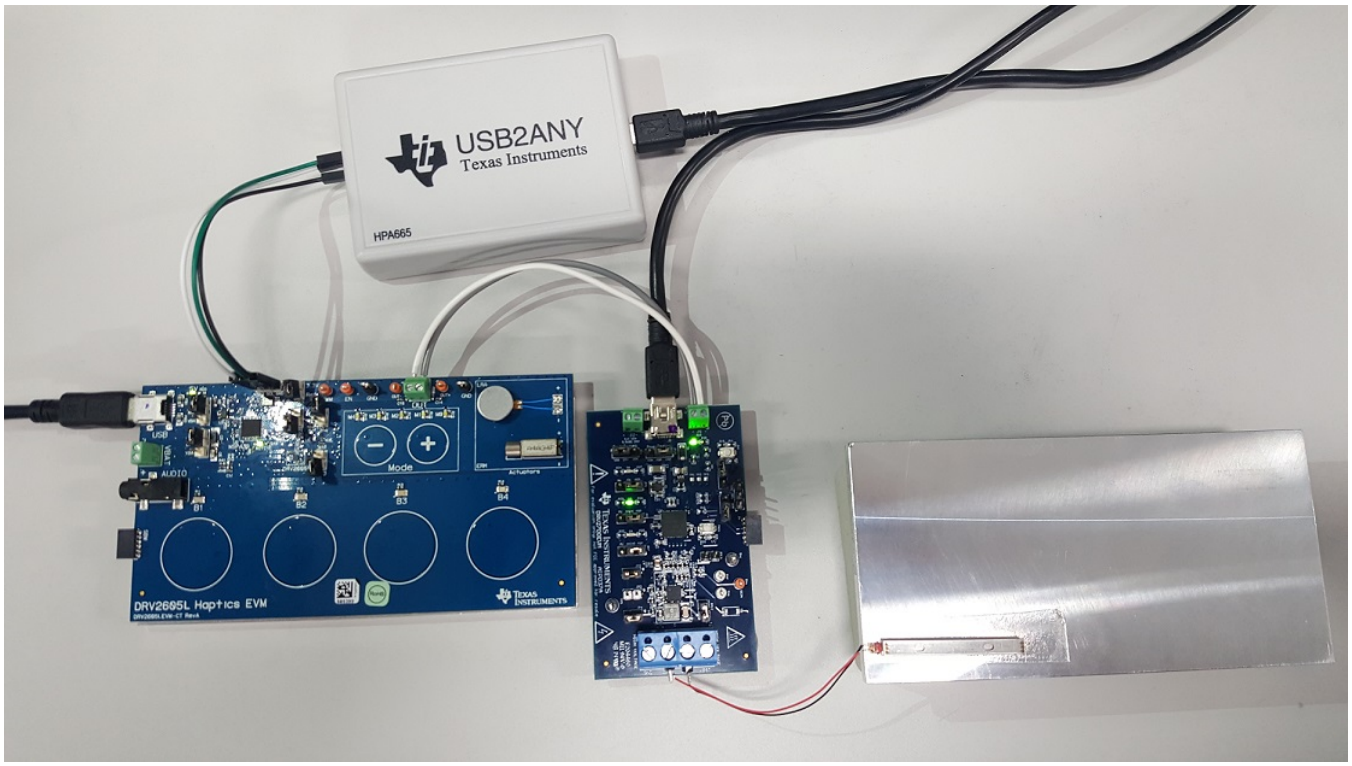

Figure 6. Final Test Setup

To optimize performance, the BRT setting (0x10) must be set to –20 ms (0xFC). This signed register removes braking. The output of the DRV2605LEVM is connected to the input jumper (J5) on the DRV2700EVM. The input goes through a second order low-pass filter and DC blocking capacitors. Figure 7, Figure 8, Figure 9, and Figure 10 show the differential output voltage and piezo acceleration profile of the DRV2700 for four different waveforms in the DRV2605L library (same as the DRV2605L-Q1).

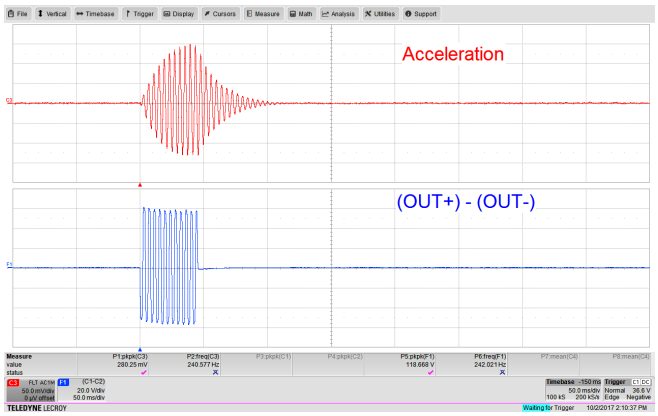

Figure 7.

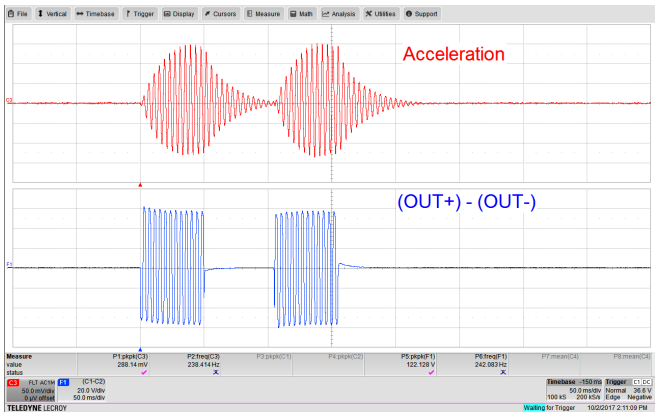

Figure 8.

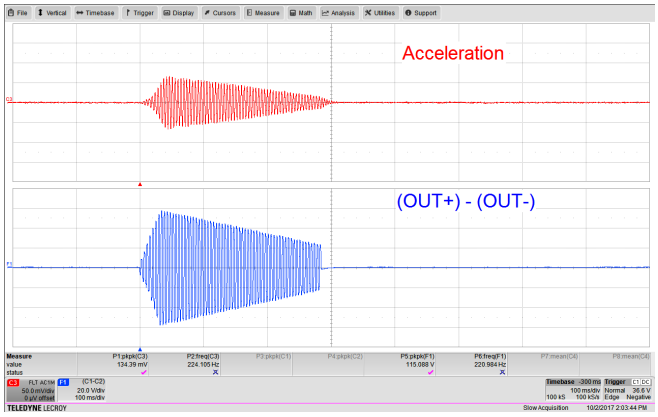

Figure 9.

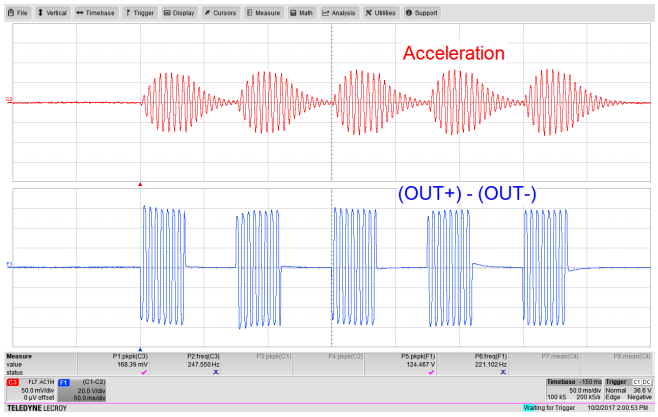

Figure 10.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Date	Revision	Description
October 2017	*	Initial release

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