Application Report

SLOA191–September 2014

Characterization Report for FMC30RF

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ABSTRACT

This application report provides characterization data for the FMC30RF. This document contains TX and RX path board performance, including internal LO and external LO test results.

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1.1 Internal Test Results

1.1.1 Block Diagram Internal LO

Figure 1 illustrates the complete system set up, including the ML605 board connected to a computer (CPU in Figure 1) via an Ethernet cable and to the FMC30RF board from the other side.

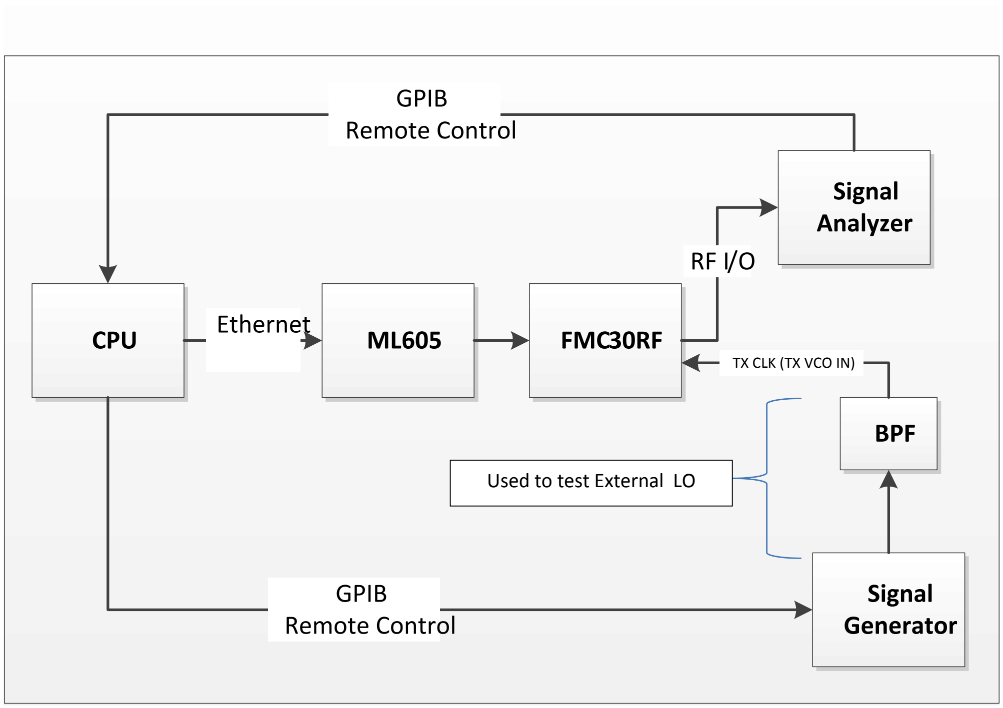

Figure 1. Block Diagram

The firmware is burned on the FPGA (located inside the ML605 board) using the Xilinx design tool. After burning the firmware, access the FMC30RF board to create a TX or RX measurement.

MATLAB is a registered trademark of The MathWorks, Inc..

Figure 2 illustrates the block diagram of the FMC30RF board (by “4DSP”).

In order to take the TX measurement, the following parts are used in the FMC30RF board (Figure 2): AFE7225, TRF3720, and CDCE62005. The AFE7225 has an internal DAC which receives an interleaved signal (digital) and transfers it (in differential IQ mode) into the TRF3720.

The TRF3720 is a modulator, requiring LO frequency (internal LO or external LO), a reference frequency, and an IQ signal. The reference frequency is generated by the CDCE62005; the IQ signal is received from the AFE7225. The LO frequency is controlled by the software (C language with visual studio) and can be changed according to demand. TI tested the FMC30RF board with two cases; internal LO and external LO.

While testing the hardware with external LO “TX VCO IN” is used in the path (TX_ CLK in Figure 2).

The RF signal is transmitted out via TX/RX (port 2 in Figure 2).

In order to test the IQ balance, port 2 was connected to FSQ (signal analyzer), see Figure 1.

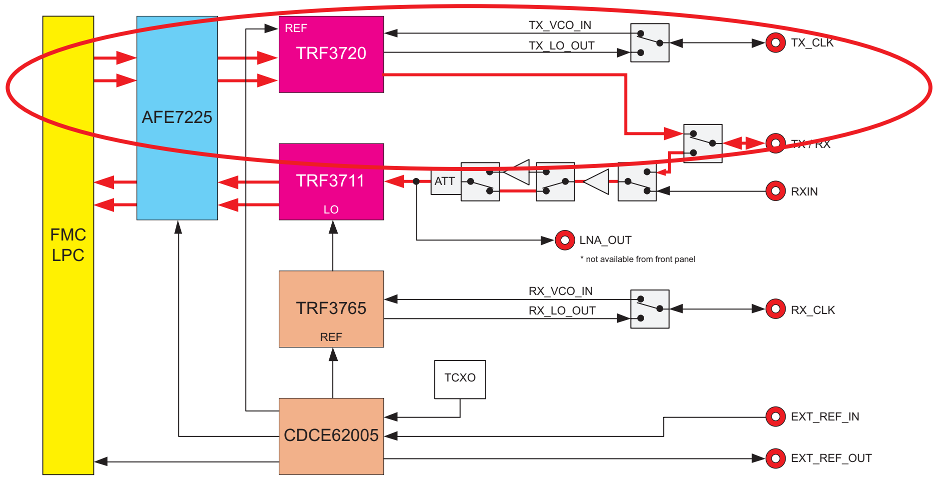

Figure 2. FMC30RF Block Diagram (TX Path Inside the Red Circle)

1.1.1.1 IQ Balance Test Theory

When transmitting a complex RF signal and analyzing it in the frequency domain, a fundamental power tone is expected in this place: **fRF = fLO ±f IF**, (represented with the number ‘1’ in Figure 3) a LO tone on **fLO** (represented with the number ‘2’ in Figure 3), and a sideband tone, (represent with the number ‘3’ in Figure 3).

The sideband tone should be zero in an ideal transmitted signal (the FFT of COS and SIN should cancel each other out) but because there are mismatches in the signal chain in gain and phase, we get a sideband tone with a nonzero value.

The IQ balance test measures the difference between the power of the fundamental tone and the power of the sideband tone. The value of **Pfundamental – Psideband** should be around 40 dBc.

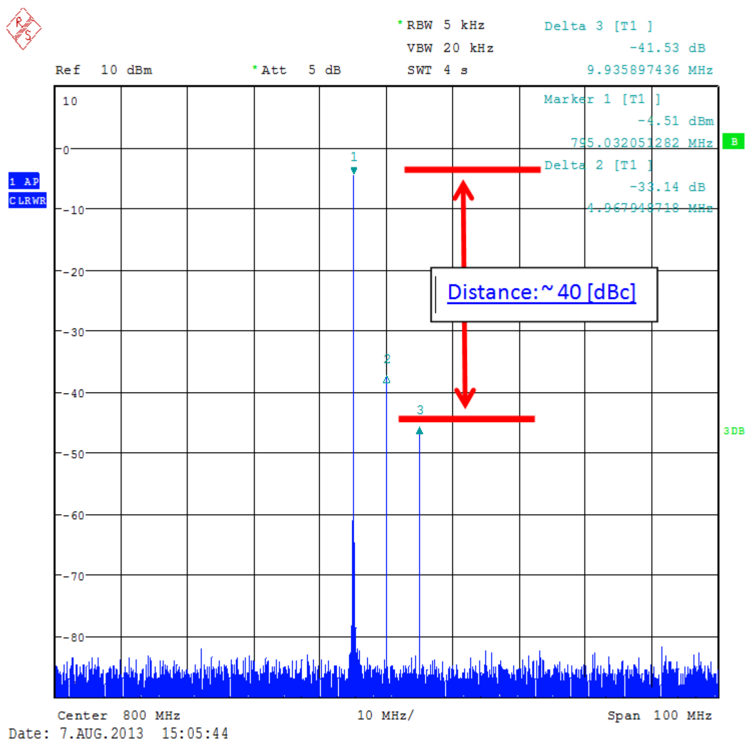

Figure 3. Example of IQ Balance Plot

1.1.1.2 IP3 Test (IMD3) Theory

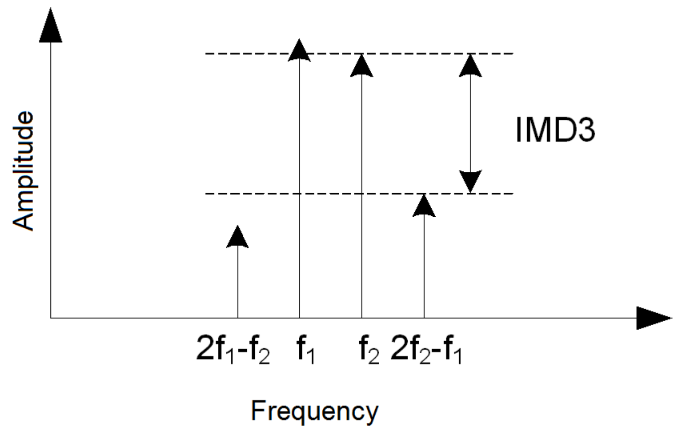

Figure 4. Frequency versus Amplitude for IMD3 Products

When generating a two-tone signal, input frequencies f1 and f2, there is a product that emerges in the output beside the two tones, the second order is neglected but the third order product is important because it falls near the band. The frequencies which are expected to be found are: $2f_1 – f_2$ and $2f_2 – f_1$.

The main issue is when the input power of the two tones increases **1XdB**, the output power of the product increases **3XdB**.

There is a theoretical point where the fundamental power meets the product IMD3 power, this point is called the *IP3 point*. The IP3 point is only theoretical because before the power reaches this point, the amplifier causes a distortion in the output signal.

1.1.2 System Setup Description

In order to test the IQ balance and IP3, the internal VCO mode was set in the FMC30RF board. TI tested the following frequencies: 300, 800, 1300, 1800, 2100, 2300, 2800, 3300, 3800 MHZ. For every frequency, two amplitude values were taken: (full scale) and (full scale – 6 dB).

The IF frequency is set to = 5 MHz, the RF I/O port is connected to the FSQ 26 signal analyzer to take the measurement values.

From this point on, few changes have been taken from the original 4DSP code settings. The reason for the changes is the TRF3720 datasheet (SLWS221), which guides how to work with fractional mode:

The following values were changed in order to work in fractional mode:

1. Reg [4] bit 25 – “**EN_DITH**” was set to 1.
2. Reg [4] bit 19 – “**LD_ANA_PREC**” was set to 3.
3. Reg [4] bit 26 – “**MOD_ORD**” was set to 2.
4. Reg [7] bit 20 – “**ISOURCE_TRIM**” was set to 7.
5. Reg [6] bit 28 – “**TX_DIV_BIAS**” was set to 0 and then set to 2 (attached the result in Section 1.1)

NOTE: On the IP3 test, the thermal conditions were: Hot – No Air Flows.

1.1.3 IQ-Balance Test Result

Figure 3 shows an example IQ-Balance test result.

There is a fundamental tone (marker ‘1’ in the plot), a LO frequency (marker ‘’2 in the plot), and the sideband tone (marker ‘3’ in the plot). The test checked the rejection value (marker 1 amplitude – marker 2 amplitude ≥ 40 dB).

The normal rejection values for TRF3720 are around 40 dB. The following sections show test results for the IQ-Balance with different conditions.

The influence of two signals was checked for every condition: full scale signal versus a full scale – 6 dB (back off signal). These conditions were also tested with internal OSC (internal LO). In Section 1.1.4, the same test was performed but only with external LO. The value of the “**TX_DIV_BIAS** “ (Reg [6] bit 28 in TRF3720) was changed from 25 µA to 50 µA to determine how that changes the results.

Results: IQ-Balance, Full scale, IF= 5 MHz, internal LO = 300 MHz to 3800 MHz.

“**TX_DIV_BIAS**” was set to 0 gives a bias point of 25 µA.

As the graphs in Figure 5 and Figure 6 illustrate, the results are around 40 dB, as expected.

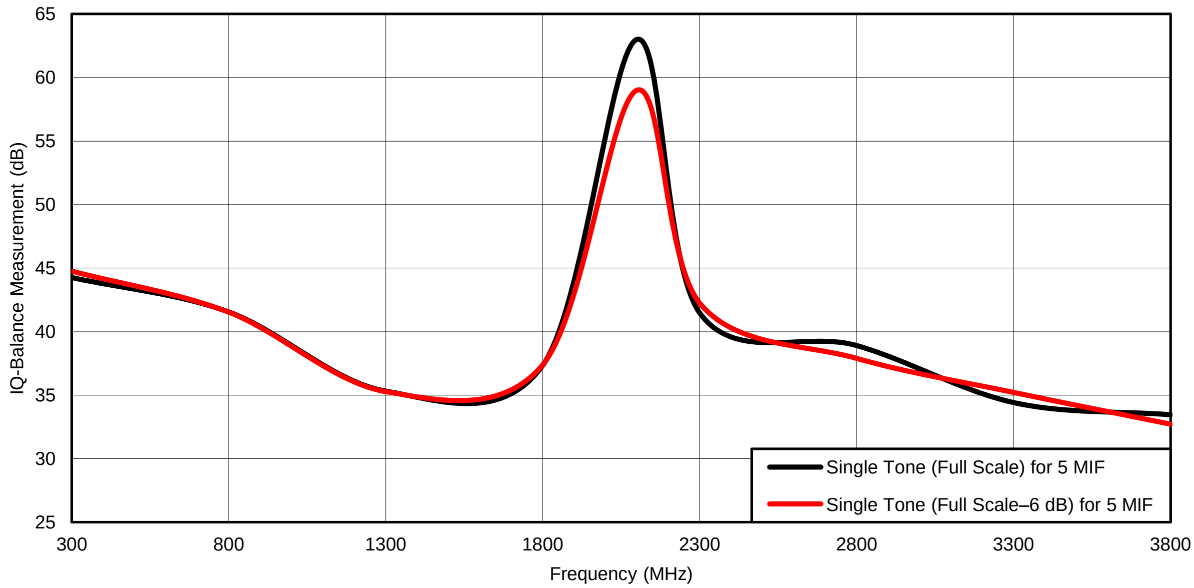

Figure 5. IQ Balance Graph for Internal LO and Bias Point of 25 µA

For Reg [6] bit 28 - "**TX_DIV_BIAS**" is set to 2, giving a bias point of 50 µA.

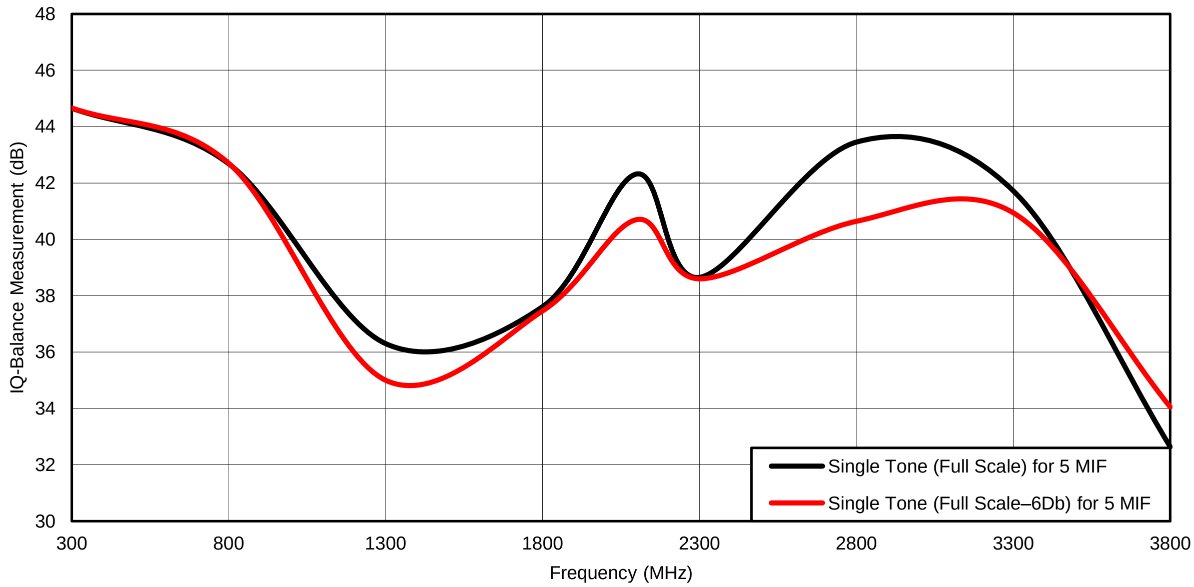

Figure 6. IQ Balance Graph for Internal LO and Bias Point of 50 µA

1.1.4 IP3 Test Results

As described in Section 1.1.1.1, two tones at the same power were created with MATLAB® as a signal generator and transmitted through the DAC in the AFE7225 and through the TRF3720 to the spectrum analyzer.

In this section the system is tested (FMC30RF board) with internal LO, in Section 1.2 the same test is performed but with changes to External LO.

In order to test the system reaction for two tones, the internal VCO mode is set in the FMC30RF board. The LO frequencies are: 300, 800, 1300,1800, 2100, 2300, 2800, 3300, and 3800 MHZ. The two tones were tested in full scale signal. The rest of the settings are the same as in the IQ balance test.

Figure 7 is an example plot from the output of the RF chain (MATLAB in CPU → ML605 → AFE7225 (DAC) → TRF3720 → signal analyzer).

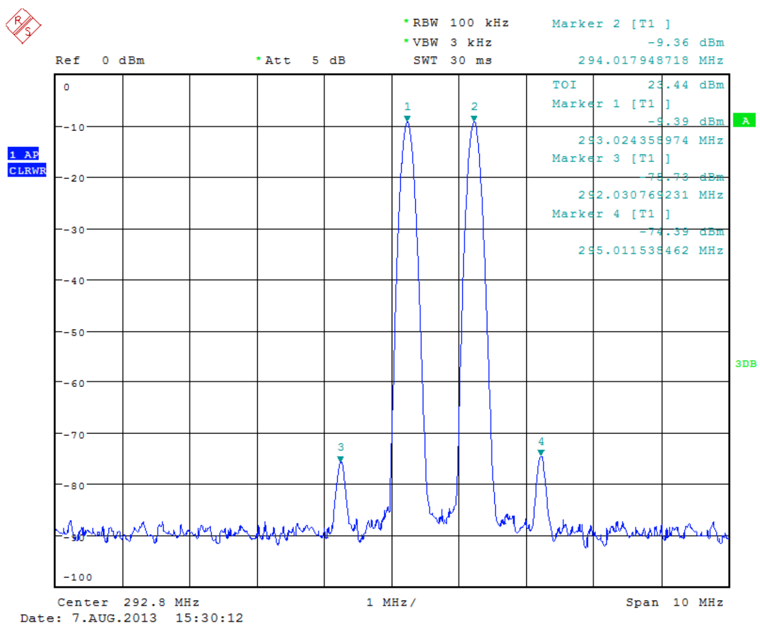

Figure 7. TX of Two Tones (Markers 1 and 2) and the IP3 Products Result (Markers 3 and 4)

Figure 8 shows the results for two bias points: 25 µA and 50 µA, as previously described.

The expected value for IP3 is around 25 dB.

Results: IP3, Full scale, internal LO = 300 MHz to 3800 MHz

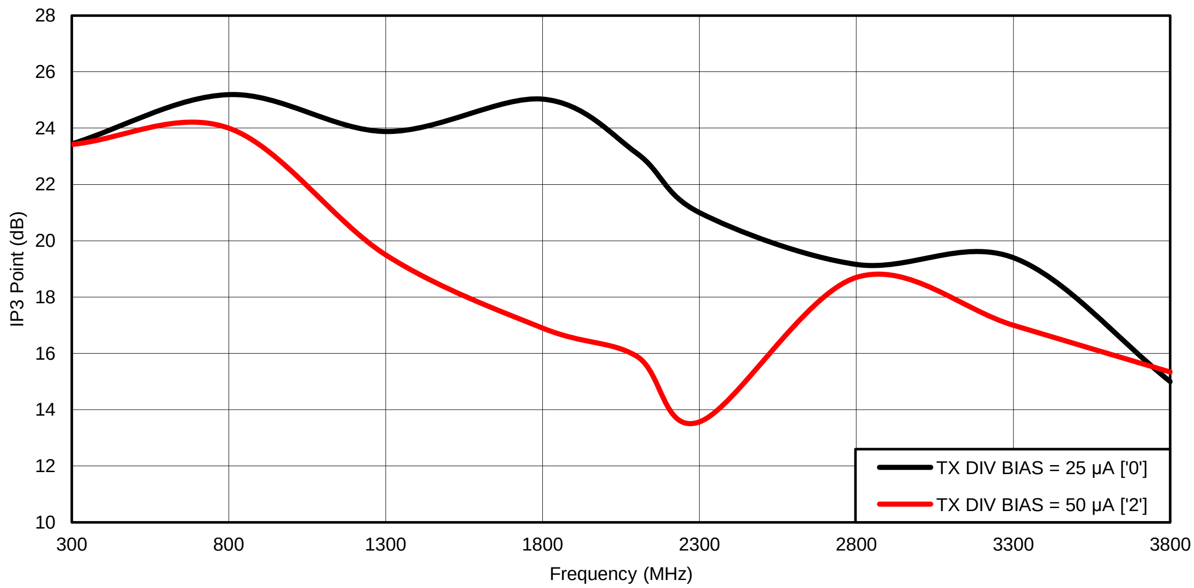

Figure 8. IP3 Plot – Internal LO

Figure 8 illustrates that the black graph (25 µA) has better IP3 values.

LO carrier Phase Noise

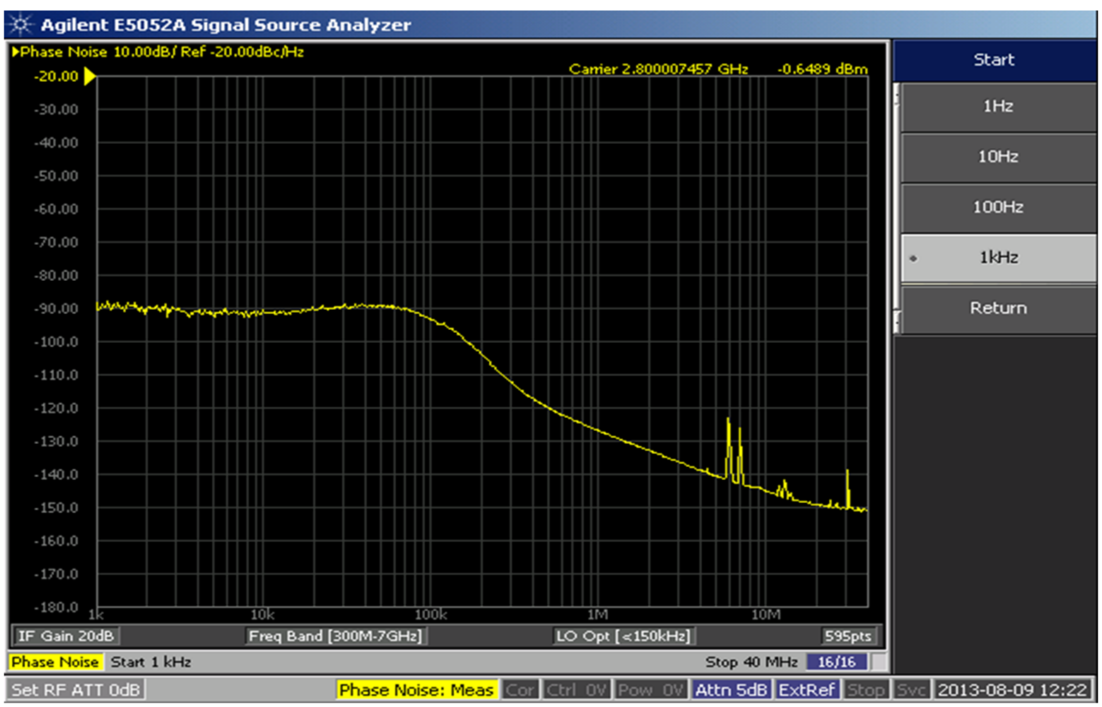

Figure 9. Phase Noise Plot – LO Carrier

NOTE: TI found better results of 3 dB more on both IP3 tests while using the IONIZER to reduce board temperature.

Due to cable connections, a loss of –1.41 dB in 300 MHz, –2.854 dB in 1.5 GHz, –4.084 dB in 2.8 GHz, –4.281 dB in 3.8 GHz is seen.

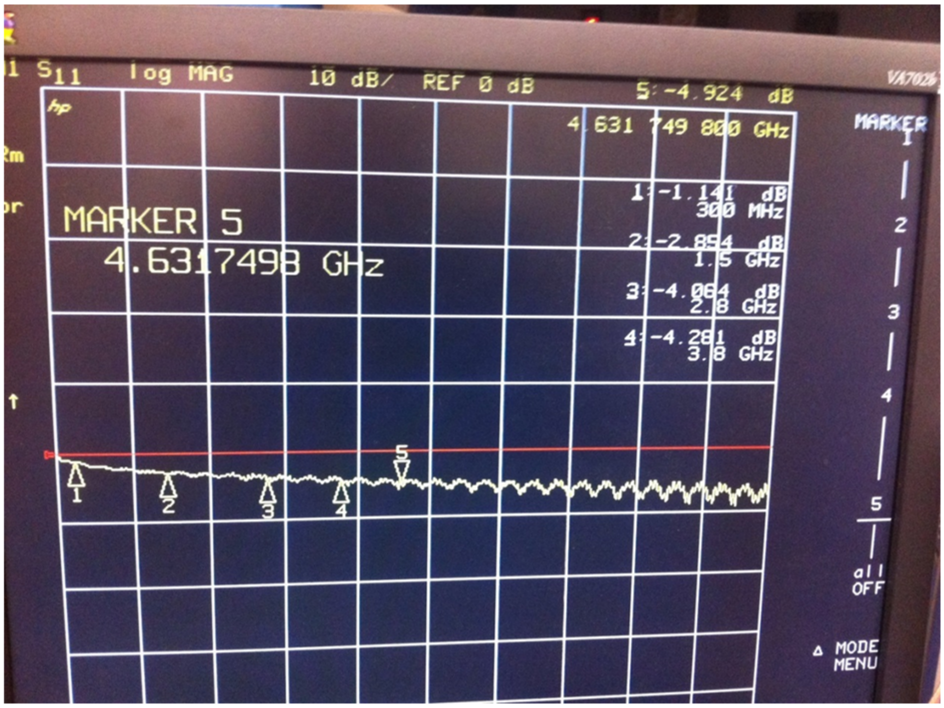

Figure 10. Cable Losses versus Frequency

1.1.5 Conclusion

The performance meets expectations as per the typical values in the TRF3720 datasheet (SLWS221). The module was operating without air flow and temperatures were significantly higher than room temperature. Performance is expected to improve with air flow.

1.2 External Test Results

1.2.1 Block Diagram External LO

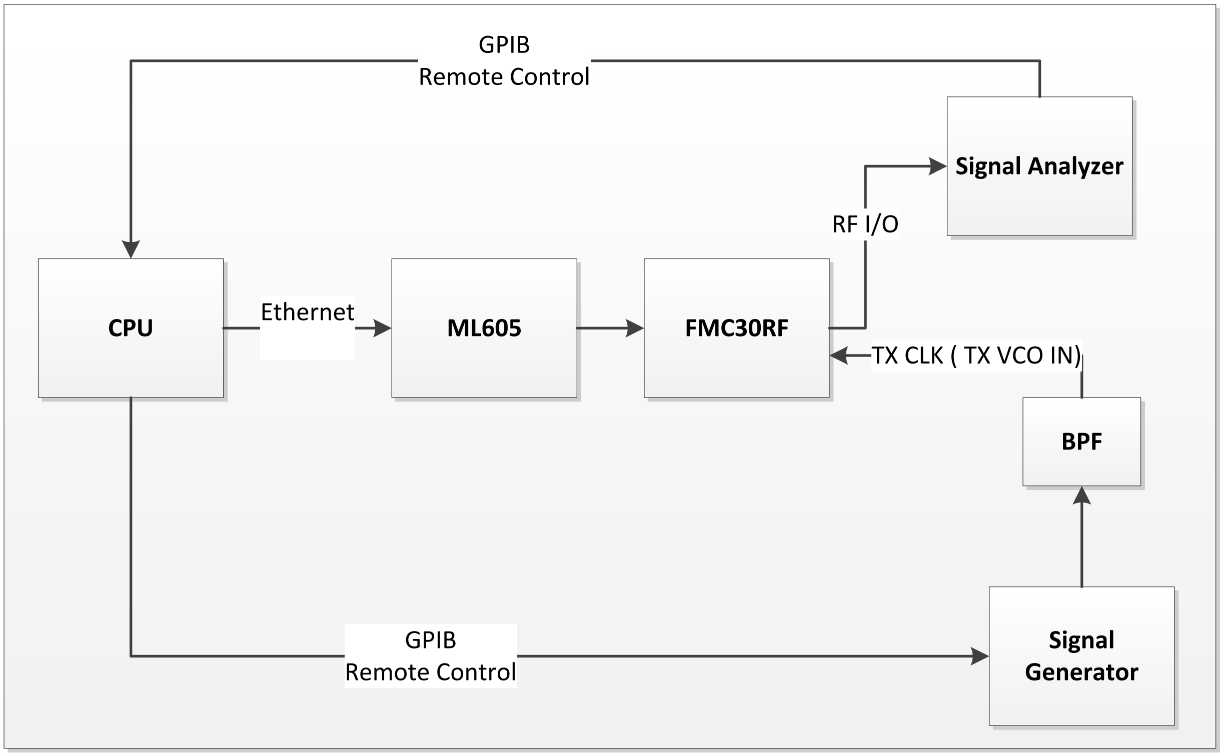

Figure 11. Block Diagram: External LO

1.2.2 Setup Description

As described in Section 1.1.2 – Section 1.1.4, the same test is performed but with external LO. In order to test the IQ Balance and IP3, the external VCO mode is set in the FMC30RF board.

A signal generator is set to sweep on the following external LO frequencies: 800, 900, 1000, 1100, 1250, 1350, 1500, 1600, 1750, 1850, 2000, 2100 MHZ.

For every frequency, four amplitude values (–5, 0, 5, and 10 dBm) are tested.

In order to reduce harmonics, a BPF connected to the output of the signal generator was used. The IF frequency is set = 10 MHz.

The RF I/O port is connected to FSQ 26 signal analyzer to take the measurement values. The whole system was controlled with MATLAB via GPIB. Differences were seen with and without the BPF in the output of the signal generator.

1.2.3 IQ-Balance Test Result

Figure 12 is the example plot from the signal analyzer:

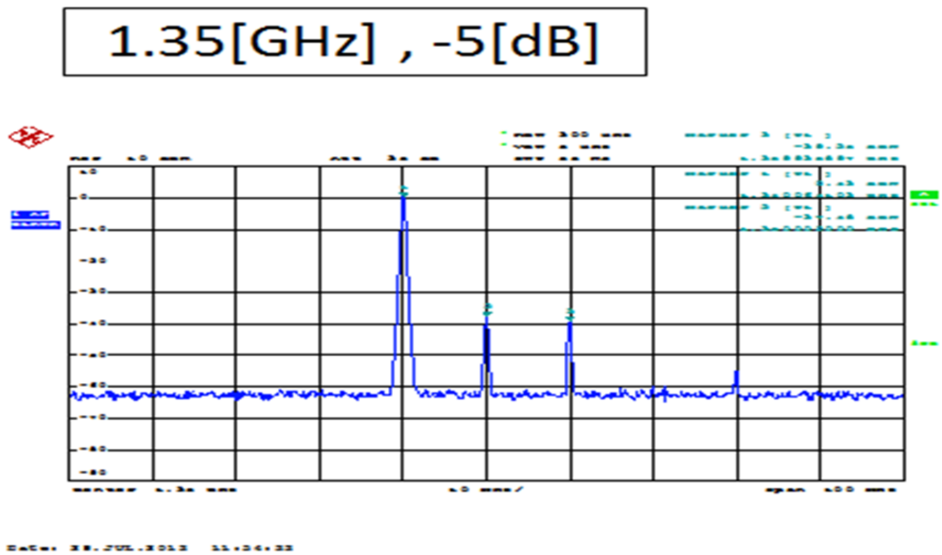

Figure 12. IQ Balance – Signal Analyzer Plot

As Figure 12 shows, there is a fundamental tone (marker ‘1’ in the plot), the LO frequency (marker ‘’2 in the plot), and the sideband tone (marker ‘3’ in the plot). The test checked the imbalance value (marker 1 amplitude – marker 2 amplitude ≥ 40 dB). The normal rejection values for TRF3720 are supposed to be around 40 dB.

Results: Full scaled signal, IF= 10 MHz, LO = 800 MHz to 2100 MHz.

Table 1. IQ Balance for Full Scaled Signal – External LO

IQ Balance –5 dBm		IQ Balance 0 dBm		IQ Balance 5 dBm		IQ Balance 10 dBm	
MHz	**dBc**	**MHz**	**dBc**	**MHz**	**dBc**	**MHz**	**dBc**
800	32.37	800	28.09	800	30.45	800	29.01
900	38.01	900	26.4	900	22.88	900	36.68
1000	34.51	1000	27.75	1000	19.39	1000	23.5
1100	32.26	1100	30.47	1100	19.63	1100	21.25
1250	27.68	1250	26.48	1250	20.64	1250	21.42
1350	39.68	1350	31.46	1350	23.22	1350	22.64
1500	45.87	1500	36.91	1500	26.61	1500	25.38
1600	32.21	1600	37.15	1600	30.84	1600	30.84
1750	48.16	1750	50.51	1750	37.98	1750	34.31
1850	46.74	1850	45.91	1850	43.79	1850	40.19
2000	49.91	2000	53.76	2000	52.59	2000	59.86
2100	40.25	2100	38.96	2100	34.74	2100	40.6

Each table has a different power amplitude from –5 dBm to 10 dBm.

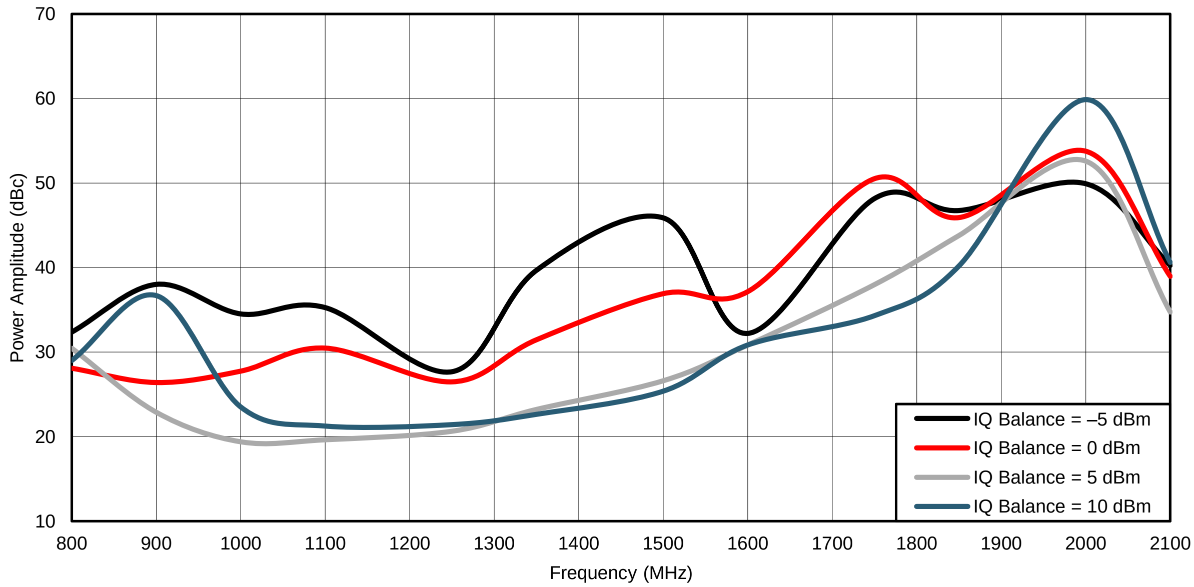

Figure 13. IQ Balance IF = 10 MHz Full Scaled Signal

Results: Full scaled –1-bit signal, IF= 10 MHz, LO = 800 MHz to 2100 MHz

Table 2. IQ Balance Table, Full Scaled –1-bit Signal – External LO

IQ Balance –5 dBm		IQ Balance 0 dBm		IQ Balance 5 dBm		IQ Balance 10 dBm	
MHz	dBc	MHz	dBc	MHz	dBc	MHz	dBc
800	32.9	800	29.28	800	31.27	800	28.11
900	39.14	900	27.31	900	22.73	900	37.88
1000	35.06	1000	28.29	1000	19.57	1000	23.92
1100	35	1100	31.62	1100	19.81	1100	21.64
1250	27.42	1250	26.93	1250	20.95	1250	21.49
1350	41.12	1350	32.58	1350	23.4	1350	22.84
1500	49.35	1500	39.61	1500	26.97	1500	25.36
1600	31.66	1600	36.27	1600	30.35	1600	28.18
1750	58.45	1750	49.91	1750	38.87	1750	35.04
1850	39.72	1850	41.22	1850	48.06	1850	40.89
2000	46.05	2000	51.84	2000	51.14	2000	55.24

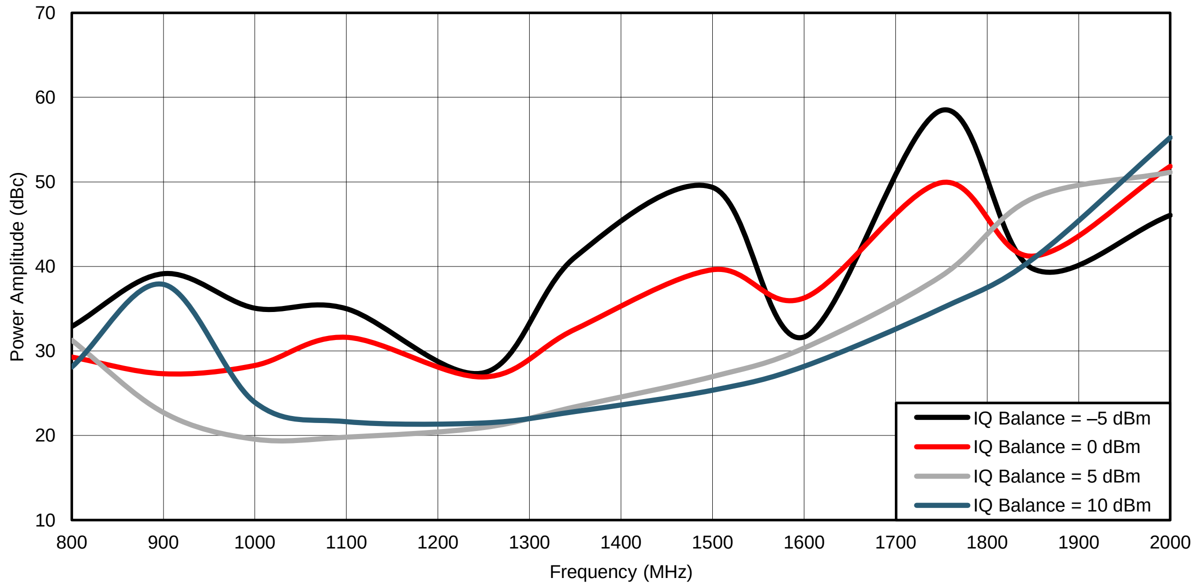

Figure 14. IQ balance, 2D Graph, Full Scaled – 1-bit IF= 10 MHz

1.2.4 IP3 Test Result

As described in Section 1.1.1.2, two tones were created with MATLAB as the signal generator with the same power and transmitted them through the DAC inside the AFE7225 and through the TRF3720 to the spectrum analyzer.

In this section the system (FMC30RF board) is tested with external LO. In order to test the system reaction for two tones the external VCO mode is set in the FMC30RF board. The LO frequencies are: 800,900,1000,1100,1250,1350,1500,1600,1750, and 1850 MHZ. The two tones were tested in full scale signal. The rest of the setting is the same as in IQ balance test.

Here is an example plot from the output of the RF chain (MATLAB in CPU → ML605 → AFE7225 (DAC) → TRF3720 → signal analyzer.

Results: IF = 10 MHz, LO = 800 MHz to 2000 MHz

Table 3. IP3 Table – External LO

TOI –5 dBm		TOI 0 dBm		TOI 5 dBm		TOI 10 dBm	
MHz	dBc	MHz	dBc	MHz	dBc	MHz	dBc
800	26.17	800	26.25	800	26.19	800	26.03
900	25.64	900	26.08	900	26.18	900	26.21
1000	26.52	1000	26.7	1000	26.14	1000	26.49
1100	26.38	1100	26.36	1100	26.11	1100	25.74
1250	26.29	1250	26.54	1250	24.99	1250	24.76
1350	24.83	1350	25.12	1350	24.44	1350	24.62
1500	22.68	1500	22.89	1500	23.42	1500	23.71
1600	25.5	1600	25.71	1600	27.47	1600	27.06
1750	28.6	1750	28.7	1750	27.26	1750	26.88
1850	27.83	1850	28.01	1850	27.9	1850	26.03
2000	25.83	2000	24.95	2000	23.88	2000	59.86

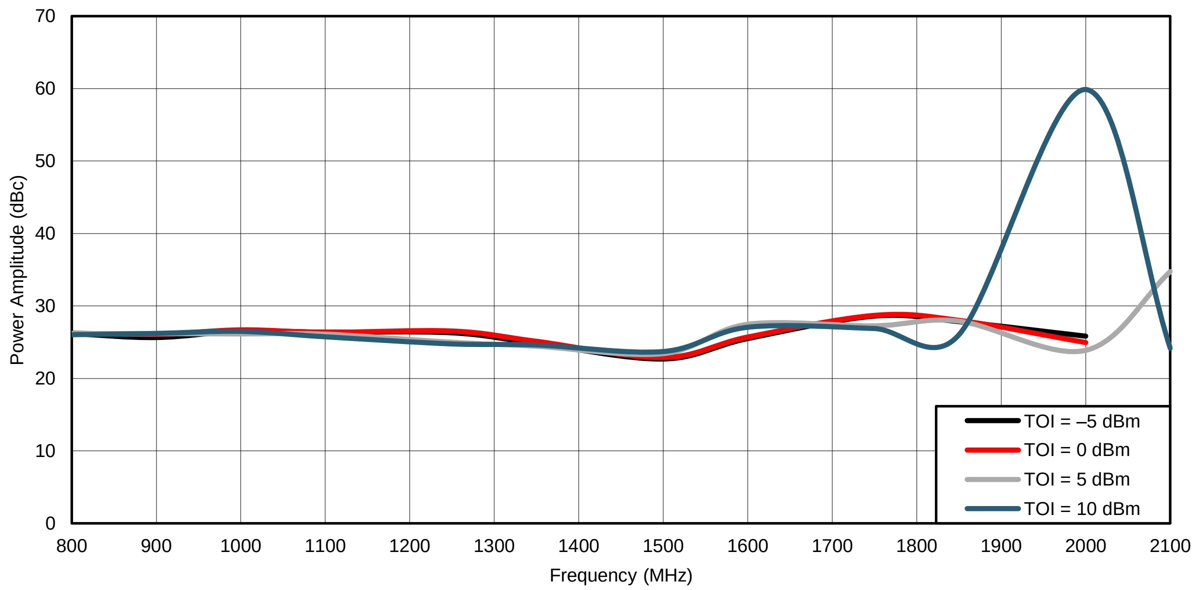

Figure 15. TOI – External LO

As described in the TRF3720 datasheet, the values are as the expected. (around 25 dB)

There is a 3-dB cable loss (changes through the frequencies)

1.3 ACPR – LTE Signal, Base Band 5 MHz, 10 MHz, 20 MHz

1.3.1 Test Description

5-, 10-, 20-MHz baseband LTE *full scale* signals were created with a pattern generator (TSW3100). Another set of 5/10/20 MHz baseband LTE *full scale-6dB* signals were created in the same way. An automation process was done with MATLAB (set and run the exe file from visual C, control the FSQ and the signal generator). The signal generator was used only in external VCO test.

The following graphs describe the results from these tests:

1. TX power – Full scale versus [Full scale – 6 dB], (2 graphs – internal and external).
2. Adjacent channel – Full scale versus [Full scale – 6 dB], (2 graphs – internal and external).
3. Alternate channel – Full scale versus [Full scale – 6 dB], (2 graphs – internal and external).

While testing with the external VCO, the amplitude is ‘0’ [dBm] .

The FSQ BW and spacing has been set according to the standard values:

- For 5 MHz BB: BW = 4.515 MHz, spacing = 5 MHz
- For 10 MHz BB: BW=9.015 MHz, spacing = 10 MHz
- For 20 MHz BB: BW=18.015 MHz, spacing = 20 MHz

1.3.2 Internal LO versus External LO for TX Channel

Results: Internal LO: TX Channel Full scale versus [Full scale – 6 dB]

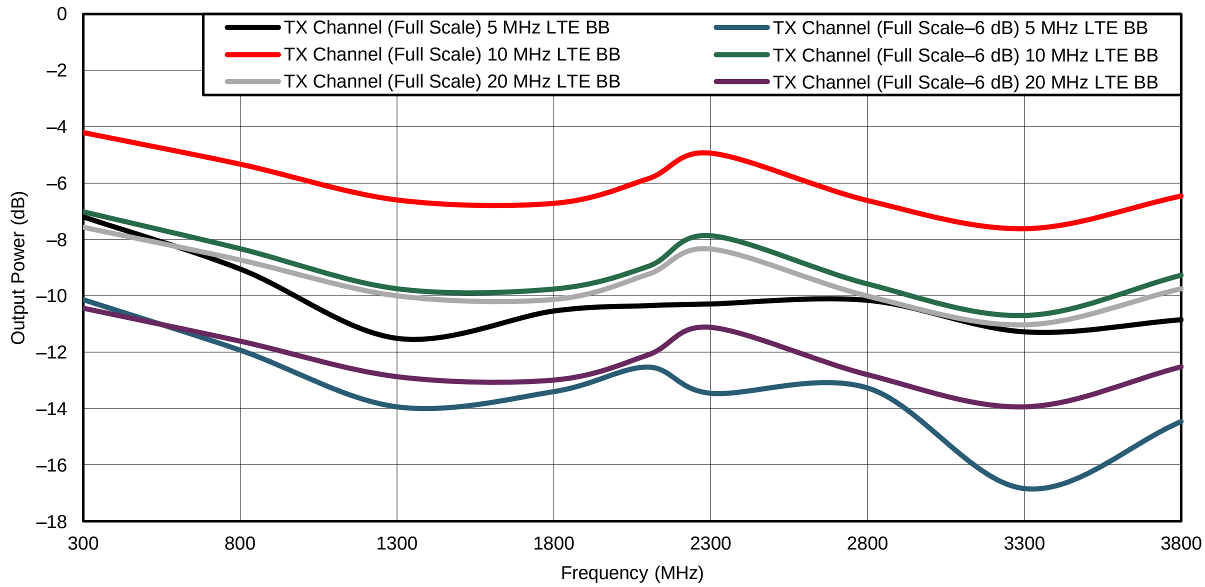

Figure 16. Internal LO – TX Channel Full Scale versus [Full Scale – 6 dB]

Results: External LO: TX Channel Full scale versus [Full scale – 6 dB]

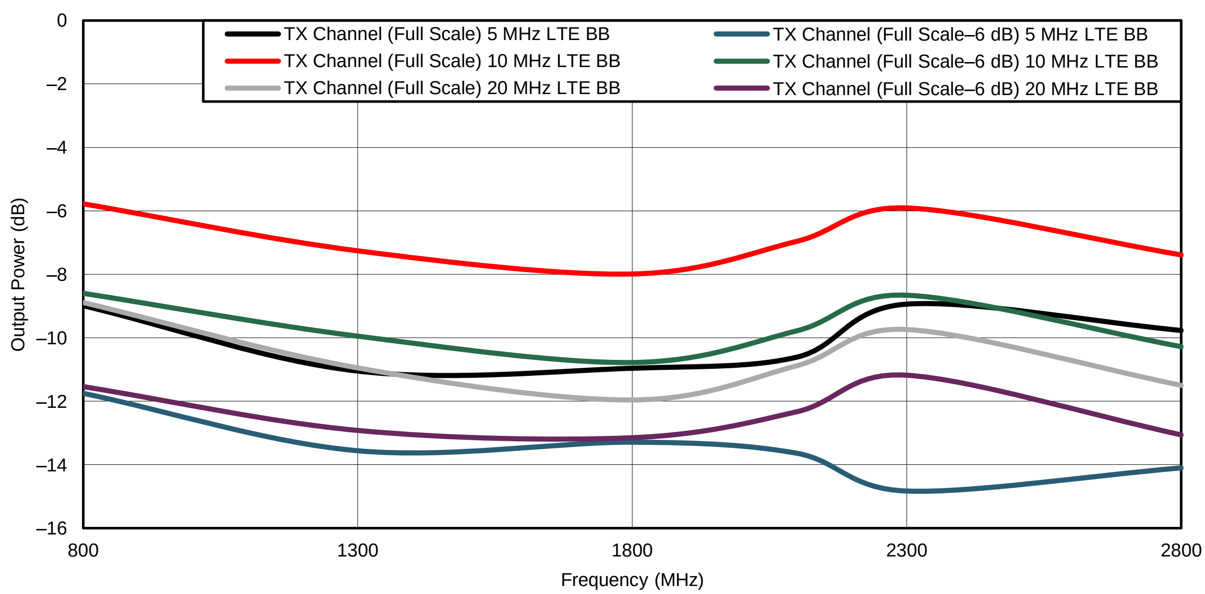

Figure 17. External LO: TX Channel Full Scale versus [Full scale – 6 dB]

1.3.3 Internal LO versus External LO for: Adjacent channel

Adjacent channel power ratio (ACPR) is a critical measurement, for many transmission standards (IS-95 CDMA, WCDMA, IS-54 NADC, and so forth). This test characterized the distortion and defines the interference with neighboring radio. As in the IP3 test, there is a product from the 3rd order that falls inside the band. The main goal of this test is to make sure that while transmitting the LTE signal, the parts that fall outside the bandwidth will not interfere with other LTE signals.

Normally, the lower values attained, the better the results for this test as shown in Figure 18 and Figure 19.

Results: Internal LO: TX Channel Full scale versus [Full scale – 6 dB]

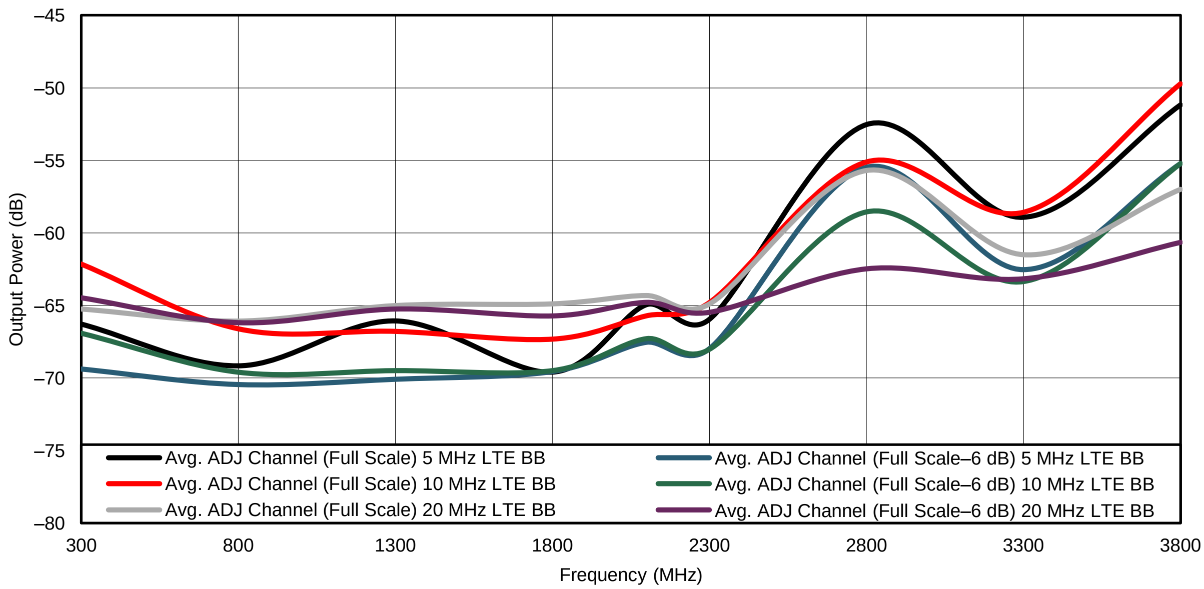

Figure 18. Adjacent Channel – Internal LO

Results: External LO: TX Channel Full scale versus [Full scale – 6 dB]

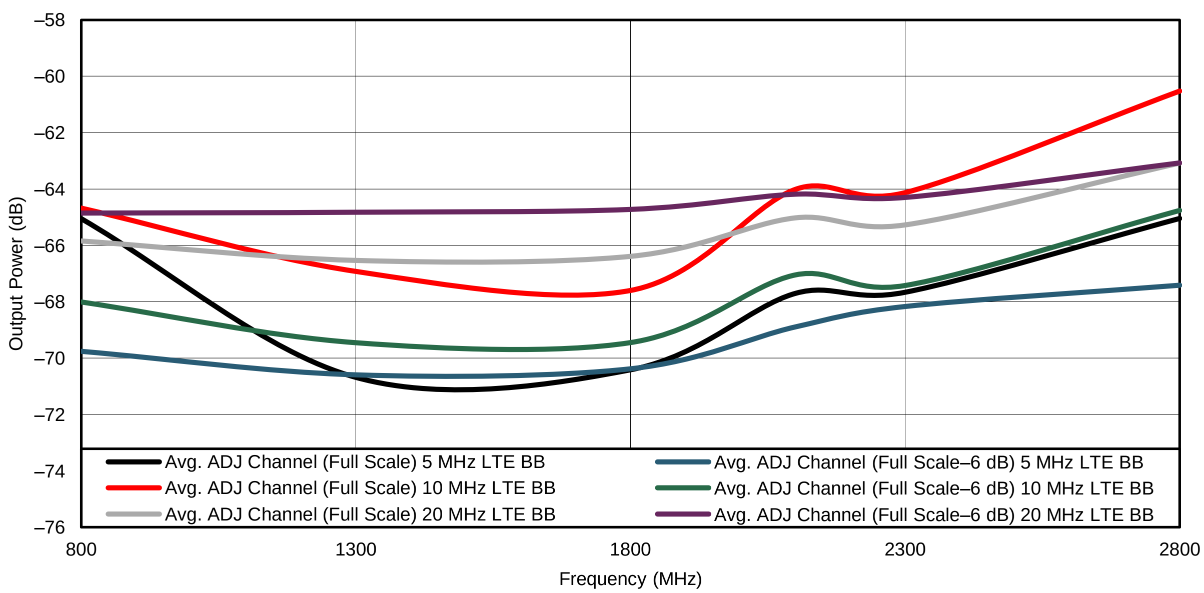

Figure 19. Adjacent Channel – External LO

1.3.4 Internal LO versus External LO for: Adjacent Channel

Results: Internal LO: Alternate Channel Full scale versus [Full scale – 6 dB]

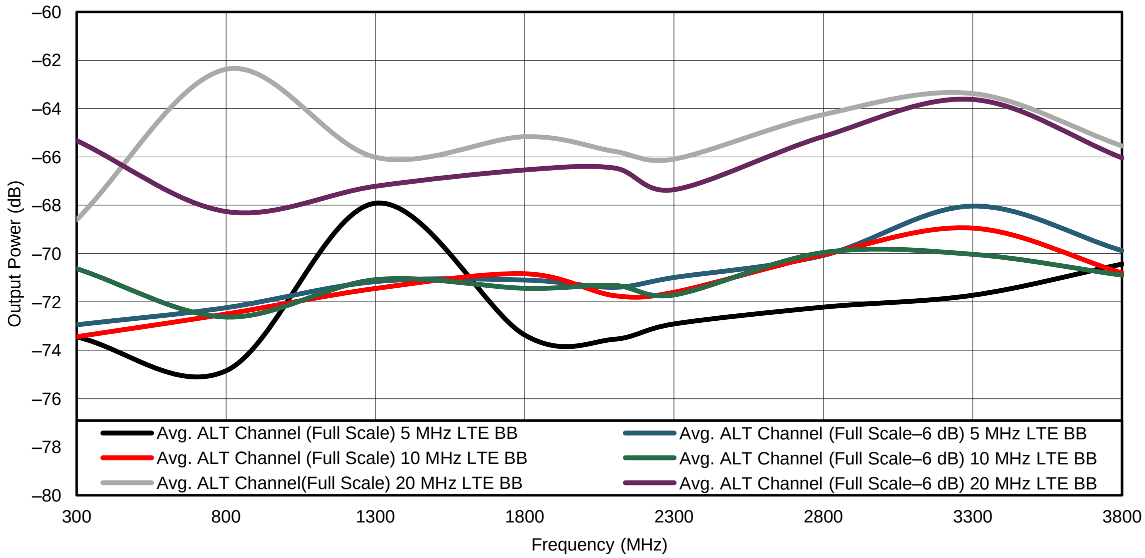

Figure 20. Internal LO: Alternate Channel

Results: External LO: Alternate Channel Full scale versus [Full scale – 6 dB]

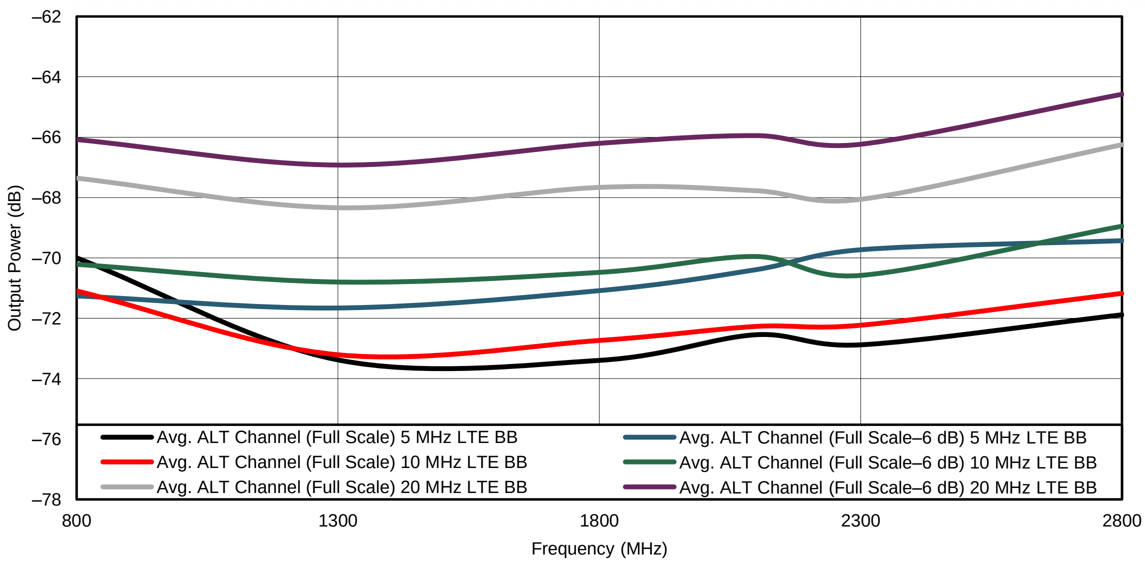

Figure 21. External LO – Alternate Channel

1.4 Conclusion

In this section the IQ Balance and the third order intercept points are tested for internal and external LO. While comparing a full scaled signal and a back off signal with 6 dB, the performance meets expectations for the typical values in the TRF3720 data sheet.

In the last test performed on an LTE signal when measuring the adjacent channel, the power channel and the alternate channel – there is some rising in the result on the 2800 MHz, but besides that, the results meets the expectation.

2 RX Path

2.1 IQ Balance Test

2.1.1 Block Diagram Internal LO

Figure 22 illustrates the complete system set up, including the ML605 board which is connected from one side to a computer via Ethernet cable and from the other side to the FMC30RF board The signal generator is used to generate the input RF signal and the internal and external VCO mode in TRF3765 is set alternately in the tests.

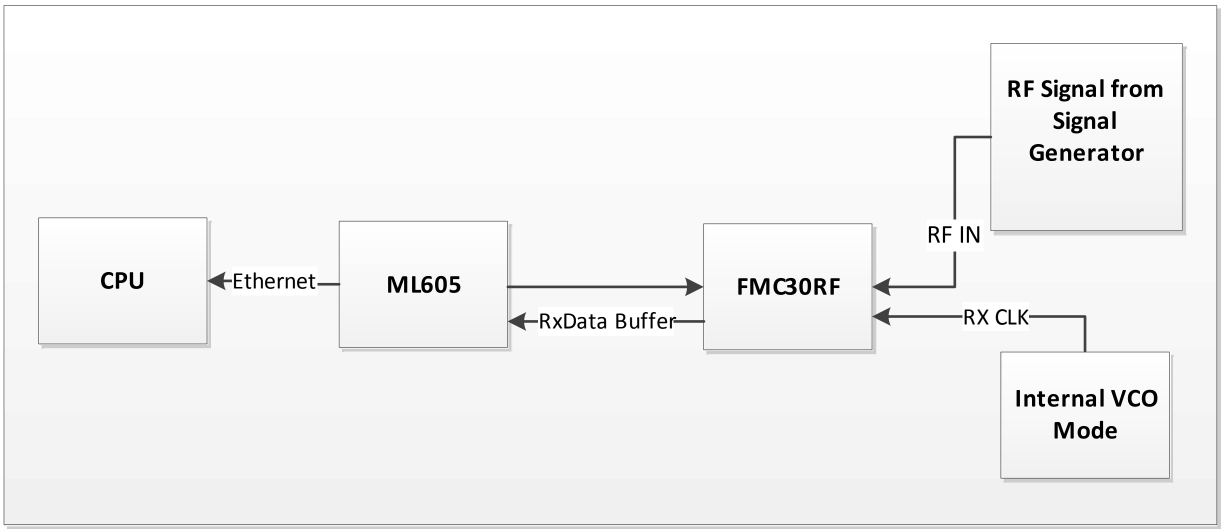

Figure 22. Block Diagram Internal LO

The firmware is burned on the FPGA which located inside the ML605 board by using the Xilinx design tool. After burning the firmware, the FMC30RF board can be accessed to take RX measurement. The block diagram of the FMC30RF board (with “4 DSPs) is shown in Figure 23.

In order to take the RX measurement we will use the following parts inside the FMC30RF board:

- AFE7225 – used the ADC inside it to receive a IQ signal and save it in a buffer (RXData.txt)
- TRF3765 – used to generate the LO into the TRF3711, working with two modes – internal LO and External LO
- TRF3711 – used as demodulator, received the RF signal after gaining it with 1 low-noise amplifier (LNA) from the signal generator, and a LO from TRF3765, in the output of this device there are I/Q signals
- CDC62005 – used to generate references to the AFE7225, TRF3765, and TRF3711

While testing the hardware with internal LO, the TRF3765 was set to “RX_VCO_OUT“ (port 4) and “RX IN” (port 3) was connected to the signal generator as shown Figure 22. The second LNA remained bypassed. The attenuator is set to minimum and maximum values

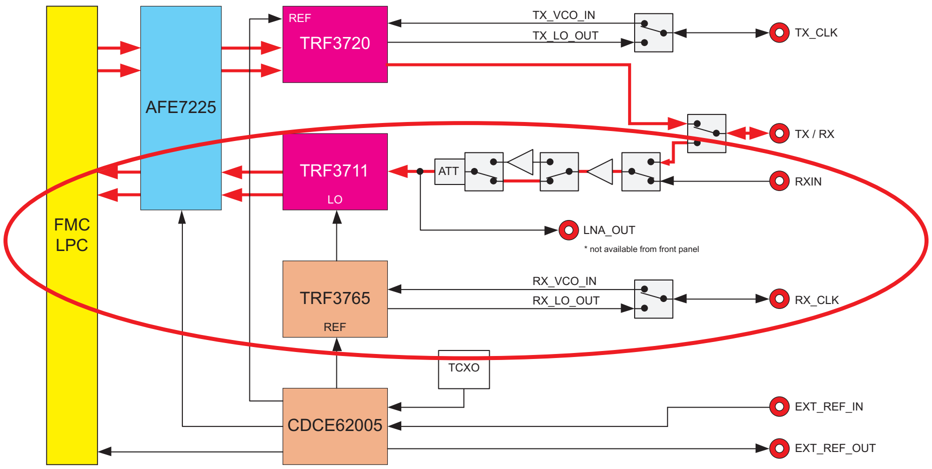

Figure 23. FMC30RF Block Diagram

2.1.2 Setup Description

Prior to this test a line up analysis was performed to know which gain is expected and which IP3 value should be received (best theoretical values). In order to test the IQ balance, the following settings are used:

1. TR3765 is set to internal LO mode and the following frequencies are swept: 1500, 2140, 2800, 3300, 3800 MHz.
2. The attenuator before TRF3711 is set to minimum (0 dB) in the first half of the tests and set to maximum attenuation (31 dB) in the last half.
3. Inside TRF3711, four BB gain settings were used (0, 5, 15, 24 dB) and the results are from these different types of gains and also from EN/D is the 3-dB attenuator.
4. The following RF frequencies were tested: 1500, 2140, 2800, 3300, 3800 MHz with a different amplitude pin [0, –20, –30, and –50 dBm] for each of the previous settings.
5. The IF frequency is set to 5 MHz.
6. MATLAB was used to automate the process using BPF on the RF signal.

Figure 24 shows an example plot for IQ balance test with 5 MHz IF.

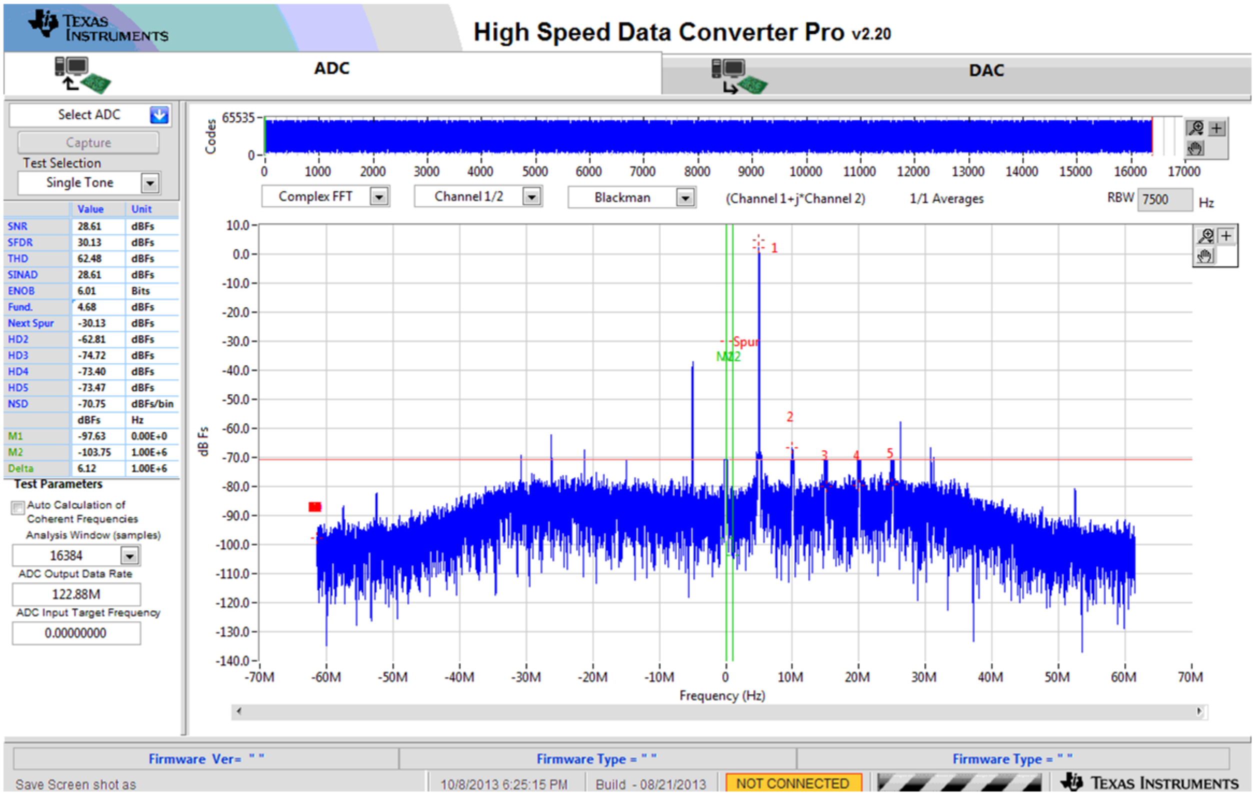

Figure 24. IQ Balance – Internal LO 5 MHz IF

The system:

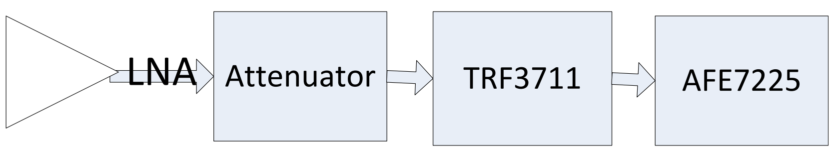

Figure 25. RX Signal Chain Block Diagram

Max/Min attenuation refers to the attenuator values.

Base Band gain (BB Gain) and EN/DIS 3-dB attenuation refers to the gain inside the TRF3711.

The different settings for all the tests are listed in the following table:

Setting	Total Gain
Max attenuation _ BB gain zero, EN 3-db attenuation	0
Max attenuation _ BB gain 5, EN 3-db attenuation	5
Max attenuation _ BB gain 15, EN 3-db attenuation	15
Max attenuation _ BB gain 24, EN 3-db attenuation	24
Max attenuation _ BB gain zero, 3-db attenuation off	3
Max attenuation _ BB gain 5, 3-db attenuation off	8
Max attenuation _ BB gain 15, 3-db attenuation off	18
Max attenuation _ BB gain 24, 3-db attenuation off	27
Min attenuation _ BB gain zero, EN 3-db attenuation	31
Min attenuation _ BB gain 5, EN 3-db attenuation	36
Min attenuation _ BB gain 15, EN 3-db attenuation	46
Min attenuation _ BB gain 24, EN 3-db attenuation	55
Min attenuation _ BB gain zero, 3-db attenuation off	34
Min attenuation _ BB gain 5, 3-db attenuation off	39
Min attenuation _ BB gain 15, 3-db attenuation off	49
Min attenuation _ BB gain 24, 3-db attenuation off	58

2.1.3 Internal LO Test Result

The plots in Figure 26 through Figure 29 show that you can choose the desired setting (16 options) and the results are around 35–40 dB for the IQ Balance test.

Do not work below RF Frequency = 1000 MHz because the LNA is designed to work well below 1 GHz.

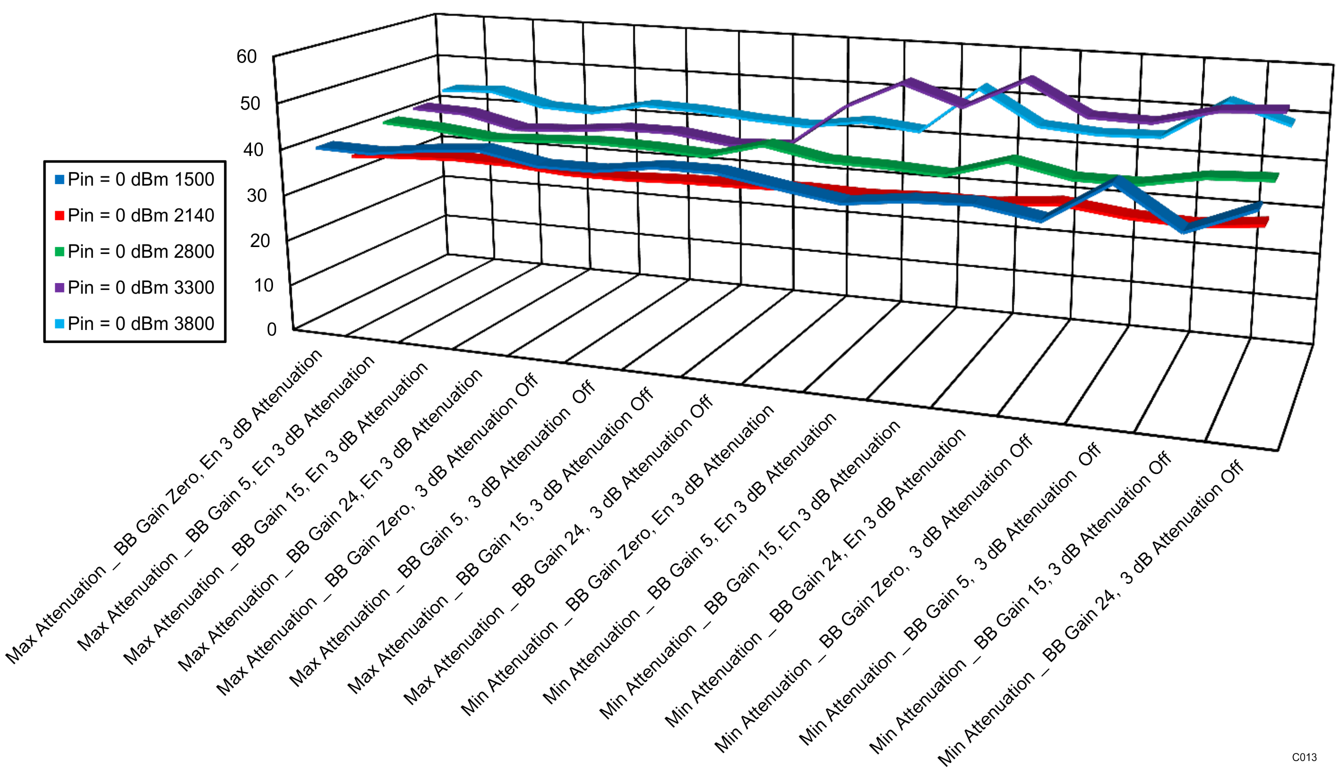

Figure 26. IQ Balance Internal LO, Pin = 0 dBm

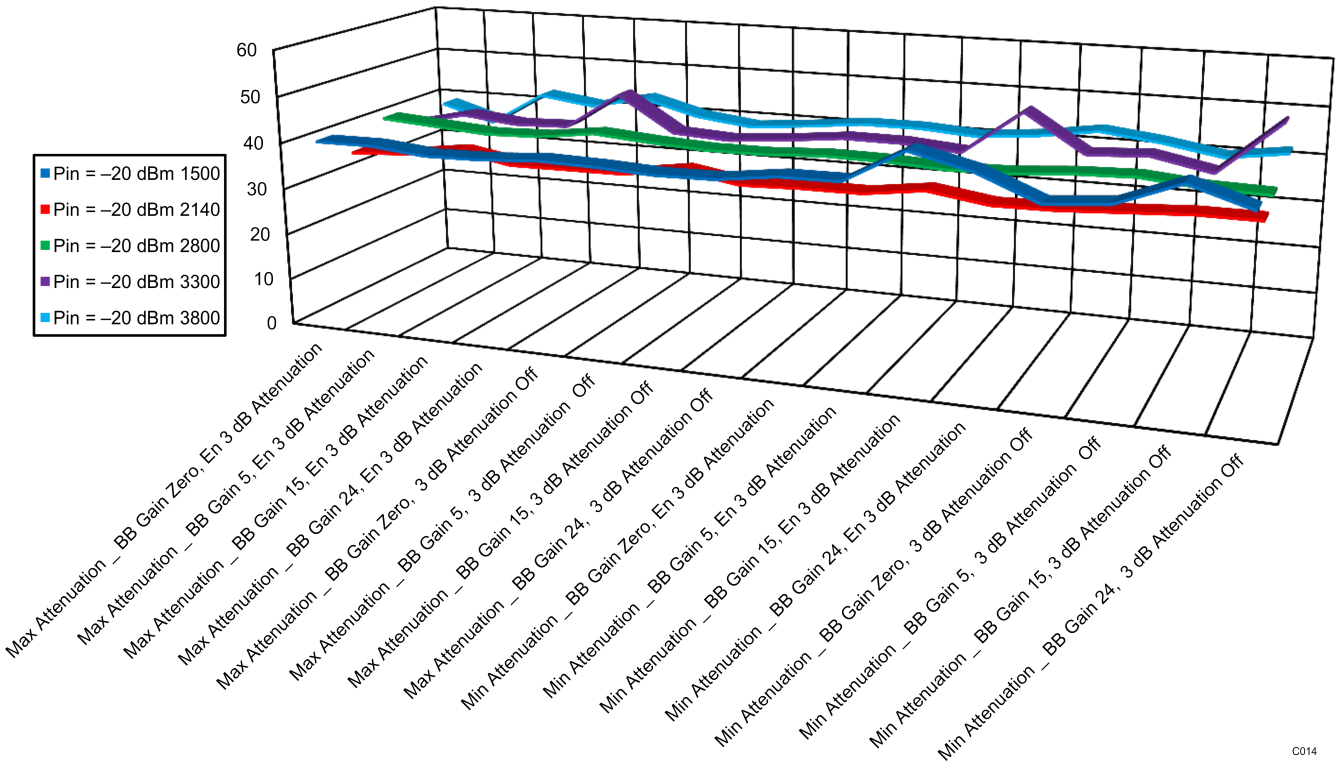

Figure 27. IQ Balance Internal LO, Pin = –20 dBm

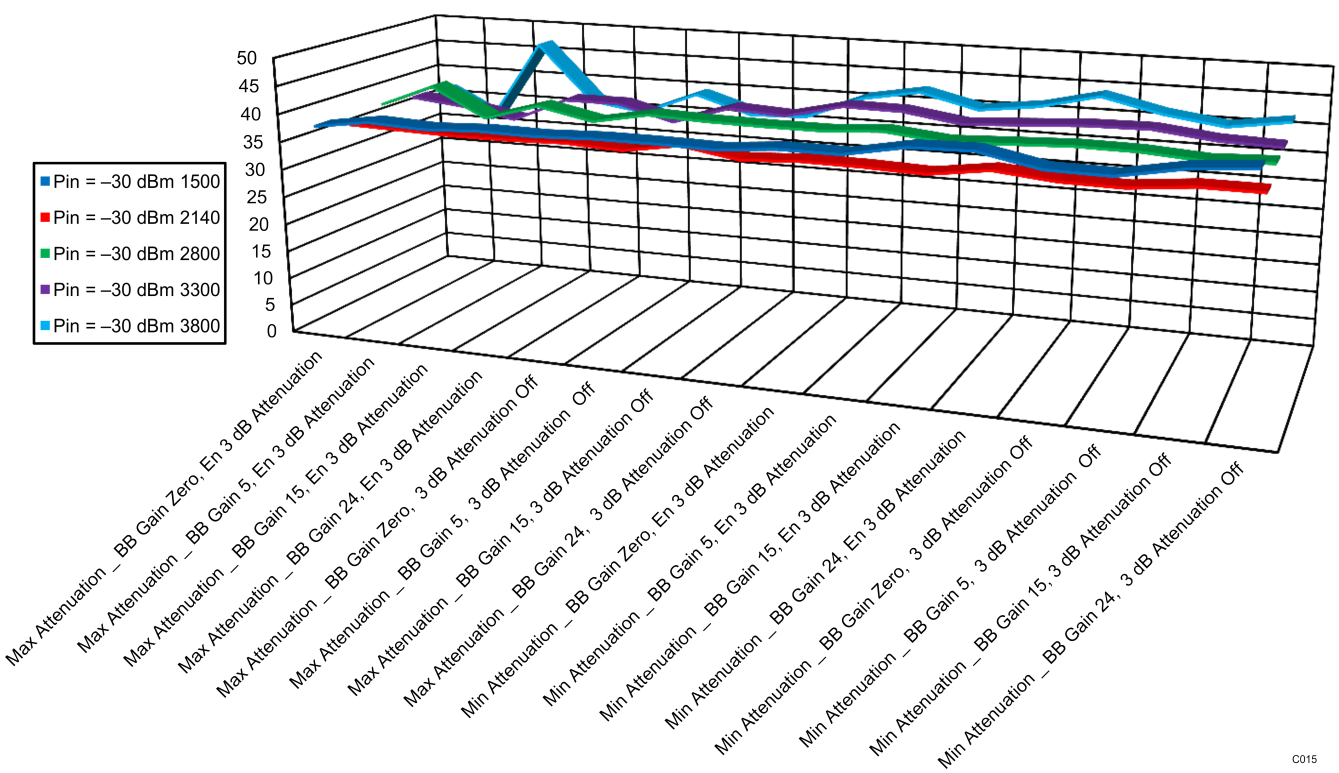

Figure 28. IQ Balance Internal LO, Pin = –30 dBm

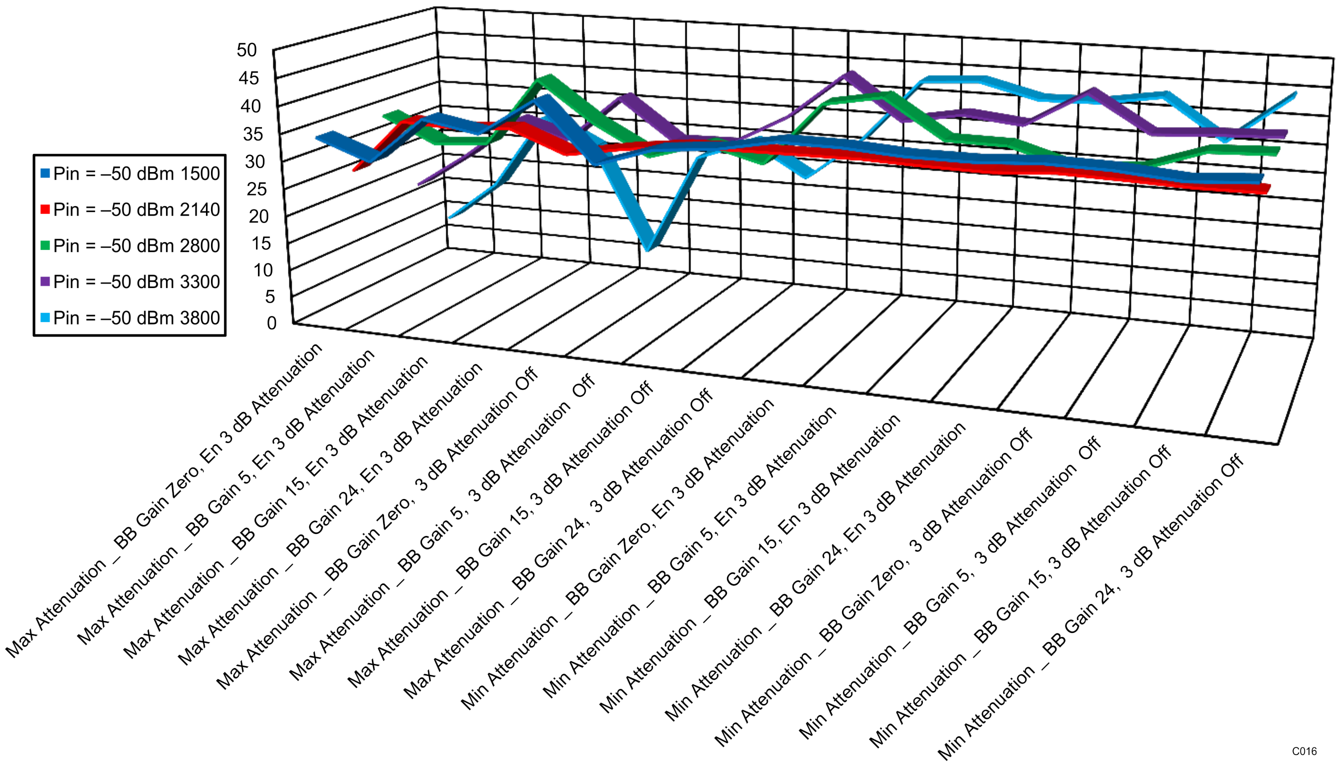

Figure 29. IQ Balance Internal LO, Pin = –50 dBm

2.1.4 Block Diagram External LO

Figure 30 illustrates the complete system set up.

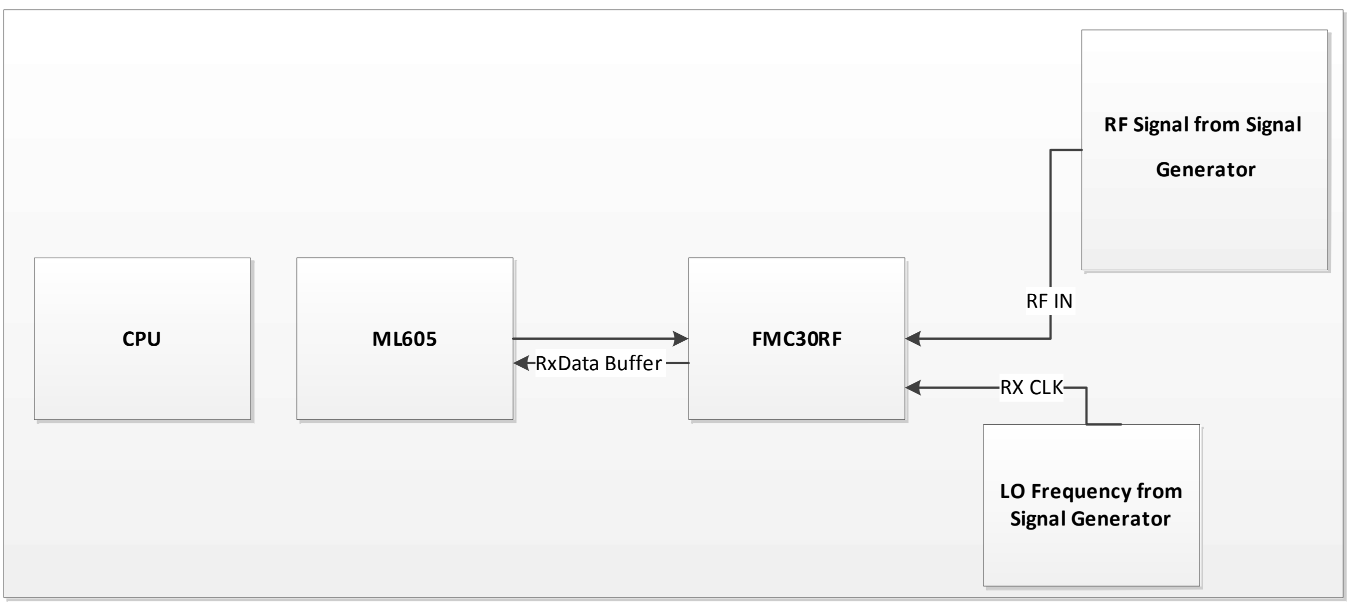

Figure 30. External LO Block Diagram

The firmware is burned on the FPGA located inside the ML605 board by using the Xilinx design tool. After burning the firmware we can access to the FMC30RF board to take RX measurements. The block diagram of the FMC30RF board (with 4 DSPs) is shown in Figure 31.

In order to take the RX measurement the following parts inside the FMC30RF board are used:

- AFE7225 – used the ADC inside it to receive a IQ signal and save it in a buffer (RXData.txt)
- TRF3765 – used to generate the LO into the TRF3711, we worked with two modes – internal LO and External LO
- TRF3711 – used as demodulator – received RF signal after gaining it with 1 LNA from the signal generator, and an LO from TRF3765, in the output of this device we have an I/Q signals
- CDC62005 – used to generate references to the AFE7225, TRF3765, and TRF3711

While testing the hardware with external LO, the TRF3765 was set to Ext VCO (*RX_VCO_IN*-port 4) and to signal generator. RX IN (port 3) was connected to the signal generator as shown in Figure 30.

The second LNA remained bypassed. The attenuator is set to minimum and maximum values.

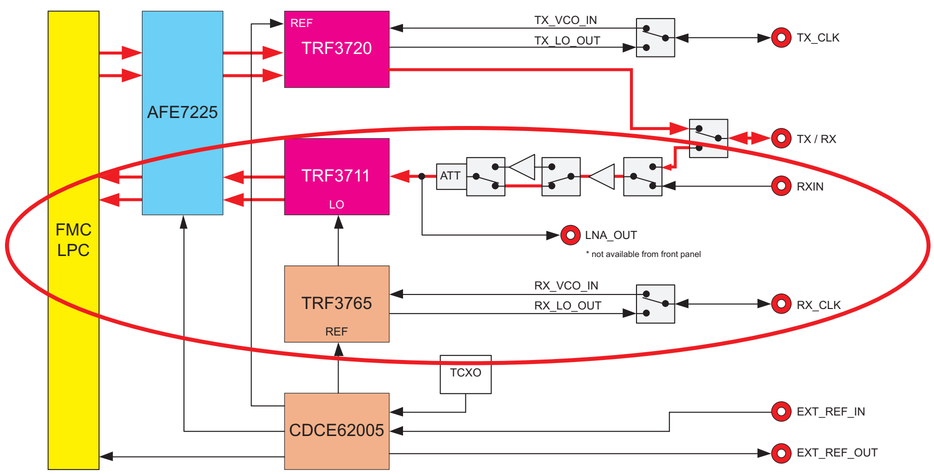

Figure 31. FMC30RF Block Diagram RX Path

2.1.5 Setup Description

The following settings were used to test the IQ balance:

1. TR3765 is set to **External LO mode** and swept at the following frequencies: 1500, 2140, 2800, 3300, and 3800 MHz via signal generator.
2. The attenuator before TRF3711 is set in 8/16 setting to minimum (0 dB) and in 8/16 setting to maximum attenuation (31 dB).
3. Inside TRF3711, four BB gain settings were used (0-, 5-, 15-, 24-dB gain) and also EN/DIS the 3-dB attenuator.
4. We tested these RF frequencies: 1500, 2140, 2800, 3300, 3800 MHz, with different amplitude pin [0, –20, –30, –50 dBm] for each of the setting above.
5. The IF frequency is set to 5 MHz.
6. MATLAB was used to automate the process and BPF was used on the RF signal.

Figure 32 through Figure 35 show the results:

2.1.6 External LO Test Result

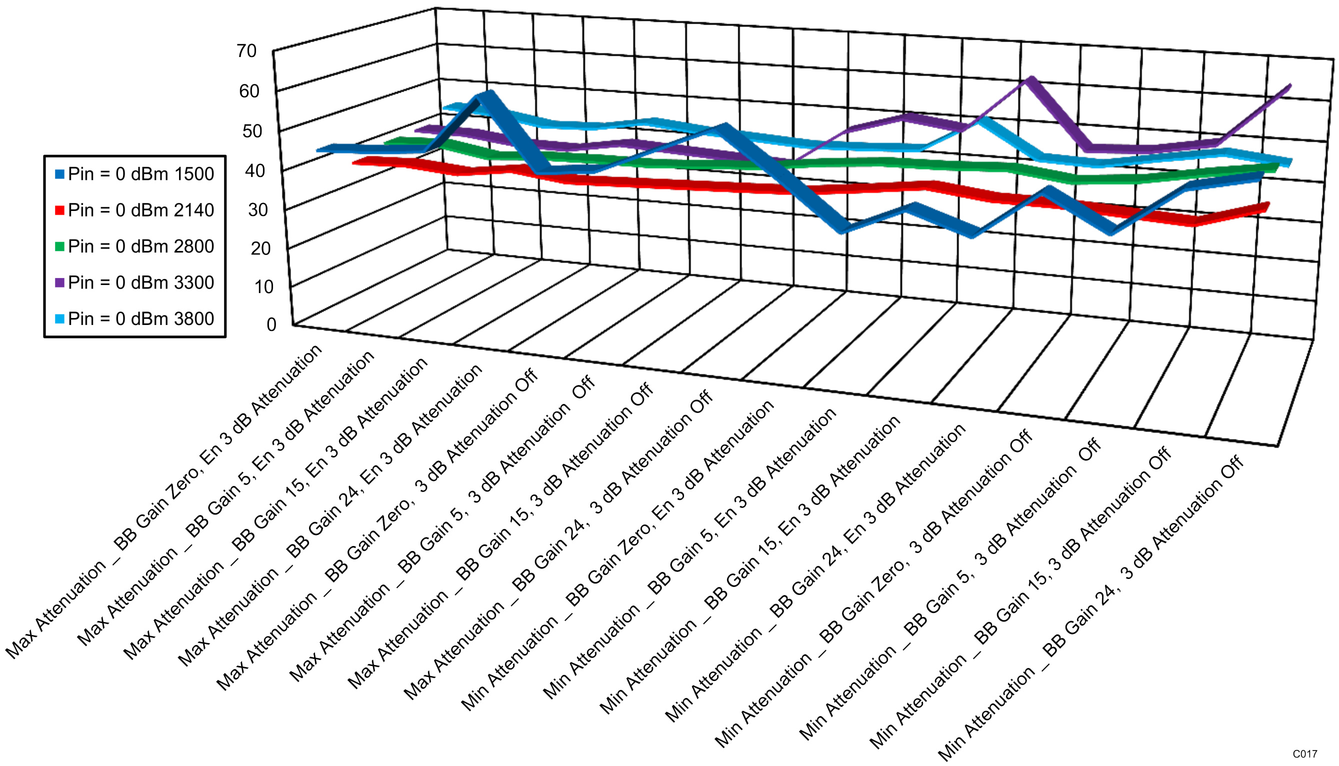

Figure 32. IQ Balance External LO, Pin = 0 dBm

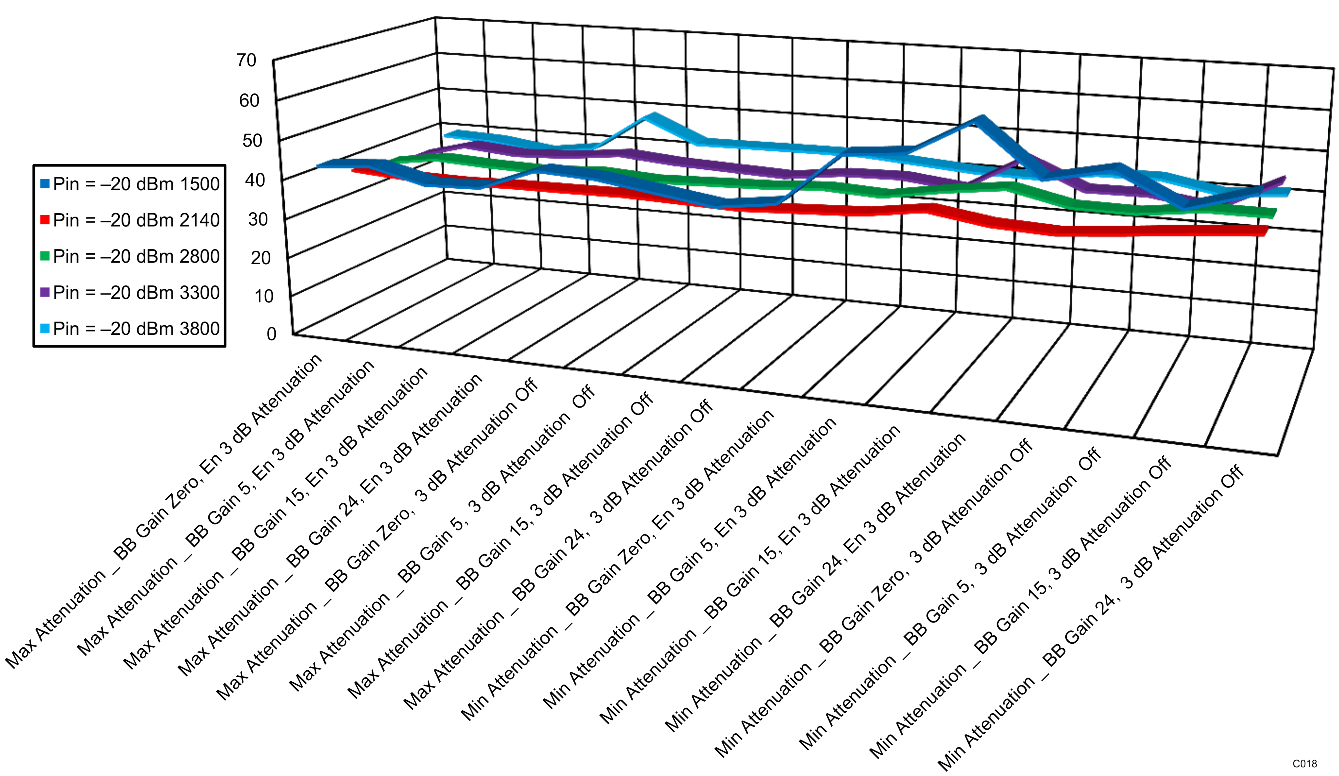

Figure 33. IQ Balance External LO, Pin = –20 dBm

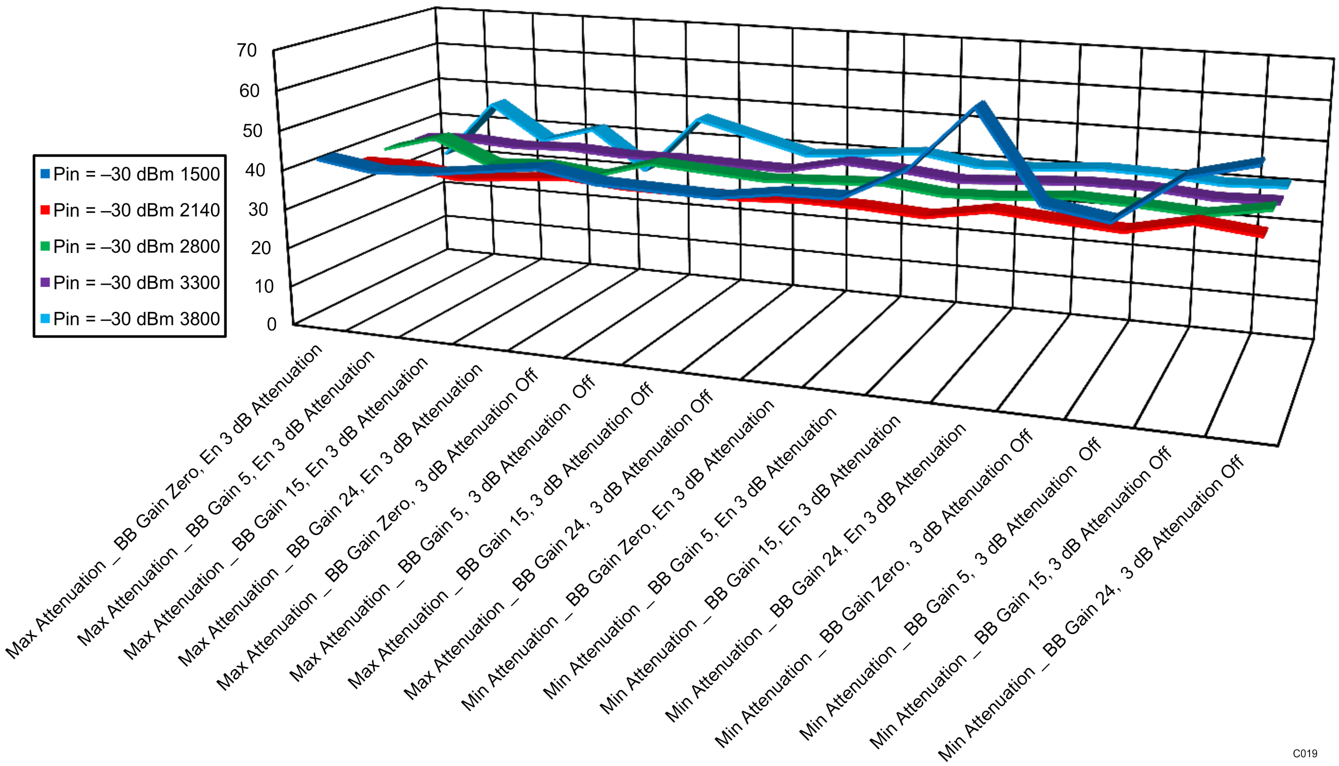

Figure 34. IQ Balance External LO, Pin = –30 dBm

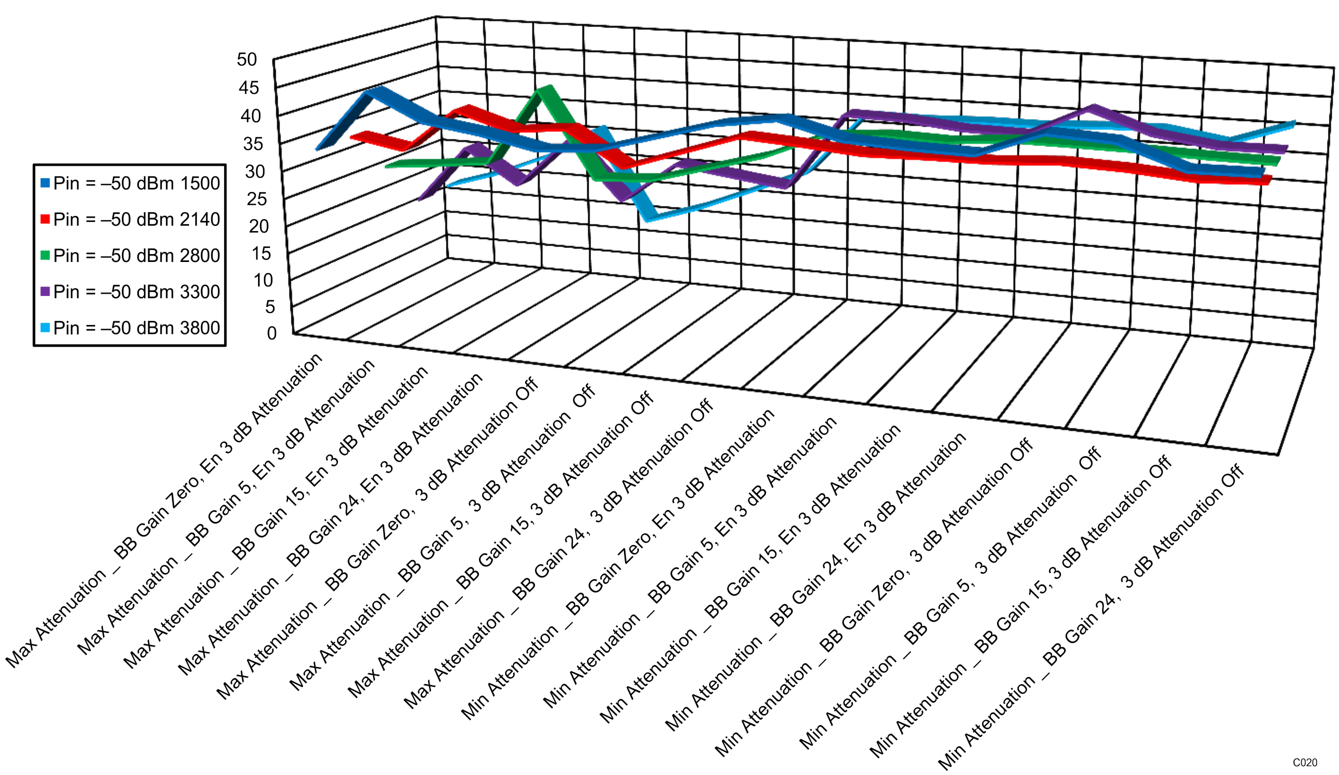

Figure 35. IQ Balance External LO, Pin = –50 dBm

2.1.6.1 Summary for IQ Balance Test

We tested the hardware with internal and external VCO – and the result are around these values 30–40 dB, it is expected to be in this range there for we can say the results are good.

The result are expected to be even better if using the IQ correction firmware.

The LNA was designed for a minimum value of Fin = 1 GHz, therefore, it is recommended not to work below that frequency.

2.2 IP3 Test

2.2.1 Block Diagram Internal / External LO

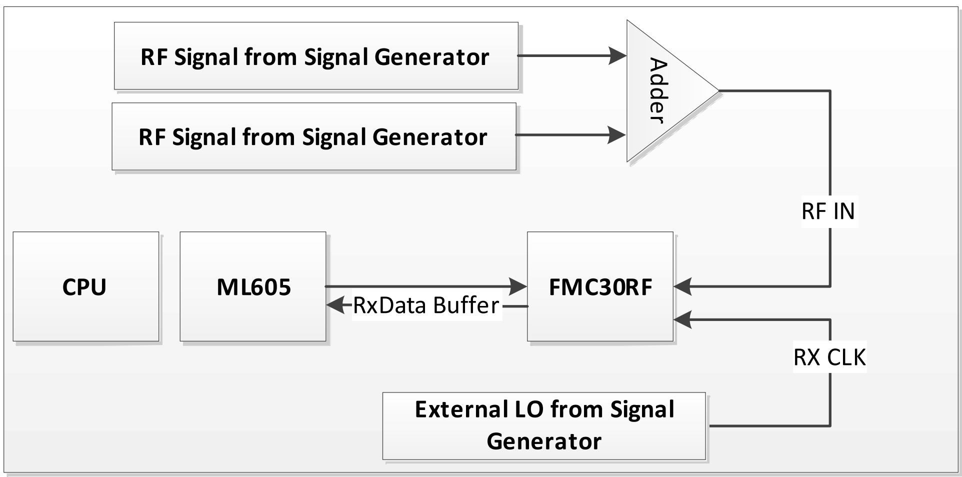

Figure 36. Block Diagram Internal / External LO

In the RX path, the following parts were used: AFE7225, TRF3711, and TRF3765. While testing the hardware with external LO, the TRF3765 is set to Ext VCO (RX_VCO_IN – port 4) and to signal generator and while testing with internal LO the TRF3765 was set to work in that mode. “RX IN” (port 3) was connected to signal generator as shown in Figure 36.

TI combined two signal generators to create the OIP3 response and then used the following formula:

IIP3 = OIP3 – Gain (IIP3 and OIP3 are 3rd-order intercept points referring to input and output, respectively) (1)

The second LNA remained bypassed. The attenuator is set to minimum and maximum values.

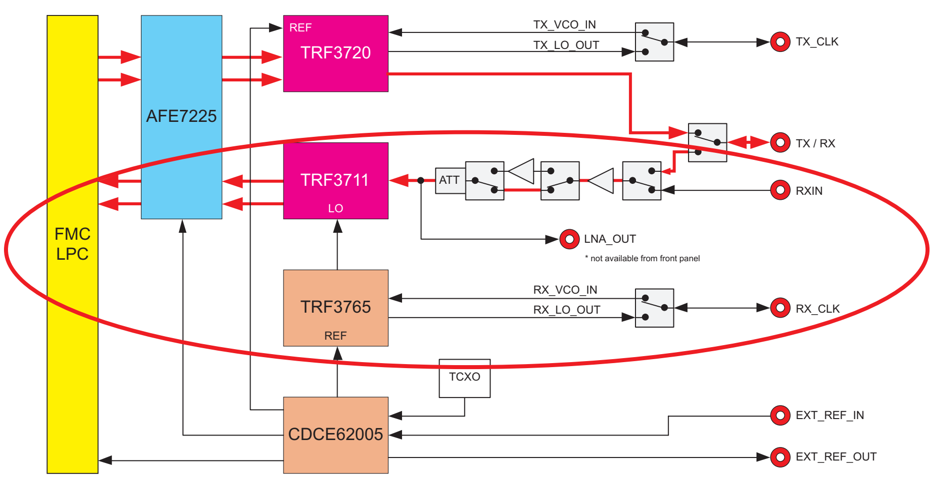

Figure 37. FMC30RF Block Diagram

2.2.2 Setup Description

The following settings were used to test the IP3:

1. TR3765 is set to internal/external LO mode and swept with the following frequencies: 750, 1000, 1500, 2140, 2800, 3300, and 3800 MHz (for the external mode only, signal generator was used to sweep) both the tests were controlled with the MATLAB automation process
2. The attenuator before TRF3711 is set to minimum attenuation
3. Inside TRF3711, set the BB gain to 5 dB and disable the 3-dB attenuator
4. Two tone is generated via signal generators: the RF frequencies are: 756, 1006, 1506, 2146, 2806, 3306, and 3806 MHz for one and 754, 1004, 1504, 2144, 2804, 3304, and 3804 MHz for the other.

All 16 settings are checked from the previous test (IQ balance) and in most of the cases there are two main results; either the signal was saturated or the IM3 products were too low to discover.

Finally, the worst-case scenario for the IP3 number is tested. This case is shown in the following example:

The result is good and as expected.

The worst-case results follow:

- LO amplitude is set to 0 dBm and LO freq is 750–3800 MHz
- RF1 amplitude and RF2 amplitude in (the table) is represented in Pin [dBm]

The gain was calculated in lineup analysis and was tested using from V_{OUT} in dBFs to Vpp, Equation 2 is used:

$$V_{out} = 2 \times 10^{\frac{Vout\_dBFs}{20}} \tag{2}$$

From Vin in dBm to Vpp at 50-Ω load; P_0 = 1 mW, $V_{RMS} = \sqrt{\left(10^{\frac{V_{IN}}{10}}\right) \times R \times P_0}$:

$$Vin_{vpp} = 2\sqrt{2}V_{RMS} \tag{3}$$

The gain is simply via: $G = \frac{V_{out}}{V_{in}}$ and appears in the table under total gain.

In the end, IP3 = OIP3 – Gain was used and the results are in the following sections.

2.2.2.1 Example of Two-Tone Measurement

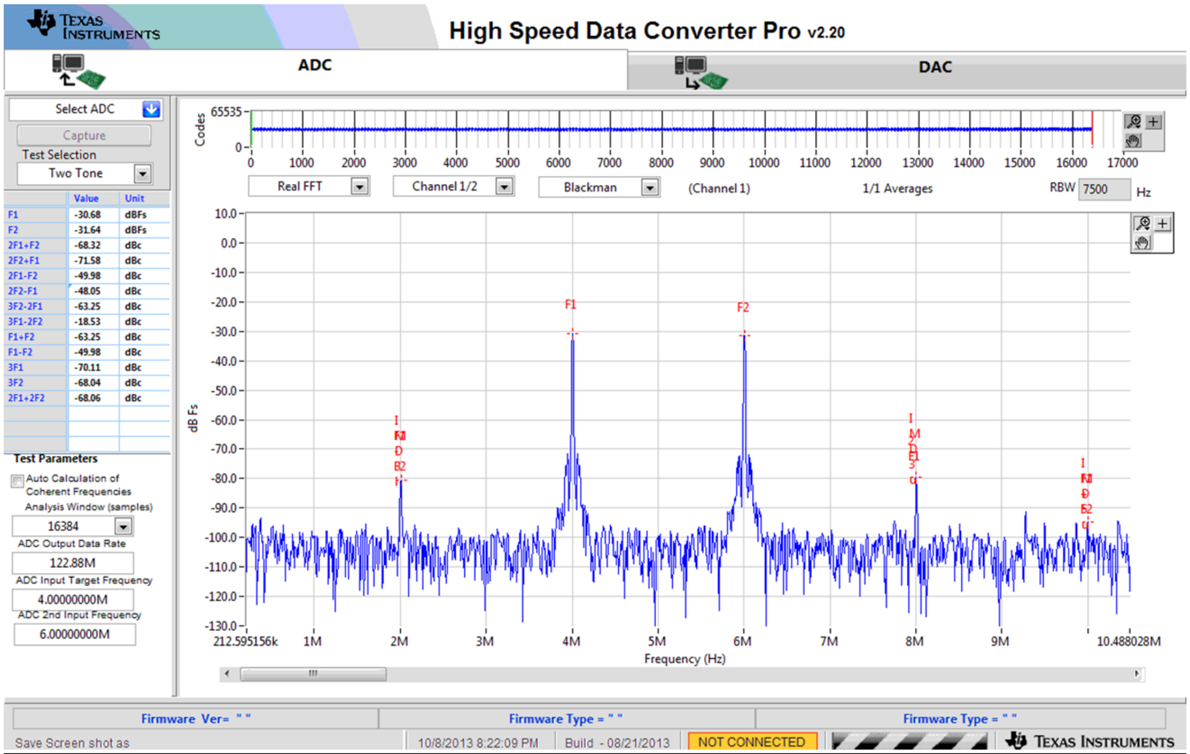

Figure 38. Two-Tone Measurement Example

2.2.3 Internal LO Test Result

Internal LO [MHz]	750	1000	1500	2140	2800	3300	3800
Pin [dBm]	–25	–29	–29	–26	–17	–13	–2
IP3_int_LO_Min_att_BBG_5_3dB_att_off	2.644721054	10.58715	8.149866	6.023239	1.2396	3.688738	0.683
Total gain	39.5047	39.8995	39.0572	44.83	39.186	39.13	39.0572

2.2.4 External LO Test Result

External LO [MHz]	750	1000	1500	2140	2800	3300	3800
Pin [dBm]	–24	–29	–29	–26	–17	–12	–2
IP3_ext_LO_Min_att_BBG_5_3dB_att_off	1.6782	9.3307	10.1426	7.7462	3.262	3.9872	1.009
Total gain	39.5047	39.8995	39.9572	44.8345	39.662	39.1131	39.0572

In most of the settings, the IM3 product stayed in the level of the noise; therefore, the result from the test is valid and expected.

2.3 Input Power Range Test Result

2.3.1 Test Description

A single tone is generated with two main settings in the system:

1. Maximum attenuation with 24-dB BB gain with 3-dB attenuation on.
2. Minimum attenuation with 24-dB BB gain with 3-dB attenuation off.

In order to simulate to two limits of the system without saturating the signal, the input power was changed until the signal was not saturated any more.

The system is tested for internal LO and external LO. Figure 39 shows a saturated signal plot.

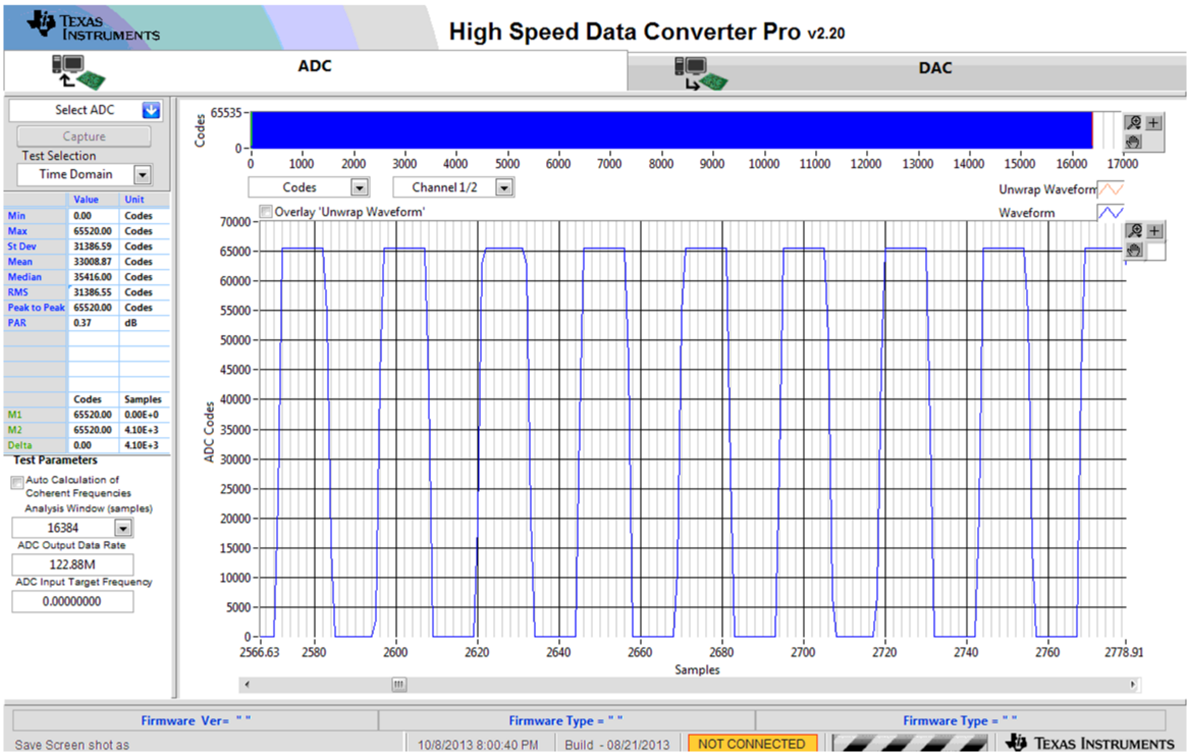

Figure 39. Saturated Signal

The signal is chopped in the edges due to saturating, in order to calculate the input power we backed off until we got a nonsaturated signal – in that point the values are posted in Section 2.3.2.

Figure 40 shows a good full scale signal after backing off.

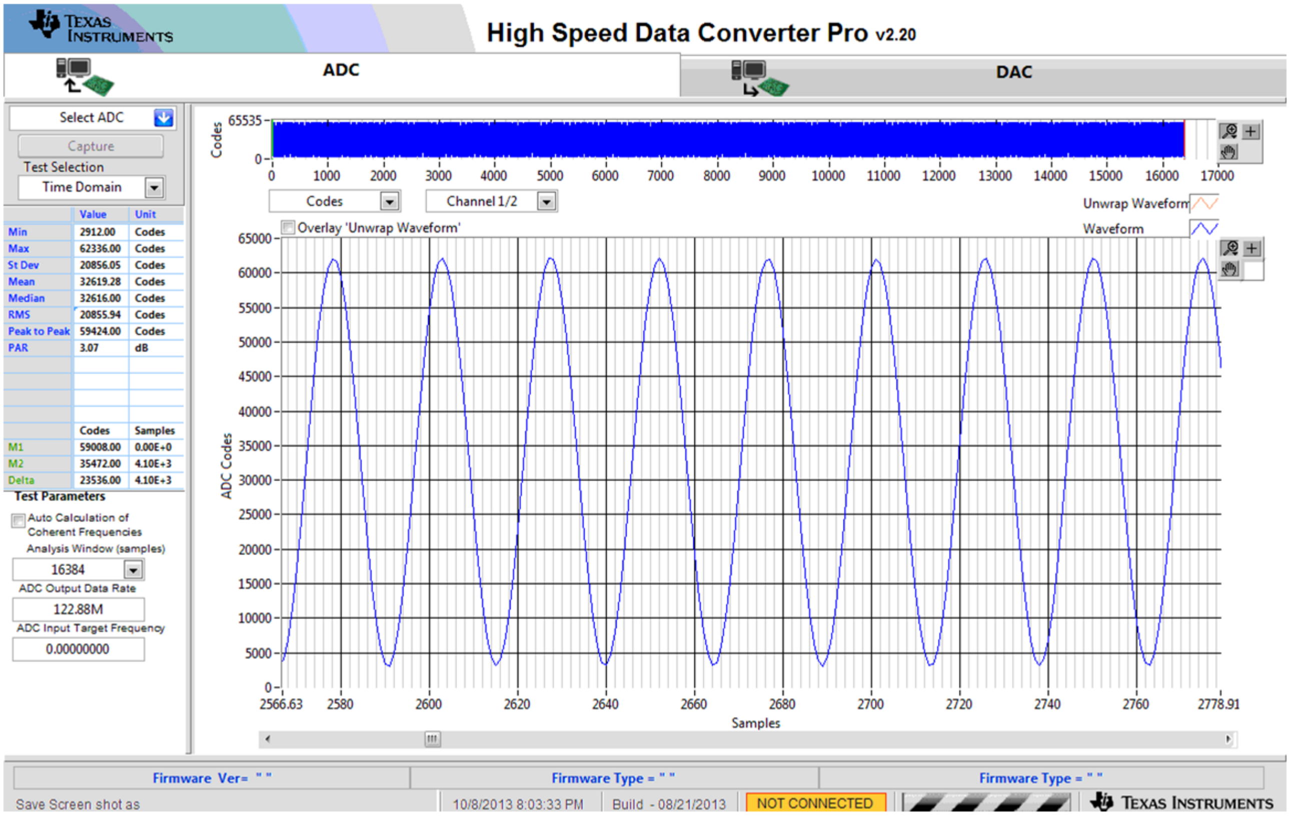

Figure 40. Backed-Off Signal

2.3.2 Internal LO

The contents in Table 4 are the result of backing off from the saturated signal to the first time we receive a nonsaturated signal – the values in the table are the input levels just below saturation at the gain setting shown. The green shading in Table 4 and Table 5 stands for maximum attenuation and the orange shading in those tables stands for minimum attenuation.

Table 4. Internal LO

Input Power Range: Internal LO							
Max Attenuation _ BB Gain 24, 3-db Attenuation on							
RF [MHz]	750	1000	1500	2140	2800	3300	3800
Pin [dBm]	–7	–10	–10	–8	0	7	10
after cable loss	–8.23	–11.18	–11.18	–10.27	–3.5	4.34	6.5
fundamental [dBFs]	–1.49	–0.47	–0.36	–0.88	–1.2114	–0.6	–4.999037
Input Power Range: Internal LO							
Min Attenuation _ BB Gain 24, 3-db Attenuation off							
RF [MHz]	750	1000	1500	2140	2800	3300	3800
Pin [dBm]	–39	–45	–42	–42	–18	–28	–19
after cable loss	–40.31	–46.15	–43.14	–43.14	–20.37	–31.63	–22.56
fundamental [dBFs]	–0.82	–1.01	–1.03	–1.1977	–1.41	–0.66	–1.142446

2.3.3 External LO

Table 5. External LO

Input Power Range: External LO							
Max Attenuation _ BB Gain 24, 3-db Attenuation off							
RF [MHz]	750	1000	1500	2140	2800	3300	3800
Pin [dBm]	–7	–11	–11	–8	0	7	10
after cable loss	–8.23	–12.25	–12.25	–10.27	–3.5	4.34	6.5
fundamental [dBFs]	–1.45367	–1.48	–1.28	–0.8	–1.19	–0.58	–5.01
Input Power Range: External LO							
Min Attenuation _ BB Gain 24, 3-db Attenuation off							
RF [MHz]	750	1000	1500	2140	2800	3300	3800
Pin [dBm]	–39	–45	–45	–42	–33	–28	–19
after cable loss	–40.31	–46.15	–46.15	–43.14	–34.15	–31.63	–22.56
fundamental [dBFs]	–0.75	–1	–1.1	–1.16	–0.92	–0.65	–1.23

2.4 SNR Test Result

2.4.1 Test Description

A single tone with two main settings in the system is generated:

1. Maximum attenuation with 24-dB BB gain with 3-dB attenuation on.
2. Minimum attenuation with 24-dB BB gain with 3-dB attenuation off.

The power was changed until the fundamental tone value, 0.5 dB, was around –1 dBFs (represented in C1 PWR); a 1-MHz band was used.

Equation 4 is used to calculate the NSD.

NSD dBFs/Hz = C2 PWR – LOG10(1 MHz) (4)

C2 PWR = the value in the “No spur" area.

The system was tested for internal LO and external LO.

Figure 41 shows an example plot.

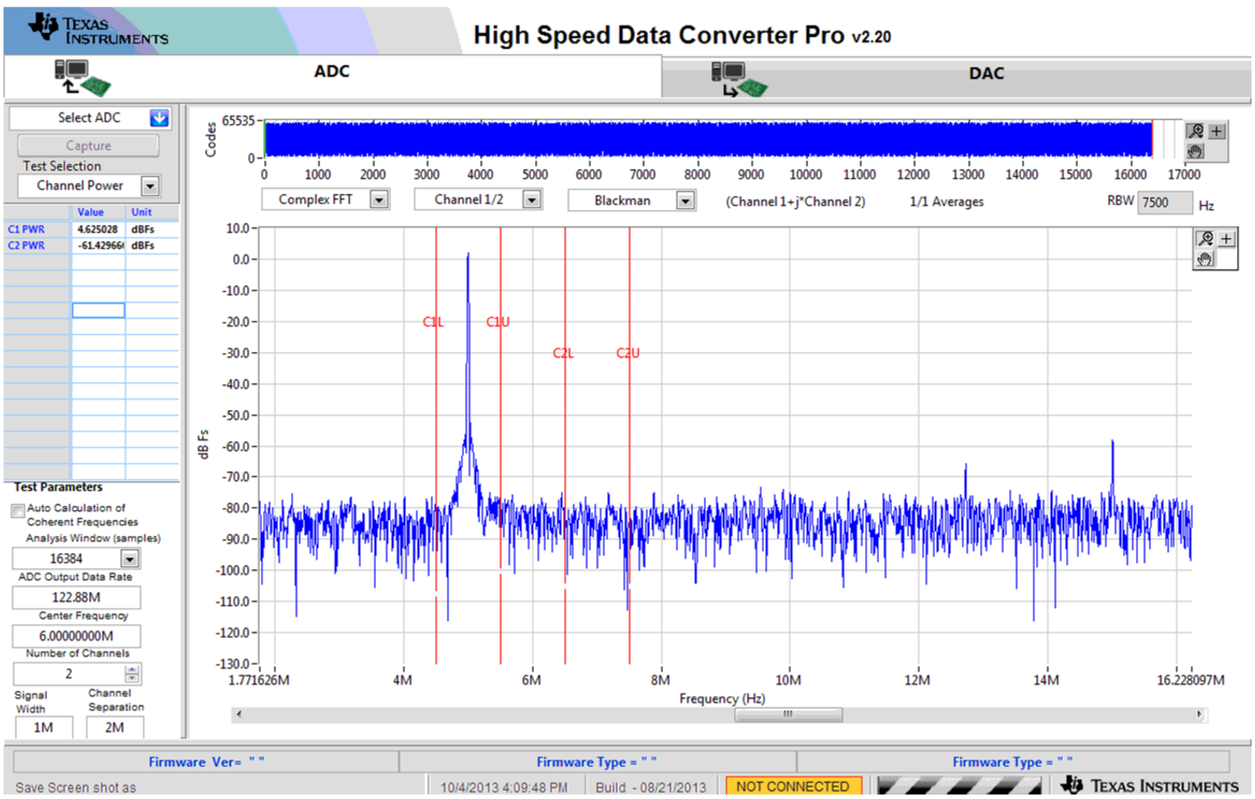

Figure 41. NSD Example

Figure 41 shows two red zones: C1 PWR – where the fundamental is inside and C2 PWR where there is no signal (no spur) inside. For the 1-MHz band, the NSD is calculated with Equation 5:

NSD dBFs/Hz = C2 PWR – LOG10(1 MHz) (5)

NOTE: The level of the noise density is while taking a band of 1 MHz, change the number in the log inside the formula if more noise density is needed.

2.4.2 Internal LO

The green shading in Table 6 and Table 7 stands for maximum attenuation and the orange shading in those tables stands for minimum attenuation.

In each table the NSD value is measured and calculated.

Table 6. Internal LO

SNR: Internal LO							
Max Attenuation _ BB Gain 24, 3-db Attenuation off							
RF [MHz]	750	1000	1500	2140	2800	3300	3800
RF [MHz]	750	1000	1500	2140	2800	3300	3800
C1 PWR	–1.471	–0.461	–0.349	–0.8716	–1.2114	0.584	4.999037
C2 PWR	–67.22	–67.07	–70.37	–69.099	–70.804	–68.18	–69.178186
NSD dBFS/Hz	–127.2	–127.1	–130.4	–129.1	–130.8	–128.2	–129.17819
SNR: Internal LO							
Min Attenuation _ BB Gain 24, 3-db Attenuation off							
RF [MHz]	750	1000	1500	2140	2800	3300	3800
C1 PWR	–0.802	–0.994	–1.035	–1.1977	–1.3965	–0.636	–1.142446
C2 PWR	–60.13	–58.71	–64.77	–62.632	–67.353	–66.73	–65.990161
NSD dBFS/Hz	–120.1	–118.7	–124.8	–122.63	–127.35	–126.7	–125.99016

2.4.3 External LO

Table 7. External LO

SNR: External LO							
Max Attenuation _ BB Gain 24, 3-db Attenuation off							
RF [MHz]	750	1000	1500	2140	2800	3300	3800
C1 PWR	–1.45367	–1.37325	–1.2627	–0.7964	–1.17108	0.56018	–4.996
C2 PWR	–63.09	–63.068	–68.884	–69.3846	–70.0083	–71.4108	–69.809
NSD dBFS/Hz	–123.09	–123.068	–128.88	–129.385	–130.008	–131.411	–129.81
SNR: External LO							
Min Attenuation _ BB Gain 24, 3-db Attenuation off							
RF [MHz]	750	1000	1500	2140	2800	3300	3800
C1 PWR	–0.72814	–0.97214	–1.0761	–1.14242	–0.90654	–0.63352	–1.2183
C2 PWR	–58.4705	–59.3046	–61.792	–64.327	–66.0771	–68.2949	–67.005
NSD dBFS/Hz	–118.471	–119.305	–121.79	–124.327	–126.177	–128.295	–127.01

The results stand for 1-MHz bandwidth and are correlated with the theory, the results are also constant around 118–130 [dBFs/Hz]; therefore, the results are valid.

2.5 Summary

This report covered the FMC30RF board performance tests for RX path and TX path. The following tests were also discussed: IQ-Balance, IP3, ACPR, input power range, and SNR. There is an expected performance **degradation** in the low frequencies (below 1 GHz) due to the bandwidth of the LNA which is not design to work below 1 GHz. The results meet expectations and are aligned with the lineup analysis.

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