Application Report
SLOA163–September 2011

OPA836 Low-Power Op Amp Applications

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High Speed Amplifiers

ABSTRACT

The following circuits show application information for the OPA836 and OPA2836. For simplicity, power supply decoupling capacitors are not shown in these diagrams.

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1 Non-Inverting Amplifier

The OPA836 and OPA2836 can be used as non-inverting amplifiers with signal input to the non-inverting input, V_{IN+}. A basic block diagram of the circuit is shown in Figure 1.

If we set $V_{IN} = V_{REF} + V_{SIG}$, then

$$V_{OUT} = V_{SIG}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \quad (1)$$

The signal gain of the circuit is set by: $G = 1 + \frac{R_F}{R_G}$, and V_{REF} provides a reference around which the input and output signals swing. Output signals are in-phase with the input signals.

The OPA836 and OPA2836 are designed for the nominal value of R_F to be 1kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. R_F = 1kΩ should be used as a default unless other design goals require changing to other values All test circuits used to collect data for this data sheet had R_F = 1kΩ for all gains other than +1. Gain of +1 is a special case where R_F is shorted and R_G is left open.

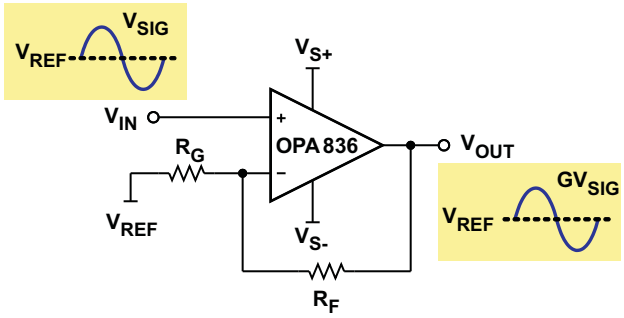

Figure 1. Non-Inverting Amplifier

2 Inverting Amplifier

The OPA836 and OPA2836 can be used as inverting amplifiers with signal input to the inverting input, V_{IN-}, through the gain setting resistor R_G. A basic block diagram of the circuit is shown in Figure 2.

If we set $V_{IN} = V_{REF} + V_{SIG}$, then

$$V_{OUT} = V_{SIG}\left(\frac{-R_F}{R_G}\right) + V_{REF} \quad (2)$$

The signal gain of the circuit is set by: $G = \frac{-R_F}{R_G}$ and V_{REF} provides a reference point around which the input and output signals swing. Output signals are 180° out-of-phase with the input signals. The nominal value of R_F should be 1kΩ for inverting gains.

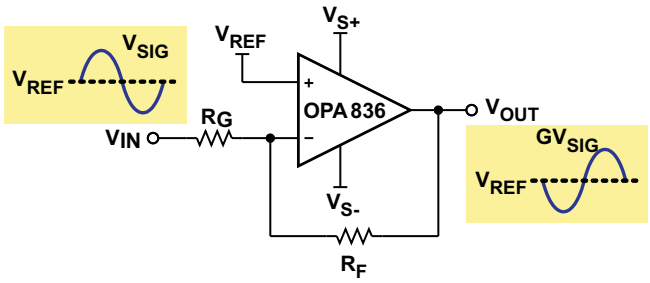

Figure 2. Inverting Amplifier

3 Attenuators

The non-inverting circuit of Figure 1 has minimum gain of 1. To implement attenuation, a resistor divider can be placed in series with the positive input, and the amplifier set for gain of 1 by shorting V_{OUT} to V_{IN-} and removing R_G. Since the op amp input is high impedance, the attenuation is set by the resistor divider.

The inverting circuit of Figure 2 can be used as an attenuator by making R_G larger than R_F. The attenuation is simply the resistor ratio. For example a 10:1 attenuator can be implemented with R_F = 1 kΩ and R_G = 10 kΩ.

4 Single Ended to Differential Amplifier

Figure 3 shows an amplifier circuit that is used to convert single-ended signals to differential, and provides gain and level shifting. This circuit can be used for converting signals to differential in applications like line drivers for CAT 5 cabling or driving differential input SAR and ΔΣ ADCs.

By setting $V_{IN} = V_{REF} + V_{SIG}$, then

$$V_{OUT+} = G \times V_{IN} + V_{REF} \quad \text{and } V_{OUT-} = -G \times V_{IN} + V_{REF} \quad \text{Where: } G = 1 + \frac{R_F}{R_G} \tag{3}$$

The differential signal gain of the circuit is 2x G, and V_{REF} provides a reference around which the output signal swings. The differential output signal is in-phase with the single ended input signal.

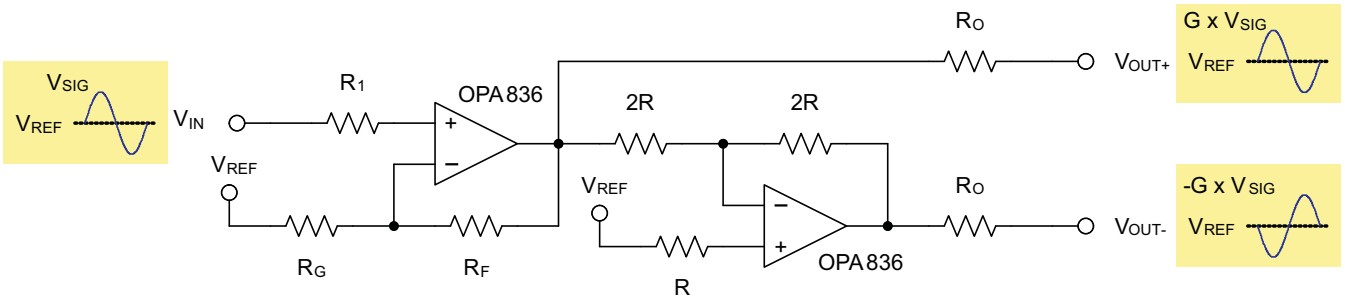

Figure 3. Single Ended to Differential Amplifier

Line termination on the output can be accomplished with resistors R_O. The impedance seen differential from the line will be 2x R_O. For example if 100 Ω CAT 5 cable is used with double termination, the amplifier is typically set for a differential gain of 2 V/V (6 dB) with R_F = 0 Ω (short) R_G = ∞Ω (open), 2R = 1 kΩ, R1 = 0 Ω, R = 499 Ω to balance the input bias currents, and R_O = 49.9 Ω for output line termination. This configuration is shown in Figure 4.

For driving a differential input ADC the situation is similar, but the output resistors, R_O, are typically chosen along with a capacitor across the ADC input for optimum filtering and settling time performance.

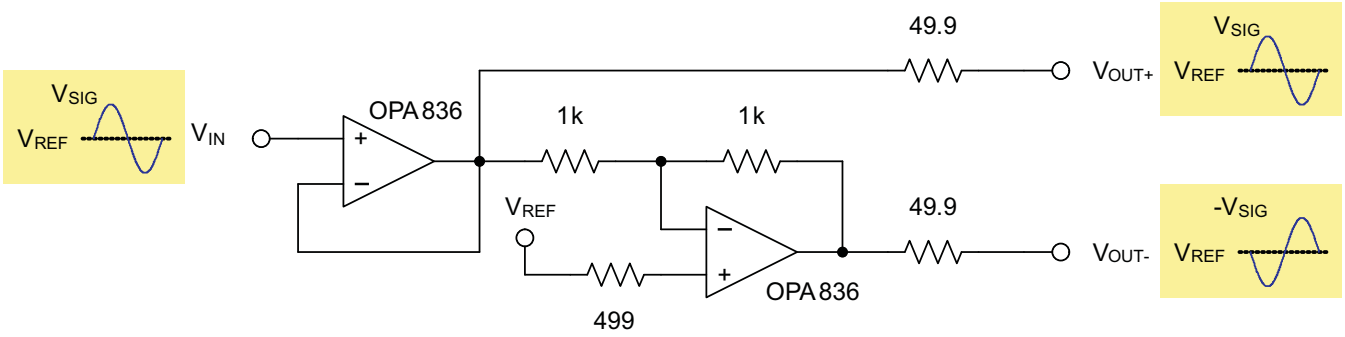

Figure 4. CAT 5 Line Driver with Gain = 2 V/V (6 dB)

5 Differential to Signal Ended Amplifier

Figure 5 shows a differential amplifier that is used to convert differential signals to single-ended and provides gain (or attenuation) and level shifting. This circuit can be used in applications like a line receiver for converting a differential signal from a CAT 5 cable to single-ended.

If we set $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then

$$V_{OUT} = \left(V_{IN+} - V_{IN-}\right) \times \left(\frac{R_F}{R_G}\right) + V_{REF} \quad (4)$$

The signal gain of the circuit is set by: $G = \frac{R_F}{R_G}$, V_{CM} is rejected, and V_{REF} provides a level shift around which the output signal swings. The single ended output signal is in-phase with the differential input signal.

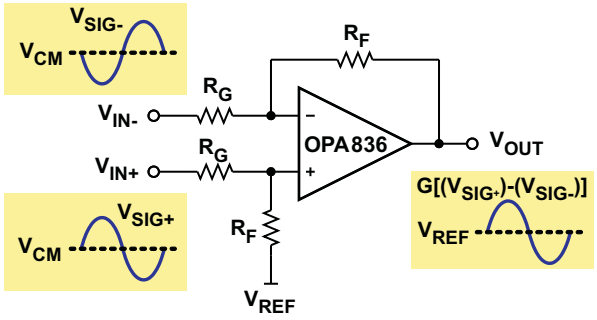

Figure 5. Differential to Single Ended Amplifier

Line termination can be accomplished with a resistor shunt across the input. The impedance seen differential from the line will be the resistor value in parallel with the amplifier circuit. For low gain and low line impedance the resistor value to add is approximately the impedance of the line. For example if 100 Ω CAT5 cable is used with a gain of 1 amplifier and $R_F = R_G = 1$ kΩ, adding a 100 Ω shunt across the input will give a differential impedance of 98 Ω; this should be adequate for most applications.

For best CMRR performance, resistors must be matched. A rule of thumb is CMRR ≈ the resistor tolerance; so 0.1% tolerance will provide about 60 dB CMRR.

6 Differential to Differential Amplifier

Figure 6 shows a differential amplifier that is used to amplify differential signals. This circuit has high input impedance and is often used in differential line driver applications where the signal source is a high impedance driver like a differential DAC that needs to drive a line.

If we set $V_{IN\pm} = V_{CM} + V_{SIG\pm}$ then

$$V_{OUT\pm} = V_{IN\pm} \times \left(1 + \frac{2R_F}{R_G}\right) + V_{CM} \quad (5)$$

The signal gain of the circuit is set by: $G = 1 + \frac{2R_F}{R_G}$, and V_{CM} passes with unity gain. The amplifier in essence combines two non-inverting amplifiers into one differential amplifier with the R_G resistor shared, which makes R_G effectively ½ its value when calculating the gain. The output signals are in-phase with the input signals.

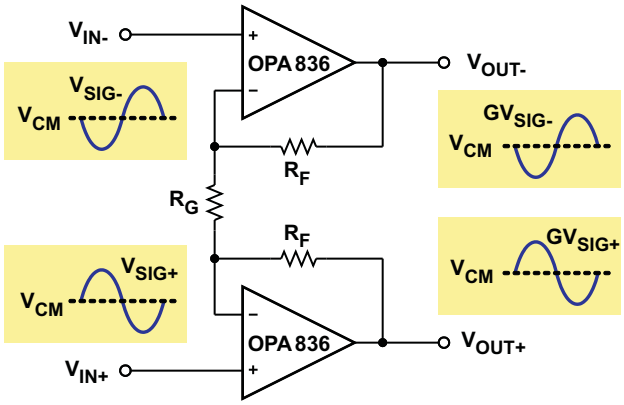

Figure 6. Differential to Differential Amplifier

7 Instrumentation Amplifier

Figure 7 is an instrumentation amplifier that combines the high input impedance of the differential to differential amplifier circuit and the common-mode rejection of the differential to single-ended amplifier circuit. This circuit is often used in applications where high input impedance is required like taps from a differential line or in cases where the signal source is a high impedance.

If we set $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then

$$V_{OUT} = \left(V_{IN+} - V_{IN-}\right) \times \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right) + V_{REF} \quad (6)$$

The signal gain of the circuit is set by:

$G = \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right)$, V_{CM} is rejected, and V_{REF} provides a level shift around which the output signal swings. The single ended output signal is in-phase with the differential input signal.

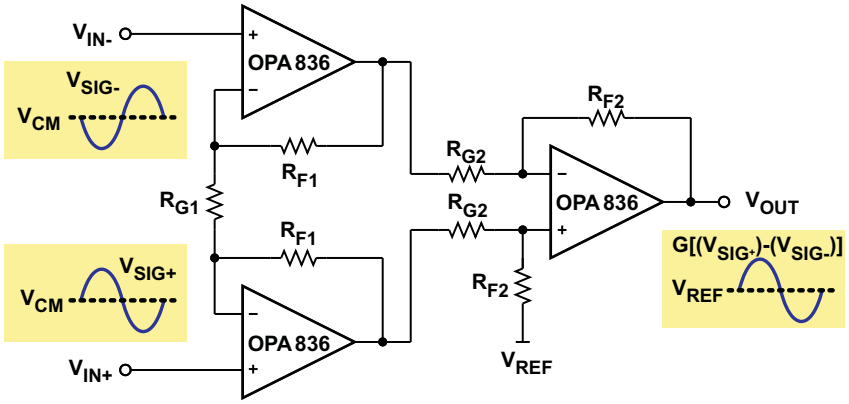

Figure 7. Instrumentation Amplifier

Integrated solutions are available, but the OPA836 provides a much lower power high frequency solution. For best CMRR performance, resistors must be matched. Assuming CMRR ≈ the resistor tolerance; so 0.1% tolerance will provide about 60 dB CMRR.

8 Gain Setting with OPA836 RUN Integrated Resistors

The OPA836 RUN package option includes integrated gain setting resistors for smallest possible footprint on a printed circuit board (≈ 2mm x 2mm). By adding circuit traces on the PCB, gains of +1, -1, -1.33, +2, +2.33, -3, +4, -4, +5, -5.33, +6.33, -7, +8 and inverting attenuations of -0.1429, -0.1875, -0.25, -0.33, -0.75 can be achieved.

Figure 8 shows a simplified view of how the OPA836IRUN integrated gain setting network is implemented. Table 1 shows the required pin connections for various non-inverting and inverting gains (reference Figure 1 and Figure 2). Table 2 shows the required pin connections for various attenuations using the inverting amplifier architecture (reference Figure 2). Due to ESD protection devices being used on all pins, the absolute maximum and minimum input voltage range, V_{S-} - 0.7V to V_{S+} + 0.7V, applies to the gain setting resistors, and so attenuation of large input voltages will require external resistors to implement.

The gain setting resistors are laser trimmed to 1% tolerance with nominal values of 1.6 kΩ, 1.2 kΩ, and 400 Ω. They have excellent temperature coefficient and gain tracking is superior to using external gain setting resistors. The 500 Ω and 1.5 pF capacitor in parallel with the 1.6 kΩ gain setting resistor provide compensation for best stability and pulse response.

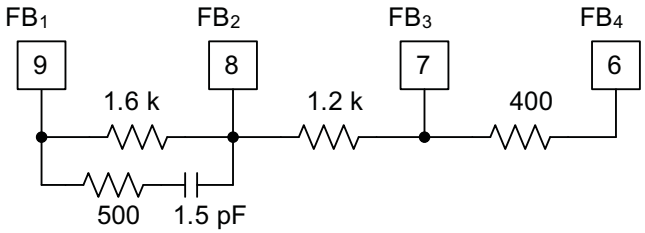

Figure 8. OPA836IRUN Gain Setting Network

Table 1. Gains Setting

Non-inverting Gain (Figure 1)	Inverting Gain (Figure 2)	Short Pins	Short Pins	Short Pins	Short Pins
1 V/V (0 dB)	-	1 to 9			-
2 V/V (6.02 dB)	-1 V/V (0 dB)	1 to 9	2 to 8	6 to GND	-
2.33 V/V (7.36 dB)	-1.33 V/V (2.5 dB)	1 to 9	2 to 8	7 to GND	-
4 V/V (12.04 dB)	-3 V/V (9.54 dB)	1 to 8	2 to 7	6 to GND	-
5 V/V (13.98 dB)	-4 V/V (12.04 dB)	1 to 9	2 to 7 or 8	7 to 8	6 to GND
6.33 V/V (16.03 dB)	-5.33 V/V (14.54 dB)	1 to 9	2 to 6 or 8	6 to 8	7 to GND
8 V/V (18.06 dB)	-7 V/V (16.90 dB)	1 to 9	2 to 7	6 to GND	-

Table 2. Attenuator Settings

Inverting Gain (Figure 2)	Short Pins	Short Pins	Short Pins	Short Pins
-0.75 V/V (-2.5 dB)	1 to 7	2 to 8	9 to GND	-
-0.333 V/V (-9.54 dB)	1 to 6	2 to 7	8 to GND	-
-0.25 V/V (-12.04 dB)	1 to 6	2 to 7 or 8	7 to 8	9 to GND
-0.1875 V/V (-14.54 dB)	1 to 7	2 to 6 or 8	6 to 8	9 to GND
-0.1429 V/V (-16.90 dB)	1 to 6	2 to 7	9 to GND	-

9 Input Common-Mode Voltage Range

When the primary design goal is a linear amplifier, with high CMRR, it is important to not violate the input common-mode voltage range (V_{ICR}) of an op amp.

Common-mode input range low and high specifications in the table data use CMRR to set the limit. The limits are chosen to ensure CMRR will not degrade more than 3dB below its limit if the input voltage is kept within the specified range. The limits cover all process variations and most parts will be better than specified. The typical specifications are from 0.2 V below the negative rail to 1.1 V below the positive rail.

Assuming the op amp is in linear operation the voltage difference between the input pins is small (ideally 0 V) and input common-mode voltage can be analyzed at either input pin and the other input pin is assumed to be at the same potential. The voltage at V_{IN+} is easy to evaluate. In non-inverting configuration, Figure 1, the input signal, V_{IN}, must not violate the V_{ICR}. In inverting configuration, Figure 2, the reference voltage, V_{REF}, needs to be within the V_{ICR}.

The input voltage limits have fixed headroom to the power rails and track the power supply voltages. For with single 5 V supply, the linear input voltage range is –0.2 V to 3.9 V and with 2.7 V supply it is –0.2 V to 1.6V . The delta from each power supply rail is the same in either case; –0.2 V and 1.1 V.

10 Output Voltage Range

The OPA836 and OPA2836 are rail-to-rail output (RRO) op amps. Rail-to-rail output typically means the output voltage can swing to within a couple hundred milli-volts of the supply rails. There are different ways to specify this; one is with the output still in linear operation and another is with the output saturated. Saturated output voltages are closer to the power supply rails than linear outputs, but the signal is not a linear representation of the input. Linear output is a better representation of how well a device performs when used as a linear amplifier. Both saturation and linear operation limits are affected by the current in the output, where higher currents lead to more loss in the output transistors.

Data in the (SLOS713 data sheet) ELECTRICAL SPECIFICATIONS tables list both linear and saturated output voltage specifications with 1 kΩ load. Figure 9 and Figure 10 show saturated voltage swing limits versus output load resistance and Figure 11 and Figure 12 show the output saturation voltage versus load current. Given a light load, the output voltage limits have nearly constant headroom to the power rails and track the power supply voltages. For example with 2 kΩ load and single 5 V supply the linear output voltage range is 0.15 V to 4.8 V and with 2.7 V supply it is 0.15 V to 2.5V. The delta from each power supply rail is the same in either case; 0.15 V and 0.2 V.

With devices like the OPA836 and OPA2836, where the input range is lower than the output range, it is typical that the input will limit the available signal swing only in non-inverting gain of 1. Signal swing in non-inverting configurations in gains > +1 and inverting configurations in any gain is generally limited by the output voltage limits of the op amp.

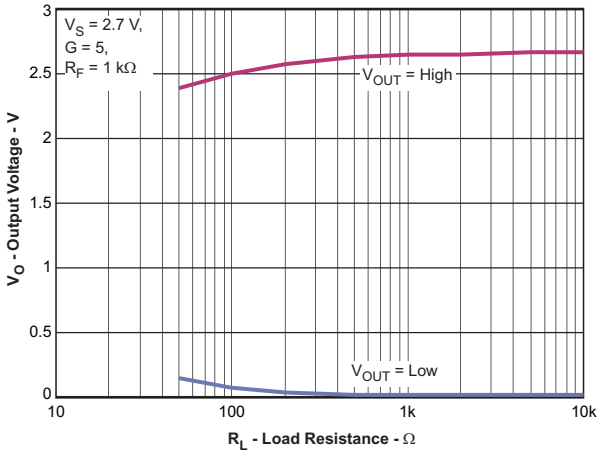

Figure 9. Output Voltage Swing vs Load Resistance

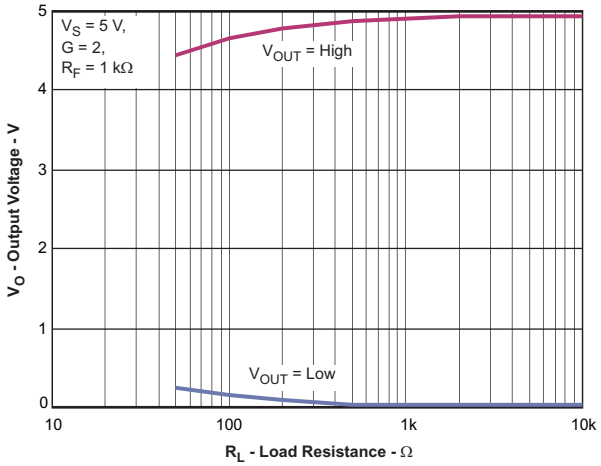

Figure 10. Output Voltage Swing vs Load Resistance

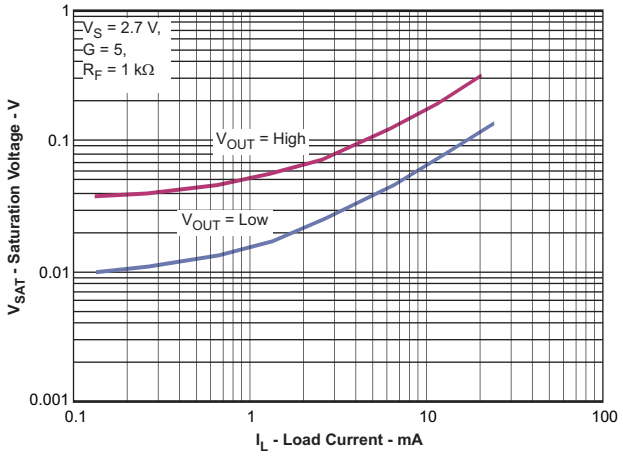

Figure 11. Output Saturation Voltage vs Load Current

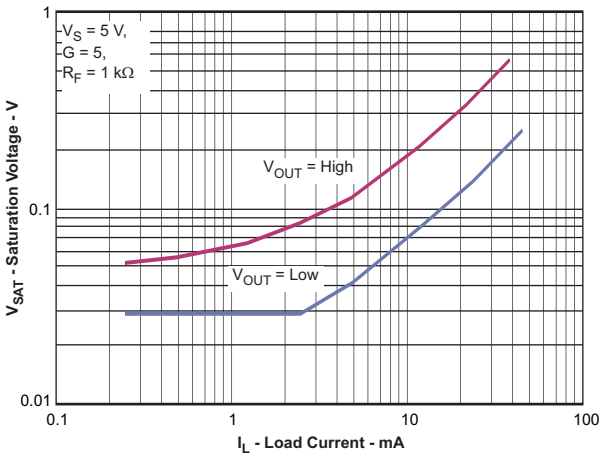

Figure 12. Output Saturation Voltage vs Load Current

11 Split-Supply Operation (±1.25V to ±2.75V)

To facilitate testing with common lab equipment, the OPA836 EVM SLOU314 is built to allow for split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers and other lab equipment reference their inputs and outputs to ground.

Figure 13 shows a simple non-inverting configuration analogous to Figure 1 with ±2.5 V supply and V_{REF} equal to ground. The input and output will swing symmetrically around ground. Due to its ease of use, split supply operation is preferred in systems where signals swing around ground, but it requires generation of two supply rails.

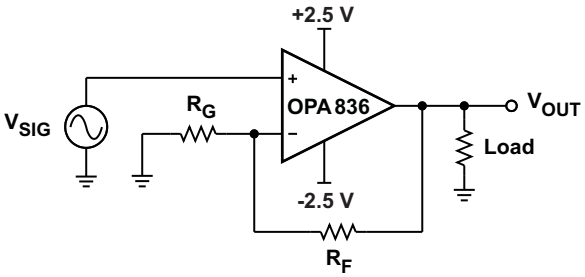

Figure 13. Split Supply Operation

12 Single-Supply Operation (2.5 V to 5.5 V)

Many newer systems use single power supply to improve efficiency and reduce the cost of the power supply. OPA836 and OPA2836 are designed for use with single-supply power operation and can be used with single-supply power with no change in performance from split supply as long as the input and output are biased within the linear operation of the device.

To change the circuit from split supply to single supply, level shift of all voltages by ½ the difference between the power supply rails. For example, changing from ±2.5 V split supply to 5 V single supply is shown conceptually in Figure 14.

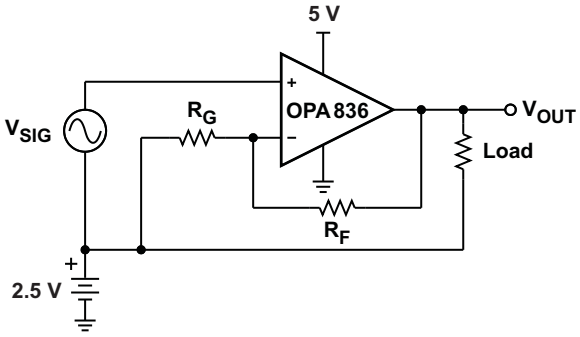

Figure 14. Single Supply Concept

A more practical circuit will have an amplifier or other circuit before to provide the bias voltage for the input and the output provides the bias for the next stage.

Figure 15 shows a typical non-inverting amplifier situation. With 5V single supply, a mid supply reference generator is needed to bias the negative side via R_G. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 is chosen to be equal to R_F in parallel with R_G. For example if gain of 2 is required and R_F = 1 kΩ, select R_G = 1 kΩ to set the gain and R_1 = 499 Ω for bias current cancellation. The value for C is dependent on the reference, but at least 0.1 µF is recommended to limit noise.

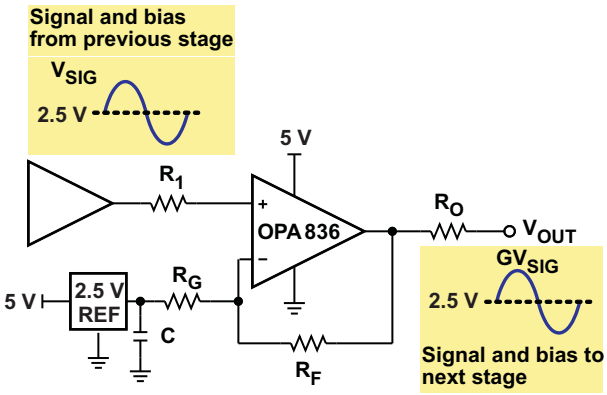

Figure 15. Non-Inverting Single Supply with Reference

Figure 16 shows a similar non-inverting single supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_G' and R_G" form a resistor divider from the 5 V supply and are used to bias the negative side with their parallel sum equal to the equivalent R_G to set the gain. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 in is chosen to be equal to R_F in parallel with R_G' in parallel with R_G" (R_1= R_F||R_G'||R_G"). For example if gain of 2 is required and R_F = 1 kΩ, selecting R_G' = R_G" = 2 kΩ gives equivalent parallel sum of 1 kΩ, sets the gain to 2, and references the input to mid supply (2.5 V). R_1 is then set to 499 Ω for bias current cancellation. This can be lower cost, but note the extra current draw required in the resistor divider.

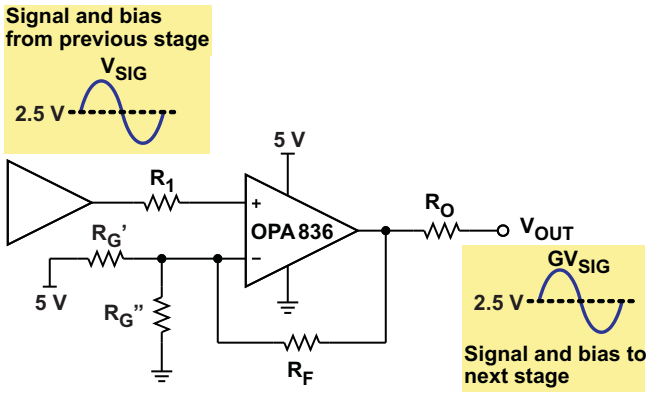

Figure 16. Non-Inverting Single Supply with Resistors

Figure 17 shows a typical inverting amplifier situation. With 5V single supply, a mid supply reference generator is needed to bias the positive side via R_1. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 is chosen to be equal to R_F in parallel with R_G. For example if gain of -2 is required and R_F = 1 kΩ, select R_G = 499 Ω to set the gain and R_1 = 332 Ω for bias current cancellation. The value for C is dependent on the reference, but at least 0.1 µF is recommended to limit noise into the op amp.

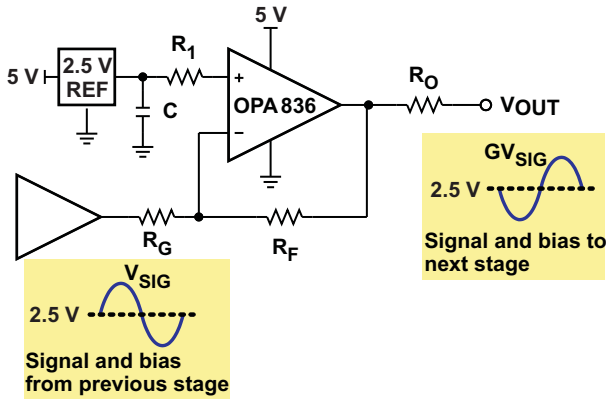

Figure 17. Inverting Single Supply with Reference

Figure 18 shows a similar inverting single supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_1 and R_2 form a resistor divider from the 5 V supply and are used to bias the positive side. To cancel the voltage offset that would otherwise be caused by the input bias currents, set the parallel sum of R_1 and R_2 equal to the parallel sum of R_F and R_G. C should be added to limit coupling of noise into the positive input. For example if gain of –2 is required and R_F = 1 kΩ, select R_G = 499 Ω to set the gain. $R_1 = R_2$ = 665 Ω for mid supply voltage bias and for op amp input bias current cancellation. A good value for C is 0.1 µF. This can be lower cost, but note the extra current draw required in the resistor divider.

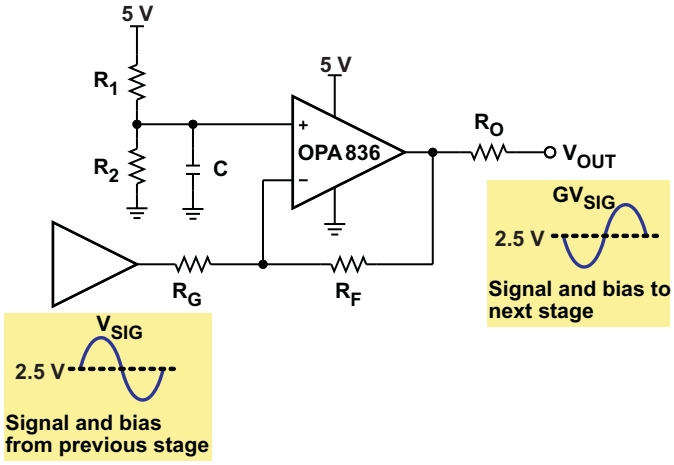

Figure 18. Inverting Single Supply with Resistors

13 Pulse Application with Single-Supply

For pulsed applications, where the signal is at ground and pulses to some positive or negative voltage, the circuit bias voltage considerations are different than with a signal that swings symmetrical about a reference point and the circuit configuration should be adjusted accordingly. Figure 19 shows a pulsed situation where the signal is at ground (0 V) and pulses to a positive value.

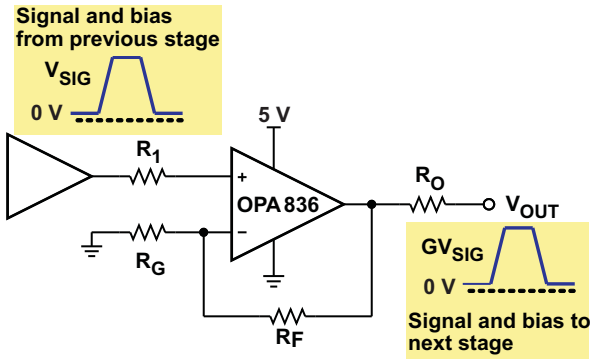

Figure 19. Non-Inverting Single Supply with Pulse

If the input signal pulses negative from ground, an inverting amplifier is more appropriate as shown in Figure 20. A key consideration in both non-inverting and inverting cases is that the input and output voltages are kept within the limits of the amplifier, and since the V_{ICR} of the OPA836 includes the negative supply rail, the op amp lends itself to this application.

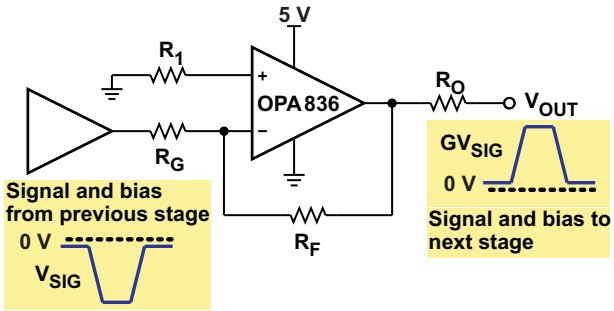

Figure 20. Inverting Single Supply with Pulse

14 Power-Down Operation

The OPA836 and OPA2836 include a power-down mode. Under logic control, the amplifiers can be switched from normal operation to a standby current of <1.5µA. When the $\overline{PD}$ pin is connected high, the amplifier is active. Connecting $\overline{PD}$ pin low disables the amplifier, and places the output in a high impedance state. Note: the op amp's output in gain of +1 is high impedance similar to a 3-state high impedance gate, but in other gains the feedback network is a parallel load.

The $\overline{PD}$ pin must be actively driven high or low and should not be left floating. If the power-down mode is not used, $\overline{PD}$ should be tied to the positive supply rail.

$\overline{PD}$ logic states are TTL with reference to the negative supply rail, V_{S-}. When the op amp is powered from single supply and ground, driving from logic devices with similar V_{DD} voltages to the op amp should not require any special consideration. When the op amp is powered from split supply, V_{S-} is below ground and an open collector type of interface with pull-up resistor is more appropriate. Pull-up resistor values should be lower than 100k and the drive logic should be negated due to the inverting action of an open collector gate.

15 Low Power Applications and the Effects of Resistor Values on Bandwidth

The OPA836 and OPA2836 are designed for the nominal value of R_F to be 1 kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. It also loads the amplifier. For example; in gain of 2 with $R_F = R_G = 1$ kΩ, R_G to ground, and $V_{OUT} = 4$ V, 2 mA of current will flow through the feedback path to ground. In gain of +1, R_G is open and no current will flow to ground. In low power applications, it is desirable to reduce this current by increasing the gain setting resistors values. Using larger value gain resistors has two primary side effects (other than lower power) due to their interaction with parasitic circuit capacitance.

1. Lowers the bandwidth.
2. Lowers the phase margin
   (a) This will cause peaking in the frequency response.
   (b) And will cause over shoot and ringing in the pulse response.

Figure 21 shows the small signal frequency response on OPA836EVM for non-inverting gain of 2 with R_F and R_G equal to 1 kΩ, 10 kΩ, and 100kΩ. The test was done with $R_L = 1$ kΩ. Due to loading effects of R_L, lower values may reduce the peaking, but higher values will not have a significant effect.

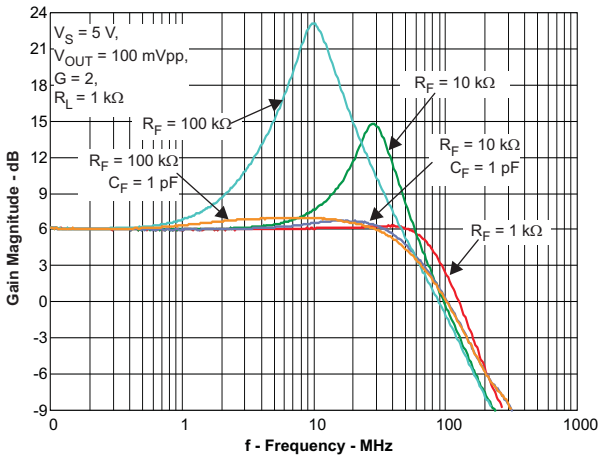

Figure 21. Frequency Response with Various Gain Setting Resistor Values

As expected, larger value gain resistors cause lower bandwidth and peaking in the response (peaking in frequency response is synonymous with overshoot and ringing in pulse response). Adding 1 pF capacitors in parallel with R_F helps compensate the phase margin and restores flat frequency response. Figure 22 shows the test circuit used.

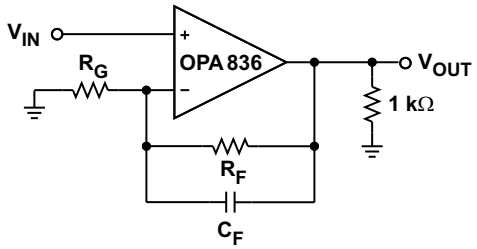

Figure 22. G = 2 Test Circuit for Various Gain Setting Resistor Values

16 Driving Capacitive Loads

The OPA836 and OPA2836 can drive up to a nominal capacitive load of 2.2 pF on the output with no special consideration. When driving capacitive loads greater than this, it is recommended to use a small resister (R_O) in series with the output as close to the device as possible. Without R_O, capacitance on the output will interact with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that will reduce the phase margin. This will cause peaking in the frequency response and overshoot and ringing in the pulses response. Interaction with other parasitic elements may lead to instability or oscillation. Inserting R_O will isolate the phase shift from the loop gain path and restore the phase margin; however, it will also limit the bandwidth.

Figure 23 shows the test circuit and Figure 25 shows the recommended values of R_O versus capacitive loads, C_L. See Figure 24 for frequency response with various values.

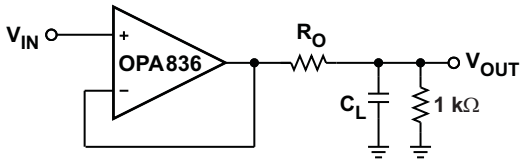

Figure 23. R_O versus C_L Test Circuit

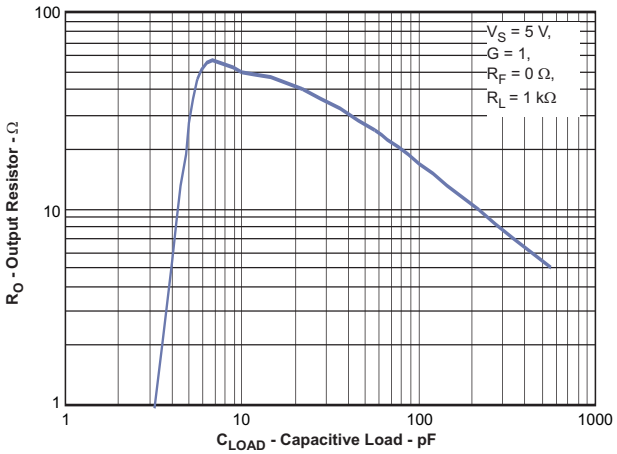

Figure 24. Series Output Resistor vs Capacitive Load

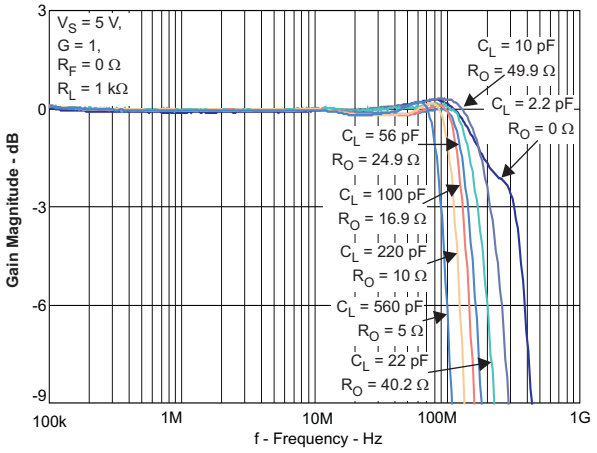

Figure 25. Frequency Response with Capacitive Load

17 Active Filters

The OPA836 and OPA2836 can be used to design active filters. Figure 27 and Figure 26 show MFB and Sallen-Key circuits designed using FilterPro™ http://focus.ti.com/docs/toolsw/folders/print/filterpro.html to implement 2nd order low-pass butterworth filter circuits. Figure 28 shows the frequency response.

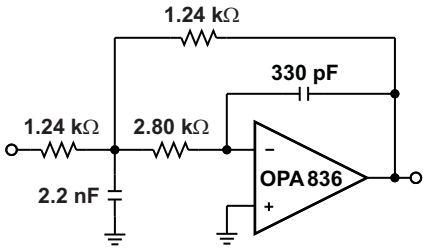

Figure 26. MFB 100kHz 2nd Order Low-Pass Butterworth Filter Circuit

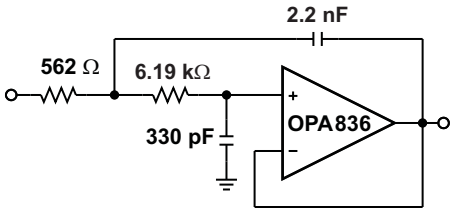

Figure 27. Sallen-Key 100kHz 2nd Order Low-Pass Butterworth Filter Circuit

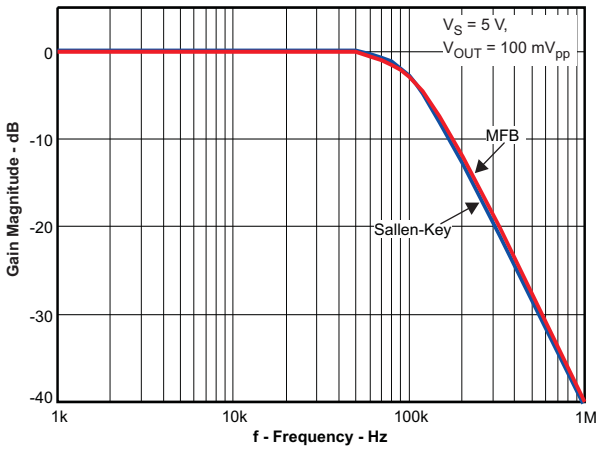

Figure 28. MFB and Sallen-Key 2_{nd} Order Low-Pass Butterworth Filter Response

MFB and Sallen-Key filter circuits offer similar performance. The main difference is the MFB is an inverting amplifier in the pass band and the Sallen-Key is non-inverting. The primary pro for each is the Sallen-Key in unity gain has no resistor gain error term, and thus no sensitivity to gain error, while the MFB has inherently better attenuation properties beyond the bandwidth of the op amp.

18 Audio Frequency Performance

The OPA836 and OPA2836 provide excellent audio performance with very low quiescent power. To show performance in the audio band, a 2700 series Audio Analyzer from Audio Precision was used to test THD+N and FFT at 1 V_{RMS} output voltage. Figure 29 is the test circuit used. Note the 100 pF capacitor to ground on the input helped to decouple noise pick up in the lab and improved noise performance.

Figure 30 shows the THD+N performance with 100 kΩ and 300Ω loads, with A-weighting, and with no weighting. Both loads show similar performance. With no weighting the THD+N performance is dominated by the noise whereas A-weighting provides filtering that improves the noise.

Figure 31 and Figure 32 show FFT output with a 1 kHz tone and 100 kΩ and 300 Ω loads. To show relative performance of the device versus the test set, one channel has the OPA836 in line between generator output and analyzer input and the other channel is in “Gen Mon” loopback mode, which internally connects the signal generator to the analyzer input. With 100 kΩ load, Figure 31, the curves are basically indistinguishable from each other except for noise, which means the OPA836 cannot be directly measured. With 300 Ω load, Figure 32, the main difference between the curves is OPA836 shows slightly higher even order harmonics, but odd order is masked by the test set performance.

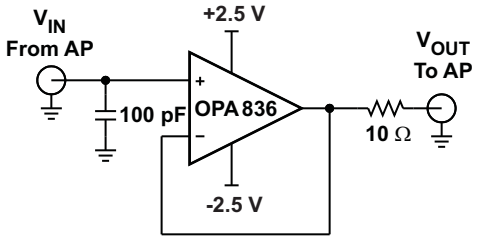

Figure 29. OPA836 AP Analyzer Test Circuit

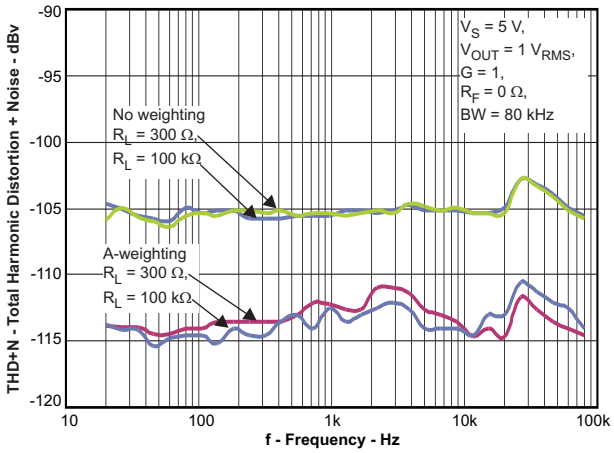

Figure 30. OPA836 1Vrms 20 Hz to 80 kHz THD+N

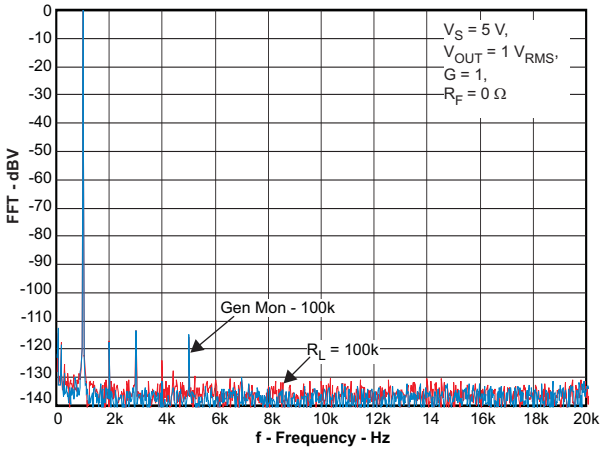

Figure 31. OPA836 and AP Gen Mon 10kHz FFT Plot; V_{OUT} = 1 V_{RMS}, R_L = 100 kΩ

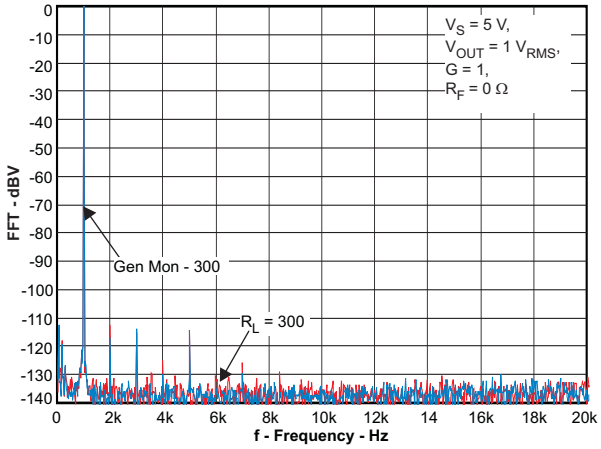

Figure 32. OPA836 and AP Gen Mon 10 kHz FFT Plot; V_{OUT} = 1 V_{RMS}, R_L = 300Ω

19 ADC Driver Performance

The OPA836 provides excellent performance when driving high performance delta-sigma (ΔΣ) and successive approximation register (SAR) ADCs in low power audio and industrial applications.

20 OPA836 and ADS8326 Combined Performance

To show achievable performance, the OPA836 is tested as the drive amplifier for the ADS8326. The ADS8326 is a 16-bit, micro power, SAR ADC with pseudo-differential inputs and sample rates up to 250 kSPS. It offers excellent noise and distortion performance in a small 8-pin SOIC or VSSOP (MSOP) package. Low power and small size make the ADS8326 and OPA836 an ideal solution for portable and battery-operated systems, for remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition.

The circuit shown in Figure 33 is used to test the performance, Figure 34 is the FFT plot with 10 kHz input frequency showing the spectral performance, and the tabulated AC analysis results are in Table 3.

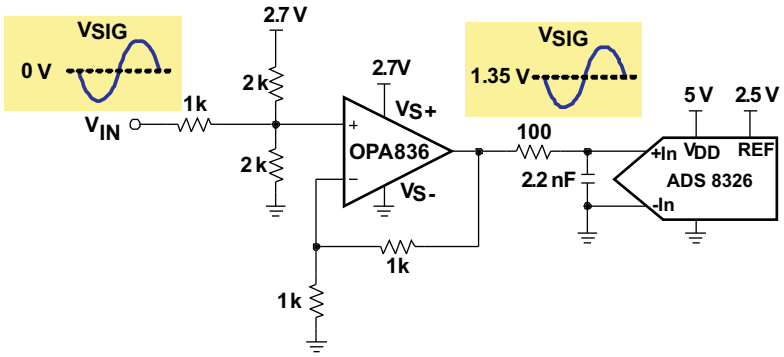

Figure 33. OPA836 and ADS8326 Test Circuit

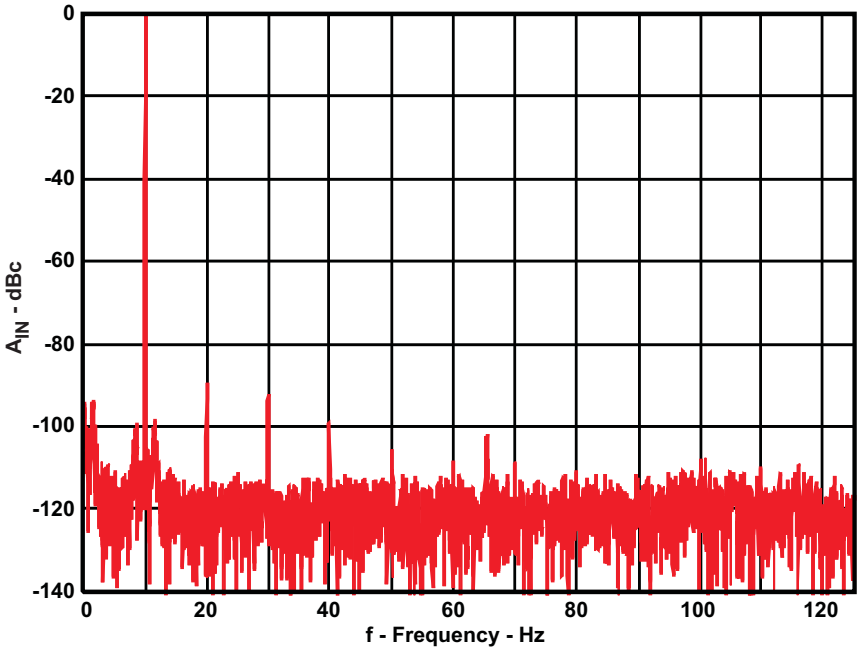

Figure 34. ADS8326 and OPA836 10kHz FFT

Table 3. AC Analysis

Tone (Hz)	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
10k	–0.85	83.3	–86.6	81.65	88.9

21 Layout Recommendations

The OPA836 EVM (SLOU314) should be used as a reference when designing the circuit board. It is recommended to follow the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into an out of the op amp.
2. The feedback path should be short and direct avoiding vias if possible especially with G = +1.
3. Ground or power planes should be removed from directly under the amplifier's negative input and output pins.
4. A series output resistor is recommended to be placed as near to the output pin as possible. See "Series Output Resistor vs. Capacitive Load" (Figure 24) for recommended values given expected capacitive load of design.
5. A 2.2 µF power supply decoupling capacitor should be placed within 2 inches of the device and can be shared with other op amps. For spit supply, a capacitor is required for both supplies.
6. A 0.1 µF power supply decoupling capacitor should be placed as near to the power supply pins as possible. Preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.
7. The $\overline{PD}$ pin uses TTL logic levels. If not used it should tied to the positive supply to enable the amplifier. If used, it must be actively driven. A bypass capacitor is not necessary, but can be used for robustness in noisy environments.

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