

## **TRF7960 and TRF7970A Comparison**

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*Josh Wyatt**Texas Instruments Embedded RF*

### **ABSTRACT**

This application report is intended to help users of the TRF7970A high-frequency RFID/NFC reader IC understand the differences between it and the TRF7960 IC. Understanding these differences in detail and applying this knowledge to application-specific requirements can assist in development efforts.

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## 1 Features Common to TRF7960 and TRF7970A

The features listed here are common to the TRF7960 and TRF7970A.

- Pin assignments
- Terminal functions and features
- Package: 32-pin QFN (RHB) ([MPQF130](#))
- Reference schematic and recommended layout
- ISO standard protocol support (ISO/IEC 14443A, ISO/IEC 14443B, ISO/IEC 15693)
- Basic non-ISO standard compliant protocol support (for example, MIFARE™ and FeliCa™)

## 2 Background

The TRF7960 has limitations with ISO14443A and ISO14443A-like protocols that require firmware workarounds. Resolving these limitations directly inside the TRF7960 is the primary reason for the introduction of the new device. New users or developers implementing the ISO14443A protocol might want to consider using the TRF7960A or TRF7970A first. Users who are already familiar with the workarounds and are in full production with the TRF7960 might consider migrating to the TRF7960A or TRF7970A only when it makes logical sense or to add full NFC capabilities. See [Table 1](#) for details on the device limitations with the TRF7960 when using ISO14443A protocol.

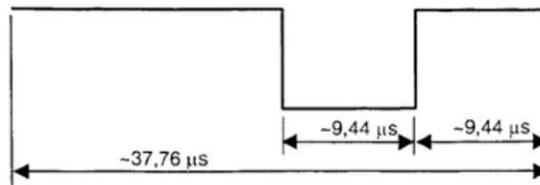
**Table 1. Device Limitations and Workarounds Using TRF7960 for ISO14443A Operations**

Item	Issue	Workaround	Comment
1	ISO14443A decoder gives wrong data using certain data rates (106 kbps, 424 kbps, and 848 kbps) and under certain hardware conditions	Switch to auxiliary receive channel and/or adjust gain.	When the analog filter overshoot is such that the digitizer produces a rising edge on the subcarrier data in a small time window the decoder will produce false data. This is rare condition and is also dependent on the output impedance matching/filter circuit. This condition is also dependant upon the resonant antenna characteristics.
2	ISO14443A anticollision not flexible	Firmware needs to accommodate different results from 6 or 7 subcarrier pulses in a given bit period	Anticollision is possible with ISO14443A, but detailed understanding of the ISO standard is required.
3	TRF7960 does not support 4 bits replay (ACK, NCK) used by some non-ISO standard ISO14443A-like protocols	Direct Mode 0	
4	TRF7960 does not allow frames in ISO14443A Layer 4 which would start with same Select (SEL) code as anticollision frames (first byte = 0x93, 0x95, or 0x97).		

### 3 Detailed Changes to the TRF7970A

To resolve device limitations shown in [Table 1](#), the following changes were implemented on the TRF7970A.

1. Improvements and fixes were made to the ISO14443A 106-kbps, 424-kbps, and 848-kbps decoders (item 1 in [Table 1](#)).
2. More flexibility was introduced to the ISO14443A collision detection mechanism. Bit 0 in register 0x10 allows the application to use one of two criteria to the process. Either 7 subcarrier pulses per bit period or 6 subcarrier pulses per period are now allowed. See [Table 2](#) for the bit definitions of the Special Function Register 0x10 (item 2 in [Table 1](#)).
3. TRF7970A can decode 4 bits replay with bit 2 = 1 in Special Functions Register (0x10) (item 3 in [Table 1](#)).
4. TRF7970A can handle frames in ISO14443A Layer 4 operations that start with same Select (SEL) code with bit 1 = 1 in Special Functions Register (0x10) (item 4 in [Table 1](#)).
5. TRF7970A also has an additional synchronization feature for ISO15693 EOF/Slot Marker commands. The timing of this command is on 37.77- $\mu$ s time interval, and this feature is enabled when bit 4 = 1 in Special Functions Register 0x10 (see [Figure 1](#) and [Table 2](#)).



**Figure 1. ISO15693 EOF/Slot Marker Sequence**

**Table 2. Special Functions Register 0x10 Bit Definitions**

Bit	Bit Name	Function	Description
B7	---	---	RFU
B6	---	---	RFU
B5	par43	Disables parity checking for ISO14443A	
B4	next_slot_37uSec	0 = 18.88 $\mu$ s 1 = 37.77 $\mu$ s	Sets time "grid" for EOF/Slot Marker for ISO15693
B3	Sp_dir_mode	Bit stream transmit for MIFARE (106 kbps)	Enables direct mode for transmitting ISO14443A data at 106 kbps, bypassing the FIFO and feeding the data bit stream directly onto the encoder.
B2	4_bit_RX	0 = Normal RX 1 = 4-bit RX	Enables 4 bit RX for MIFARE Ultra Light and my-d™ move (see file type2.c in TRF7960A reference firmware)
B1	14_anticoll	0 = Anticollision framing (0x93, 0x95 or 0x97) 1 = Normal Framing	Disable anticollision frames for ISO14443A (this bit should be set to 1 after completion of anti-collision sequence)
B0	col_7_6	0 = 7 subcarrier pulses 1 = 6 subcarrier pulses	Selects the number of subcarrier pulses that trigger a collision error in ISO14443A at 106 kbps

The TRF7970A also has improvements over the TRF7960A.

1. The TRF7970A also provides better communication with non-ISO standard ISO14443A cards (MIFARE cards). Bit 5 in register 0x10 disables the parity checking in ISO14443A protocol. Bit 3 in register 0x10 enables direct transmitting mode for MIFARE communications (see [Table 2](#)).
2. The TRF7970A provides additional information about the status of the receiver. Bit 0 in register 0x11 can indicate (with a logic 1) that the RX is in process when SOF is successfully decoded. This is intended to assist the detection of an ongoing RX operation without reading the IRQ Status Register 0x0C (see [Table 3](#)).

**Table 3. Special Functions Register 0x11 Bit Definitions**

Bit	Bit Name	Function	Description
B7		RFU	RFU
B6		RFU	RFU
B5		RFU	RFU
B4		RFU	RFU
B3		RFU	RFU
B2		RFU	RFU
B1		RFU	RFU
B0	irg_srx	Copy of the RX start signal (bit 6) from IRQ register (0x0C)	Signals the RX SOF was received and the RX is in progress. IRQ when RX is completed.

All of the changes in the TRF7970A can be enabled in Special Functions Registers 0x10 and 0x11 by setting appropriate bits to 1. To restore the default condition for the registers, set all bits to 0 and trigger a POR.

**Table 4. Pin Distribution in Special Direct Mode, TX Bit Stream**

Pin	Parallel	Parallel-Direct	Description
DATA_CLK	DATA_CLK	DATA_CLK	
I/O_7	A/D[7]		
I/O_6	A/D[6]		
I/O_5	A/D[5]	Bit clock out (for TX)	
I/O_4	A/D[4]		
I/O_3	A/D[3]	TX data input	
I/O_2	A/D[2]	TX enable (must be high for complete duration of the transmission)	
I/O_1	A/D[1]		
I/O_0	A/D[0]		
IRQ	IRQ (interrupt request)		

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