Application Report
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Comparison of TRF7960 and TRF7960A

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ABSTRACT

This application report helps current and new users of the TRF7960 high-frequency RFID/NFC reader understand the differences between the TRF7960 and the TRF7960A devices. Understanding these differences in detail and applying this knowledge to application-specific requirements helps designers make informed decisions about whether or not a bill of materials change is needed.

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1 Features Common to Both TRF7960 and TRF7960A

The following features are common to both the TRF7960 and the TRF7960A.

- Pin assignments
- Terminal functions and features
- Package is a 32-pin QFN (RHB) (S-PQFP-N32) (MPQF130)
- Reference schematic/recommended layout
- ISO standards protocol support (ISO14443A/B, ISO15693)
- Basic non-ISO standard compliant protocol support (MIFARE™, FeliCa, HF EPC, etc.)

2 Background

The TRF7960 has limitations with ISO14443A and ISO14443A-like protocols, and these limitations require firmware workarounds. Resolving these limitations directly inside the TRF7960A is the primary reason for the introduction of the new device. New users implementing the ISO14443A protocol may want to consider using the TRF7960A first. Users who are already familiar with the workarounds and are in full production with the TRF7960 may consider migrating to the TRF7960A only when it makes logical sense for them. See Table 1 for details on the device limitations with the TRF7960 when using ISO14443A protocol.

Table 1. Device Limitations and Workarounds Using TRF7960 for ISO14443A Operations

Item	Issue	Workaround	Comment
1	ISO14443A decoder gives wrong data using certain data rates (106 kbps, 424 kbps and 848 kbps) and under certain hardware conditions	Switch to auxiliary receive channel and/or adjust gain.	When the analog filter overshoot is such that the digitizer produces a rising edge on the subcarrier data in a small time window the decoder will produce false data. This is rare condition and is also dependent on the output impedance matching/filter circuit. This condition is also dependant upon the resonant antenna characteristics.
2	ISO14443A anti-collision not flexible	Firmware must accommodate different results from 6 or 7 subcarrier pulses in a given bit period	Anti-collision is possible with ISO14443A, but detailed knowledge/understanding of the ISO standard is required.
3	TRF7960 does not support 4 bits replay (ACK, NCK) used by some non-ISO standard ISO14443A-like protocols	Direct Mode 0	
4	TRF7960 does not allow frames in ISO14443A Layer 4 which would start with same Select (SEL) code as anti-collision frames.(first byte = 0x93h, 0x95h or 0x97h)		

3 Detailed Changes to the TRF7960A

To resolve device limitations shown in Table 1, the following changes were implemented on the TRF7960A.

- Improvements and fixes were made to the ISO14443A 106-kbps, 424-kbps, and 848-kbps decoders (see item 1 in Table 1).
- More flexibility was introduced to the ISO14443A collision detection mechanism. Bit 0 in register 0x10 allows the application of one of two criteria to the process. Either 7 subcarrier pulses per bit period or 6 subcarrier pulses per period are now allowed. See Table 2 for the bit definitions of the Special Function Register (see item 2 in Table 1).
- TRF7960A can decode 4 bits replay with bit 2 = 1 in the Special Functions register (see item 3 in Table 1).
- TRF7960A can process frames in ISO14443A Layer 4 operations that start with same Select (SEL) code with bit 1 = 1 in the Special Functions register (see item 4 in Table 1).
- TRF7960A has an additional synchronization feature for ISO15693 EOF and Slot Marker commands. The timing of this command is on a 37.77-µs time interval, and this feature is enabled when bit 4 = 1 in the Special Functions register (see Figure 1 and Table 2).

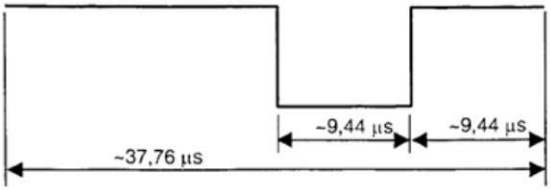

Figure 1. ISO15693 EOF/Slot Marker Sequence

Table 2. Special Functions Register (0x10h) Bit Definitions

Bit No.	Bit Name	Function	Description
B7	—	—	RFU
B6	—	—	RFU
B5	—	—	RFU
B4	next_slot_37uSec	0 = 18.88 µs 1 = 37.77 µs	Sets time grid for EOF/Slot Marker for ISO15693
B3	—	—	RFU
B2	4_bit_RX	0 = Normal RX 1 = 4 bit RX	Enables 4 bit RX for MIFARE Ultralight and my-d™ move (see file type2.c in TRF7960A reference firmware)
B1	14_anticoll	0 = Anti-collision framing (0x93h, 0x95h, or 0x97h) 1 = Normal Framing	Disable anti-collision frames for ISO14443A (this bit should be set to 1 after completion of anti-collision sequence)
B0	Col_7_6	0 = 7 subcarrier pulses 1 = 6 subcarrier pulses	Selects the number of subcarrier pulses that trigger a collision error in ISO14443A at 106 kbps

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