Application Note

DC Parameters: Input Offset Voltage (V_{OS})

Richard Palmer and Katherine Li

Abstract

The input offset voltage (V_{OS}) is a common DC parameter in operational amplifier (op amp) specifications. This report aims to familiarize the engineer with the basics and modern aspects of V_{OS} by providing a definition and a detailed explanation of causes of V_{OS} for BJT, JFET, and CMOS devices. The article centers around measurement techniques, data sheet specifications, the effect of V_{OS} on circuit design, and the trim methods to correct it.

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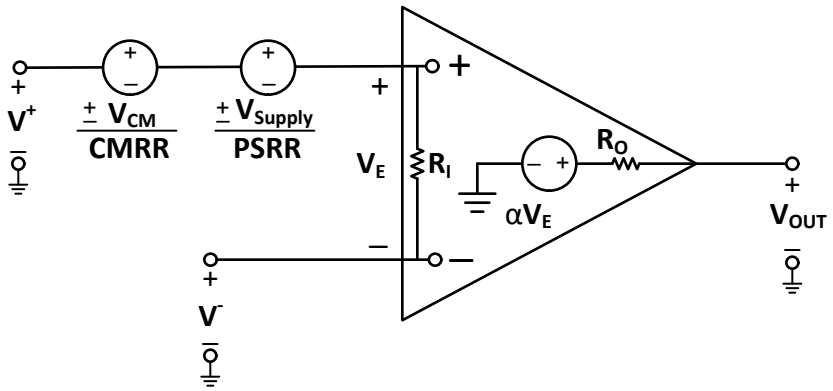
1 Introduction

Op amps find extensive use in a wide variety of circuits, and their appropriate specification for a particular application requires knowledge of relevant data sheet parameters. Data sheet specifications are divided into two general categories: DC parameters and AC parameters. The DC parameters represent internal errors that occur as a result of mismatches between devices and components inside the op amp. These errors are always present from the time the power is turned on (for example, before, during, and after any input signal is applied), and they determine how precisely the output matches the ideal op amp model. Thus, the precision of the op amp is determined by the magnitude of the DC errors.

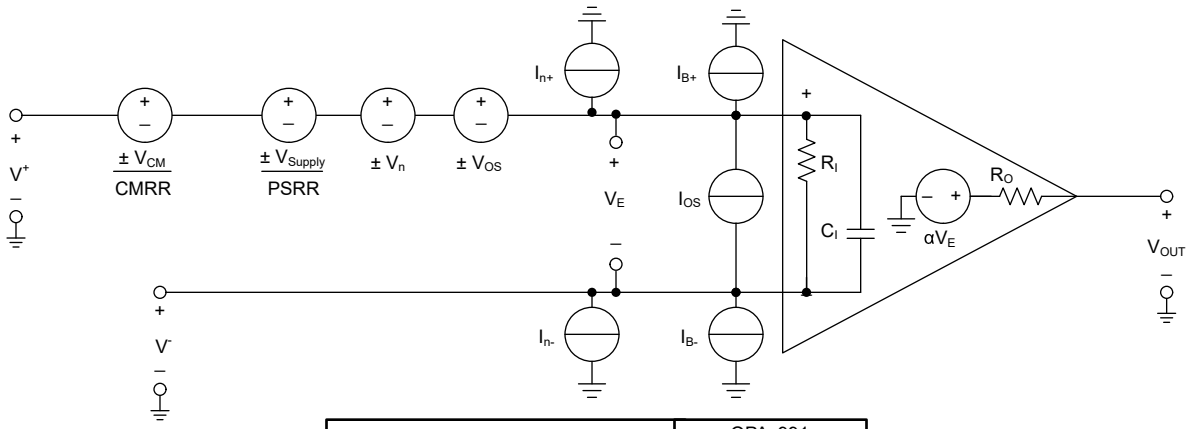
The objective of this report is to provide the information necessary for the designer to understand each parameter: what it is; what causes it; and how it is measured, trimmed, and specified.

Figure 1-1 presents an ideal op amp model together with a table of ideal parameters (see *Understanding Basic Analog – Ideal Op Amps* for more information on the ideal op amp). The general assumptions listed in the table simplify design analysis and provide a good first order approximation that is reasonable when the op amp limits are not being pushed. Most applications, however, use the op amp to the fullest extent for one or more parameters and require more detailed analysis. It is then that the non ideal, or real, op amp model must be used. Figure 1-2 shows this non ideal op amp model and uses the OPAx991 as an example for the op amp typical parameter values.



PARAMETER	IDEAL VALUE
Open-loop Gain (α, A_{OL})	∞
Open-loop Input resistance (R_I)	∞
Open-loop Output resistance (R_O)	0
Common-mode rejection ratio (CMRR)	∞
Power-supply rejection ratio (PSRR)	∞
Error Voltage (αV_E)	0

Figure 1-1. Ideal Op Amp Model and Model Parameters



PARAMETER	OPAx991	
	TYP VALUE	UNITS
Open-loop Gain (α, A_{OL})	145	dB
Open-loop Output resistance (R_O)	525	Ω
Common-mode rejection ratio (CMRR)	130	dB
Power-supply rejection ratio (PSRR)	± 0.3	µV/°C
Input capacitance (C_I)	540 || 9	GΩ || pF
Input bias current (I_{B+}, I_{B-})	±10	pA
Input noise current (I_{n+}, I_{n-})	2	fA/√Hz
Input offset current (I_{OS})	±10	pA
Input offset voltage (V_{OS})	±125	µV
Input noise voltage (V_n)	0.3	$µV_{RMS}$

Figure 1-2. Non ideal Op Amp Model

2 Input Offset Voltage Defined

The input offset voltage (V_{OS}) is defined as the voltage that must be applied between the two input terminals of the op amp to obtain zero volts at the output. V_{OS} is symbolically represented by a voltage source that is in series with either the positive or negative input terminal (it is mathematically equivalent either way). V_{OS} is considered to be a DC error and is present from the moment that power is applied until it is turned off, with or without an input signal. It occurs during the biasing of the op amp and its effect can only be reduced, not eliminated.

It can be either negative or positive in polarity and can vary from device to device (die to die) of the same wafer lot. Figure 2-1 shows the distribution of V_{OS} measured in one wafer lot of the OPA2991 op amp as an example of the variance that V_{OS} can have.

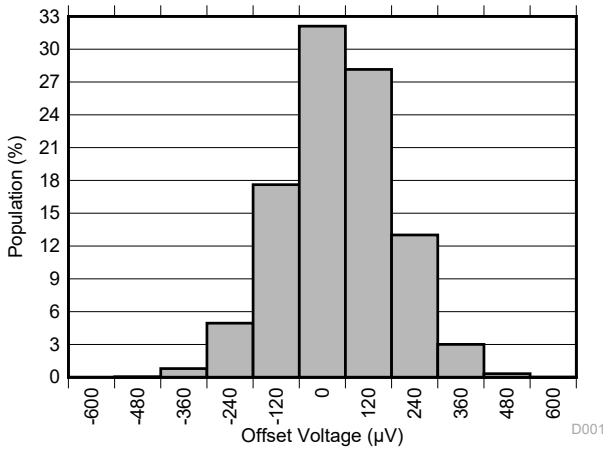


Figure 2-1. Distribution of V_{OS} for the OPA2991

3 Cause of V_{OS}

The cause of V_{OS} is well known: it is mostly due to the inherent mismatch of the input transistors and components during fabrication of the silicon die, but stresses placed on the die during the packaging process have a minor contribution. These effects collectively produce a mismatch of the bias currents that flow through the input circuit, and primarily the input devices, resulting in a voltage differential at the input terminals of the op amp. V_{OS} has been reduced with modern manufacturing processes through increased matching and improved package materials and assembly.

The input stage of most op amps consists of a differential pair amplifier. A simplified version is shown in Figure 3-1, where Q_1 (+ or non-inverting input terminal) and Q_2 (– or inverting input terminal) can be BJT, FET, or MOS transistors. The input terminals of the op amp are the bases (BJT) or gates (FET, MOS) of these transistors. The current source biases the transistors, and ideally each leg of the circuit is balanced so that one half of the current flows through each transistor ($I_{Q1} = I_{Q2} = \frac{I_{REF}}{2}$) and the inverting and non-inverting inputs are at the same potential. Mismatches in R, Q_1, and Q_2 unbalance this current. The base (gate) voltages of the transistors then become unequal, creating the small differential voltage V_{OS}.

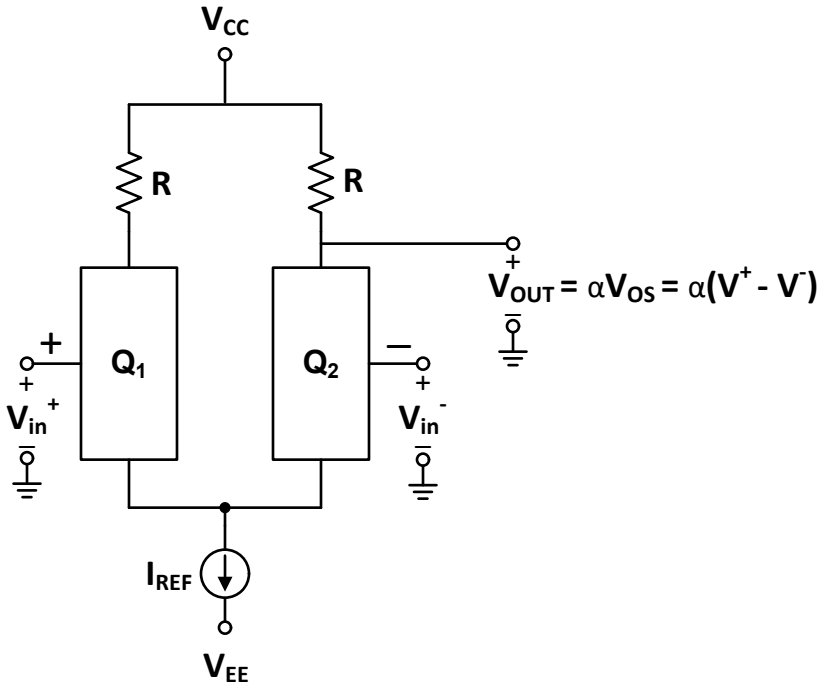


Figure 3-1. Simplified Differential Pair Amplifier. Q1 and Q2 are BJT, FET, or MOS

When the op amp is open-loop, this small differential voltage is multiplied by the open-loop gain of the amplifier (A_{OL} or α). At the very least, the output dynamic range will be greatly reduced. Normally, however, the output of the op amp is driven to one of the power supply rails, saturating the device. When the op amp is operated closed-loop, the differential voltage is multiplied by the non-inverting closed-loop gain of the op amp, which is set by the circuit designer.

4 V_{OS} and Temperature Drift in the Major Device Types

There are three major manufacturing processes in which most op amps can be grouped: bipolar, JFET, and CMOS. The magnitude of V_{OS} varies, but each process has a range associated with it. Table 4-1 shows the range and drift associated with each process type and lists the typical, max, and full range V_{OS} for various op amps of each type. A brief description of each process and the mechanism of V_{OS} and drift for that particular process are described below. See Gray and Meyer [2] and Dostál [3] for more detail concerning V_{OS} and drift for the processes described in this section.

Table 4-1. Range of Input Offset Voltage and Drift Per Device Process

†Typical specifications *Laser trimmed

Note: Devices listed are commercial, ranges valid for all temperature ranges

Process	Device Type	Year	V_{OS} †at 25 °C (µV)	$\Delta V_{OS}/\Delta T$† (µV/°C)
Bipolar	LM2904B	2019	300	3.5
	LM2902B	2022	300	7
	TLV6003	2019	390	2
JFET	OPA462	2018	200	4
	OPA828*	2018	50	0.45
CMOS	OPA2991	2019	125	0.3
	TLV9041	2021	600	0.8
	OPA2310	2022	250	0.5
	TLV9162	2021	210	0.25

4.1 Bipolar

Bipolar op amps consist solely of bipolar junction transistors (BJTs). A wide range of performance specifications are available, ranging from low performance, widely used relics such as the LM324, to the more contemporary op amps such as the LM2904B and the precision op amp OPA828.

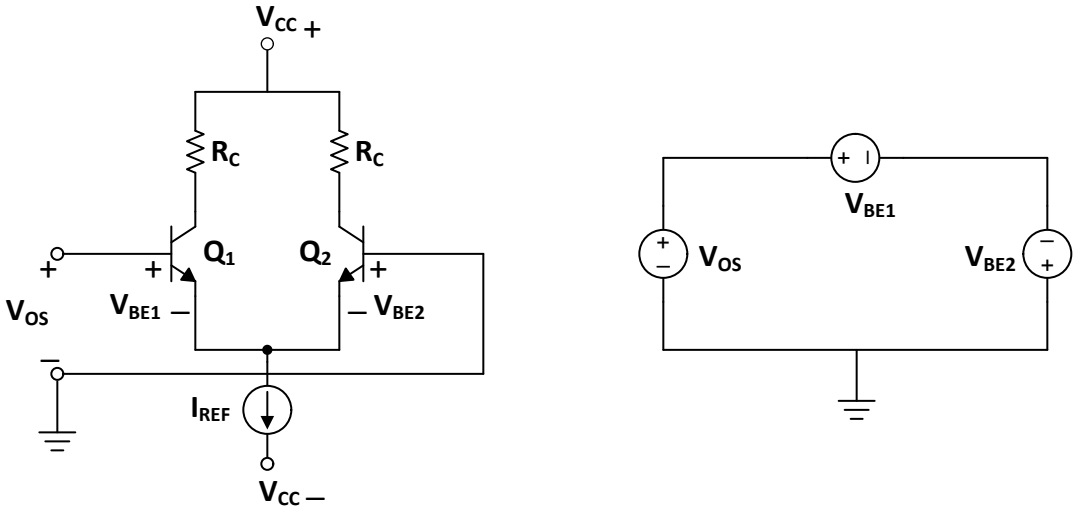


Figure 4-1. Bipolar Transistor Differential Pair Circuit. (left) Basic Circuit and (right) General Circuit Used to Calculate V_{OS}

Substituting bipolar NPN transistors for Q_1 and Q_2 in the circuit of Figure 3-1 and setting $R = R_C$ provides the basic NPN bipolar differential input circuit shown on the left in Figure 4-1. Small resistors can also be placed at the emitter of the devices to improve linearity and speed at the cost of increased noise and decreased open-loop gain. This is normally done because it increases stability, but the effect is not discussed here.

In the bipolar process, V_{OS} is created primarily by differences in the base width, emitter area, and doping levels of the base and collector of transistors Q_1 and Q_2 (see Gray and Meyer [2]). These errors create differences in

the bias currents flowing in the base of the differential pair. The overall result is a difference in the V_{BE} values of $Q_1$and Q_2, which causes the differential voltage V_{OS} to appear across the op amp inputs.

When the inputs are grounded, a loop is formed as shown on the right in Figure 4-1. Kirchoff's Voltage Law (KVL) is then used to obtain Equation 1, rewritten in the form of Equation 2. V_{BE} is defined in Equation 3, where the term kT/q is known as the thermal voltage (V_T), I_C is the collector current, and I_S is the reverse saturation current. Then is substituted into Equation 2 and manipulated into the form in Equation 4:

$$-V_{OS} + V_{BE1} - V_{BE2} = 0 \tag{1}$$

$$V_{OS} = V_{BE1} - V_{BE2} \tag{2}$$

$$V_{BE} = \left(\frac{kT}{q}\right)\ln\left(\frac{I_C}{I_S}\right) \tag{3}$$

$$V_{OS} = \left(\frac{kT}{q}\right)\ln\left(\frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}}\right) \tag{4}$$

The errors introduced in Equation 4 by the I_C terms are due to the mismatch in the RC resistors. The I_S-term errors are due primarily to mismatches in the area of the emitter and the width and doping of the base (see Gray and Meyer [2]). The value of V_T (kT/q) is material-dependent (for example, 26 mV for silicon) and is inherent in all transistors. This term has the largest impact on V_{OS} and its drift with temperature. As T changes, V_{OS} predictably changes, as shown in Equation 5.

$$V_{OS} = V_{OS}(25°C) + \left(\frac{V_{OS}}{T}\right) \cdot \Delta T \tag{5}$$

4.2 JFET

JFET op amps consist of a JFET input stage and BJTs in the gain and output stages. These devices typically have the highest V_{OS} and temperature drift of the 3 process types. This can be attributed to the transconductance of the JFET, which is lower than that of the BJT (see Gray and Meyer [2]). DC precision is sacrificed in JFET op amps, so they are generally used when a high input impedance or AC performance is needed.

The JFET differential input circuit is the same as the bipolar circuit shown in Figure 4-1 with JFET transistors substituted for Q_1 and Q_2. The collector load resistor R_C now becomes the drain load resistor R_D. Again, Kirchoff's Voltage Law is used to derive Equation 6. V_{GS} is defined in Equation 7, assuming the JFET is a square-law device, and substituted into Equation 6 to get Equation 8.

$$V_{OS} = V_{GS1} - V_{GS2} \tag{6}$$

$$V_{GS} = V_P\left[\ 1 - \sqrt{\frac{I_D}{I_{DSS}}}\ \right] \tag{7}$$

$$V_{OS} = (V_{P1} - V_{P2}) - V_{P1}\sqrt{\frac{I_{D1}}{I_{DSS1}}} + V_{P2}\sqrt{\frac{I_{D2}}{I_{DSS2}}} \tag{8}$$

The JFET is much more sensitive to changes in bias current from mismatches in the channels of Q_1, Q_2, R_D, and I_{REF}, resulting in a higher overall V_{OS} than the bipolar differential input stage. V_{OS} for the JFET process is primarily created by mismatching of the pinch-off voltages (V_P) of the devices as represented in the first term (in parentheses) of Equation 8. The channel doping level and thickness are the components of V_P that create this error. The second and third terms also have some error introduced by V_P as well as error introduced by I_D through the mismatching of R_D and I_{DSS} caused by the channel geometry and doping levels of the input transistors. The overall result is a difference in the V_{GS} voltages of Q_1 and Q_2, causing V_{OS} to appear across the op amp inputs.

Overall V_{OS} is calculated for JFET similar to bipolar using Equation 5.

4.3 CMOS

CMOS op amps consist of complimentary MOS transistors (NMOS and PMOS together) throughout the device. CMOS devices typically have a low V_{OS} and the lowest drift of all three processes.

The CMOS differential input circuit is the same as that of the bipolar in Figure 3-1, with MOS transistors substituted for Q_1 and Q_2. The loop equation derived is identical to Equation 6. The MOSFET definition for V_{GS} in Equation 9 is substituted into Equation 6 and manipulated into the form of Equation 10. Here, V_{OS} is primarily due to differences in the threshold voltage, V_T (not to be confused with the thermal voltage, V_T, of bipolar devices). These are caused by variations in the width, length, thickness, and doping levels of the channels in the transistors (see Gray and Meyer [2]).

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{k'} \cdot \frac{L}{W}} \tag{9}$$

$$V_{OS} = (V_{T1} - V_{T2}) + \sqrt{\left(\frac{2I_{D1}}{\mu C_{OX}} \cdot \frac{L_1}{W_1}\right)} - \sqrt{\left(\frac{2I_{D2}}{\mu C_{OX}} \cdot \frac{L_2}{W_2}\right)} \tag{10}$$

5 Manufacturer Measurement, Trim, and Specification of V_{OS}

The salient DC parameters for any device are printed in the data sheet. To fully understand the specifications on the data sheet, it is necessary to understand the methods used by the manufacturer to measure and then trim (reduce) V_{OS}. This section briefly explains how the measurement and trim process is performed. It then explains and provides examples of the specifications for various devices.

5.1 Measurement

Most of the parameters are measured using a servo loop. Figure 5-1 shows a simplified circuit. This test loop is used for the major DC parameter measurements. V_{OS} is measured with switches S_1 and S_2 closed, essentially providing a very low source impedance to ensure that input bias current offsets are negligible during the measurement. The inverting input of op amp A_1 controls the output of the device under test (DUT) through the feedback loop containing R_F and the 50-Ω resistor. When S_3 is closed, A_1 drives the output voltage of the DUT to zero by applying the necessary voltage to the positive terminal. Thus, the voltage across the 50-Ω resistor is equal to V_{OS}, and the output of A_1 is $(R_F/50)V_{OS}$. R_F is adjusted depending on the expected offset voltage of the DUT so that the output of A_1 is not saturated, yet is easily discerned.

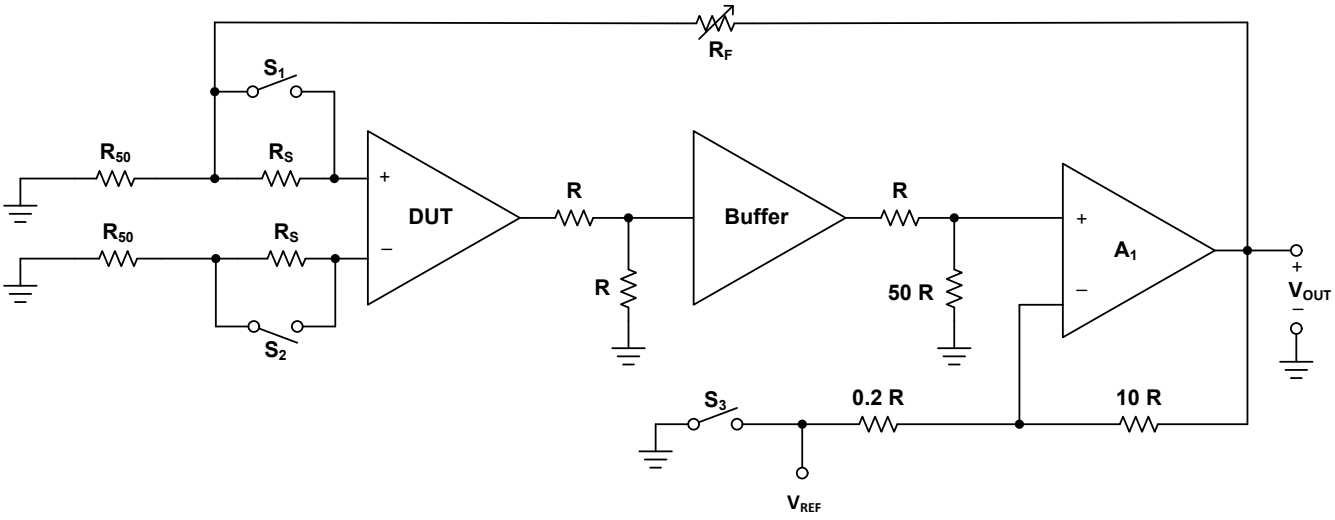


Figure 5-1. Simplified Servo Loop Test Circuit

5.2 Trim

Most op amps have some form of offset trim that is performed during the manufacturing process. The op amps with bipolar and JFET inputs use a Zener diode trim technique to reduce the offset voltages. This method places a network of Zener diodes with series resistance in parallel with the biasing collector-drain resistor. The Zener diodes are then blown as required to increase the parallel resistance, lowering the overall biasing resistance in the desired leg of the circuit.

Op amps with CMOS inputs use a fuse-link trim network because a CMOS diode structure is not available. This method places a fuse in series with resistors, rather than a Zener diode. When the fuse is removed, the parallel resistance is decreased, and the biasing resistance is increased in the desired leg of the circuit.

Laser trim is another alternative that is often used to lower V_{OS}. A resistor network is created, and then portions of it are eliminated to increase or decrease the resistance and balance the currents in each leg of the differential pair. This is a more exact technique and is reserved for precision parts.

Devices in multiple op amp packages (duals and quads) often have less trim capability. This is because the space is reduced on the silicon die for adding trim networks. Multiple op amps on a package, particularly the quads, use up all available space. One or more op amps on a quad package can therefore have a higher offset rating than the single or dual packaged devices, although good design and layout of the IC often prevents this.

5.3 Specifications

The very name input offset voltage indicates that it has been referred to the op amp input. This is done with all of the error sources because the actual output created by any error source depends on the closed-loop gain (A_{CL}) of the circuit, as seen from the error source. Thus, V_{OS} must be multiplied by the non-inverting circuit's A_{CL} to be referenced to the output.

Table 5-1. Example of V_{OS} Specifications Taken from OPA2991 Data Sheet

For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPA991, OPA2991 V_{CM} = V–			±125	±750	µV
			T_A = –40°C to 125°C			±780	
		OPA4991 V_{CM} = V–			±125	±830	
			T_A = –40°C to 125°C			±850	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.3		µV/°C

Table 5-2. Temperature Designators when Ambient Temperature Specified

The designator comes after the part name and before the package name.

Designator	Ambient Temperature Range	Designator Meaning
C	**0°C to 70°C**	**Commercial**
I	-40°C to 85°C	Industrial
T	-40°C to 105°C	N/A
Q	-40°C to 125°C	Automotive
E	-40°C to 150°C	Extended
M	-55°C to 125°C	Military

Table 5-1 shows the V_{OS} portion of the OPA2991 data sheet. Each V_{OS} specification has a column on the data sheet for the minimum, typical, and maximum values to be listed. There are three major V_{OS} specifications that may be provided for an op amp: V_{OS} at 25°C, V_{OS} full range, and drift over temperature ($\Delta V_{OS}/\Delta T$). In the past, devices fell under specific operating temperature ranges with letter designators as shown in Table 5-2. However, most new devices have a temperature range from –40°C to +125°C regardless of application. Some devices are also marked with letters such as A or B. These grades indicate the accuracy of the part—the better the quality (grade), the lower the DC errors. This is not always the case, so always check the data sheet for the actual V_{OS} specifications.

The first entry is for V_{OS} under static temperature conditions, where the maximum and typical values are listed for a temperature of 25°C. This specification is listed on virtually all op amp data sheets and is expressed in millivolts (mV) or microvolts (µV). It is possible that natural variations or future changes in the process used to create a device result in a V_{OS} that is much different from the typical value. Every device is tested at the factory to ensure that it does not exceed the maximum specified value before it is shipped to the customer, so a robust design may require a designer to look at maximum instead of typical values.

On a data sheet, V_{OS} full range is usually only provided with a maximum rating. This specification lists the worst possible V_{OS} that can be encountered over a specified temperature range. Occasionally, the full range is specified for a temperature range less than the maximum operating temperature range, so strict attention must be paid to the conditions.

The drift of a device with temperature is indicated by $\Delta V_{OS}/\Delta T$. This is an average that is calculated using the ends of the specified temperature range as shown in Equation 11. For example, V_{OS} for many parts is measured at –40°C (T_{A1}) and 125°C (T_{A2}) and the results are calculated and expressed as the number of microvolts of increase in V_{OS} per degree Celsius of temperature change (µV/°C). Drift is usually given as a typical value on data sheets. Note that only maximum values are production tested by TI, so look at the full range data or measure drift to get a more complete understanding of the device's drift.

$$\frac{\Delta V_{OS}}{\Delta T} = \frac{V_{OS}(T_{A1}) - V_{OS}(T_{A2})}{T_{A1} - T_{A2}} \quad (11)$$

Some devices have multiple slopes in their drift plot, so Equation 12 is used. This is useful when there are different slopes in different regions, since a calculation over the whole range would show only a small drift when there could be larger drifts which cancel.

$$\frac{\Delta V_{OS}}{\Delta T} = \frac{|V_{OS}(T_{A1}) - V_{OS}(25°C)| + |V_{OS}(T_{A2}) - V_{OS}(25°C)|}{|T_{A1} - T_{A2}|} \quad (12)$$

Figure 5-2 shows V_{OS} measured from –40°C to 125°C (a typical temperature range) for several devices and compares the V_{OS} drift behavior. The slope of each line indicates the magnitude of drift, or $\Delta V_{OS}/\Delta T$, for that part. The steeper the line, the greater the $\Delta V_{OS}/\Delta T$. The OPA2991 is shown to have less drift over temperature as compared to the LM358B. A designer should consider the full drift range behavior if temperature variance is expected in the application.

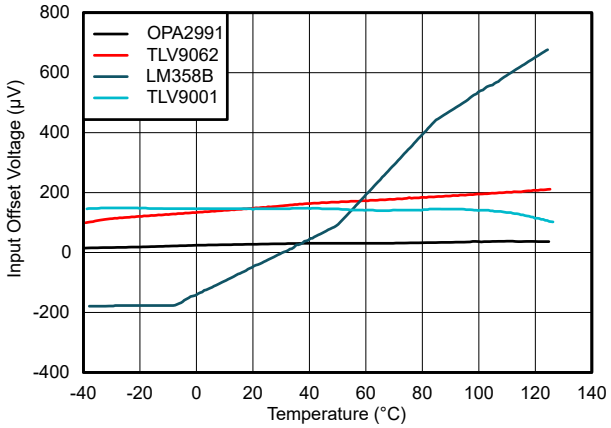


Figure 5-2. V_{OS} Drift Over Temperature

Figure 5-3 and Figure 5-4 is an example of the relationship between V_{OS} and the input common mode voltage (V_{CM}) using TLV9161, OPAx991, and TLV07xH. Since V_{OS} is normally tested at one value of V_{CM}, such graphs are useful in inferring behavior that is not specified in the data sheet. They provide the designer with an understanding of the behavior of the device over a wide range of values.

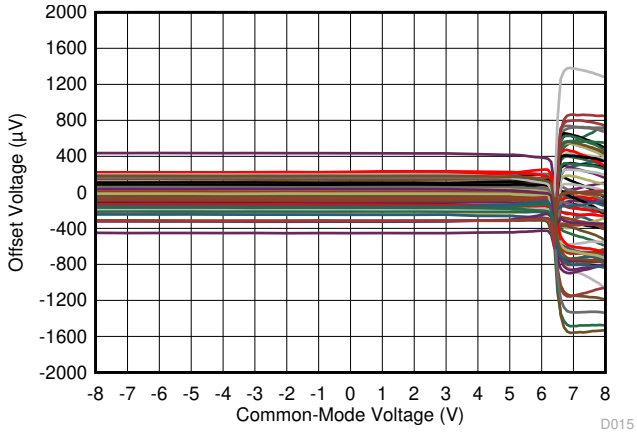


Figure 5-3. V_{OS} vs. V_{CM} for the TLV9161 Op Amp

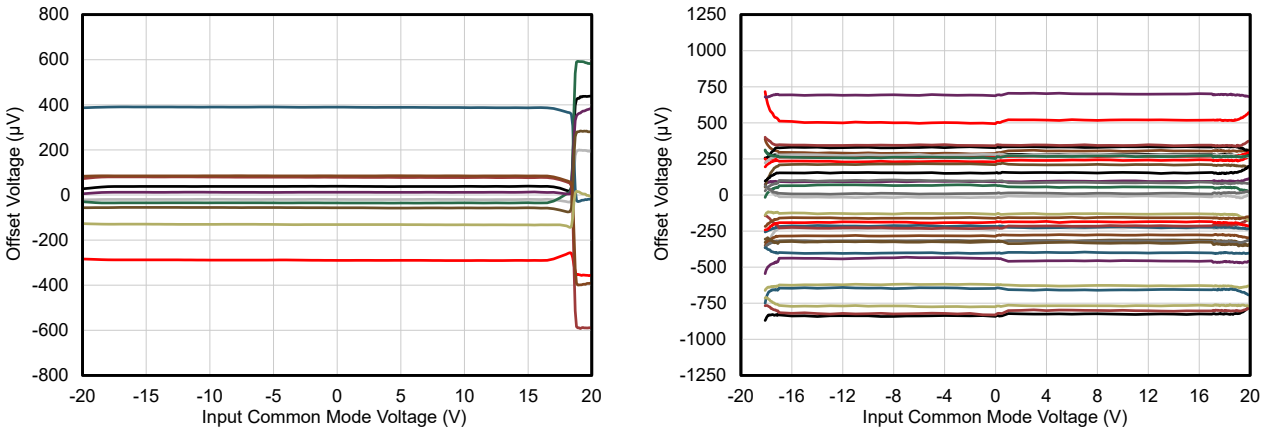


Figure 5-4. V_{OS} vs. V_{CM} for the OPAx991 (Left) and the TL07xH (Right)

6 Impact of V_{OS} on Circuit Design and Methods of Correction

Table 6-1. Range of Input Offset Voltage and Drift Per Device Process Technology

†Typical specifications

Note: Devices listed are commercial, ranges valid for all temperature ranges

Device Type	Process	Year	V_{OS} †at 25 °C (µV)	$\Delta V_{OS}/\Delta T$† (µV/°C)	Technology
OPA397	CMOS	2021	20	0.18	e-trim™
OPA2387	CMOS	2020	0.35	0.003	Zero Drift
OPA210	Bipolar	2018	5	0.1	Super Beta
OPA2325	CMOS	2016	40	2	Zero Crossover

Figure 6-1 shows an inverting op amp circuit with V_{OS} included. Superposition is used to find the closed-loop gain of the circuit (A_{CL}) in Equation 13 (see *Understanding Basic Analog - Circuit Equations*).

$$V_{OUT} = V_{IN}\left(\frac{-R_F}{R_G}\right) \pm V_{OS}\left(1 + \frac{R_F}{R_G}\right) \tag{13}$$

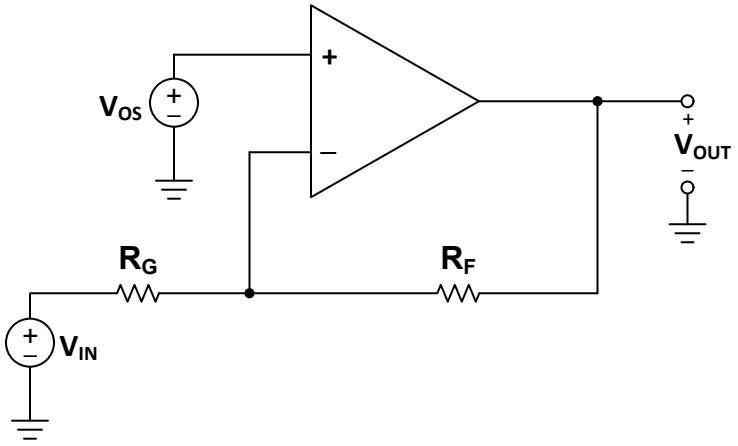


Figure 6-1. Inverting Op Amp Circuit With V_{OS} Included

V_{OS} is always multiplied by the non-inverting gain of the op amp and added to (or subtracted from) the signal gain of the circuit, which is $-(R_F/R_G)$ in this example. In large-gain DC-coupled circuits, V_{OS} can be significant and may need to be reduced through offset adjustment techniques, although an op amp with very low offset may not require adjustment. Normally, adjustment of V_{OS} is used only when the DC accuracy is necessary in order to reduce distortion.

Adding the effects of temperature drift to Equation 13 gives Equation 14. This allows a fairly accurate calculation of the worst-case change in the output due to V_{OS}. However, resistor values also change with temperature and will affect the gain of V_{OS}. Equation 14 focuses only on the effects of drift and does not include the errors from the other DC and AC sources as shown in Figure 1-2 for the nonideal op amp, so it is not completely accurate.

$$V_{OUT} = V_{IN}\left(\frac{-R_F}{R_G}\right) + V_{OS}\left(1 + \frac{R_F}{R_G}\right) + \frac{\Delta V_{OS}}{\Delta T}(T) \tag{14}$$

The first step is to determine the maximum allowable DC error in the system. An error budget analysis must be performed to determine all the DC error sources in the system, and the maximum contribution the design allows for each section. If the op amp or other device fails to meet the specification for V_{OS}, they must be compensated to remove or reduce the offset.

Methods for reducing the effects of V_{OS} include circuit modifications such as AC-coupling and DC feedback. In some applications, the solution is to use devices that have some form of internal calibration, such as chopper stabilization, an auto-zero loop, or offset trim. These methods are briefly described in the following sections.

6.1 AC Coupling

V_{OS} affects the signal conditioning ability of an op amp circuit in both AC-coupled and DC-coupled circuits. Figure 6-2 shows an AC-coupled inverting op amp. The capacitor C_1 AC-couples the input from the previous stage, and C_2 AC-couples the output to the load. Thus, C_1 prevents any DC current from flowing through R_F and R_G (with the exception of bias currents) and C_2 prevents any DC current from flowing into the load. V_{OS} appears across the inputs. Because there is no DC current flow, the amplifier is in unity gain and the output is at the same potential as the inverting input. This is the case even if the output is not DC-coupled (C_2 is not present), because V_{OS} does not appear across R_G. The capacitors also serve to establish some filtering in the circuit.

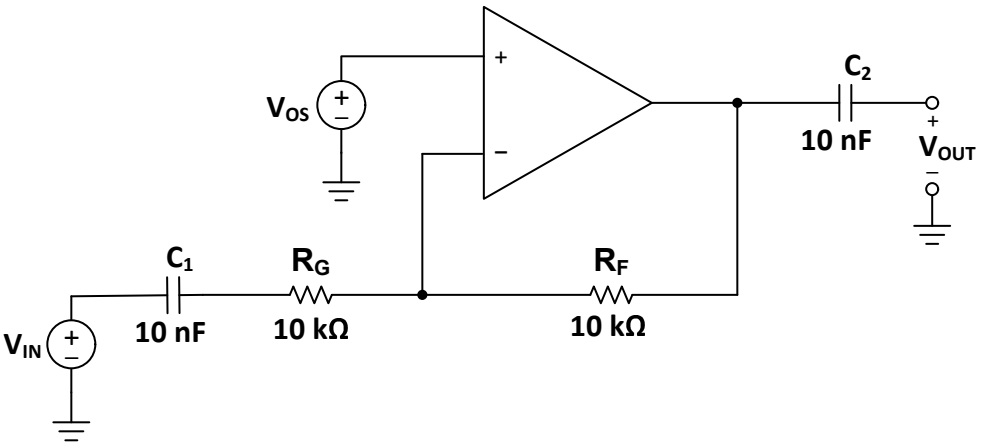


Figure 6-2. AC-Coupled Inverting Amplifier

When C_1 is removed from the circuit, the amplifier is DC-coupled to the signal source. This is the case with many transducers, such as temperature sensors and strain gauges, and DACs. Transducers output voltages, currents, or resistances, and the latter two outputs require conversion to voltage. Such applications require DC conversions, where V_{OS} and the drift play a big part in the accuracy. With C_1 removed, the V_{OS} of the op amp is multiplied by the non-inverting gain ($1+R_F/R_G$) of the circuit, and is added to any DC offset of the source multiplied by the signal gain ($-R_F/R_G$). The worst case is when the two offsets add together. If the gain of the circuit is large, either the dynamic range is greatly reduced or the output is saturated. If C_2 is also removed, the load now has a DC-offset applied, worsening the situation.

Audio power amplifiers use AC-coupling at the input to prevent any DC-voltage component of the input signal from adding to the DC level of the audio circuit (which is normally set to the mid-rail of the power supply for maximum dynamic range). For single-ended loads such as headphones, the output is AC-coupled to prevent any DC voltage from being dropped across the speakers, which might possibly damage the speakers.

V_{OS} also reduces the dynamic range of an ADC. The loss of dynamic range affects the resolution of ADC circuits because maximum dynamic range is required for maximum resolution. Table 6-2 shows the resolution of a least significant bit (LSB) for various input voltage ranges. Usually, an op amp can be chosen with a low enough V_{OS} to meet the desired resolution. It is easy to find an op amp that meets the V_{OS} specification for an 8- or 10-bit converter, but becomes increasingly difficult as the resolution increases. High-speed, low-voltage acquisition circuits can require AC-coupling at the op amp input to remove offset contribution from previous stages. An alternative is AC-coupling the op amp output prior to the ADC input to remove the DC component, particularly if the V_{OS} is higher than desired (see *Op Amps for Everyone*). This is especially true of the high-speed op amps, which often have a high V_{OS}. The number of bits of error introduced by a given V_{OS} is given by the number of bits, equal to $A_{CL}V_{IO}/LSB$, where A_{CL} is the closed-loop gain and LSB is $V_{(fullscale)}/2^N$ is the least significant bit of the ADC.

Table 6-2. Converter Resolution

Number of Bits	Number of Codes	LSB Value		
		2.7V	5 V	10 V
8	256	10.55 mV	19.53 mV	39.06 mV
10	1024	2.64 mV	4.88 mV	9.76 mV
12	4096	659.18 µV	1.22 mV	2.44 mV

Table 6-2. Converter Resolution (continued)

Number of Bits	Number of Codes	LSB Value		
		2.7V	5 V	10 V
14	16,384	164.79 µV	305.18 µV	610.35 µV
16	65,536	41.20 µV	76.29 µV	152.59 µV
18	262,144	10.30 µV	19.07 µV	38.15 µV
20	1,048,576	2.57 µV	4.77 µV	9.54 µV

High-speed amplifier circuits often use AC-coupling of the inputs and outputs to minimize the magnitude of V_{OS}, particularly in circuits that have a high gain. When AC-coupling is not possible or is not feasible for some reason, then DC feedback or op amps with calibration can be employed to reduce V_{OS}.

6.2 DC Feedback

Another method for removing V_{OS} is to use some form of a DC feedback loop. This can be done in many ways, but the general form of the circuit is shown in Figure 6-3. Such a loop is used to limit the V_{OS} of a section of a circuit, usually just before some critical input where the offset must be removed. It reduces the offset voltage to that of the error amplifier only, which can be a DAC, op amp, or some other more elaborate circuit. The DC measurement must be made when there is no input, as represented by the switches. Such offset correction takes a long time to make—usually milliseconds—compared with the speed of the system, and they are made during some noncritical time such as during start-up.

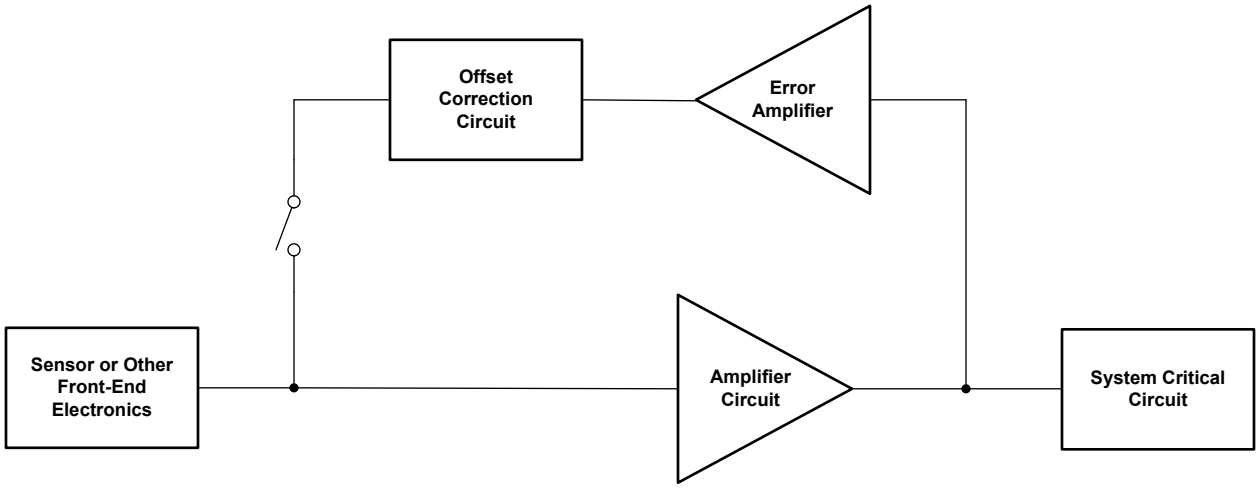


Figure 6-3. General Form of DC Feedback Loop

6.3 Internal Calibration

Some devices offer internal calibration of the input offset voltage and drift. These features are called autocalibration, zero-drift, auto-zero, chopper, or Self-Cal™. Texas Instruments zero-drift op amps are implemented using auto-zero or chopper-stabilized techniques. They both have an internal control loop that nulls out the input offset voltage that is caused by change in temperature, supply voltage, input common-mode or output voltage. For this reason, zero-drift amplifiers not only achieve single-digit µV offset and tens of nV/°C drift but also extremely high AOL, CMRR, PSRR (above 140dB).

In case of auto-zero, a main amplifier, A1, and the nulling amplifier, A2, each have an associated input offset voltage that is stored during sample phase on C_1 and C_2, respectively – see Figure 6-4. In the auto-zero phase the charge from both caps is being transferred to null the total offset. The internal high-order filter is used to minimize switching noise. Some of the first Texas Instruments auto-zero op amps are OPA335 and OPA735 with their maximum offset of ±5uV and maximum drift of ±0.05µV/°C.

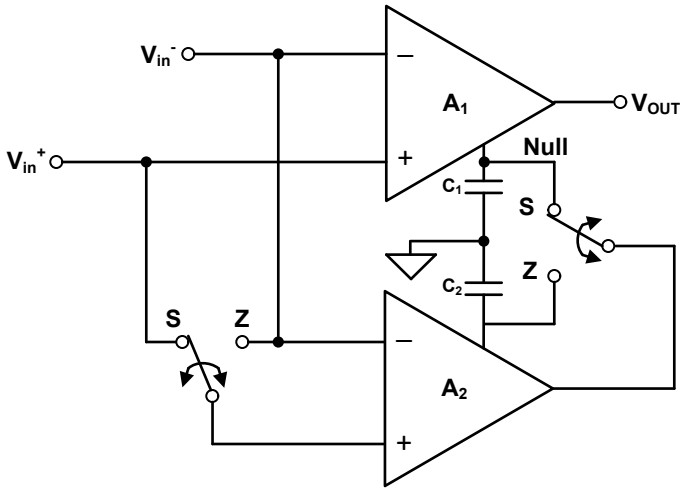


Figure 6-4. Auto-Zero Amplifier

Figure 6-5 shows the input stage of a chopper op amp. The amplifier is a conventional transconductance stage with differential input and differential output current. Chopping is accomplished with commutating switches on the input and output that synchronously reverse the polarity. The offset voltage of the transconductance stage is inside the input switching network, thus its contribution to output is periodically reversed by the output switches. The output current caused by offset voltage causes the voltage on C_1 to ramp up and down at an equal rate. The internal logic assures equal up and down ramp times so the average output voltage on C_1 is zero. Since both differential input and output stages are reversed simultaneously, the net effect on the output capacitor, C_1, is in-phase signal and zero average offset voltage.

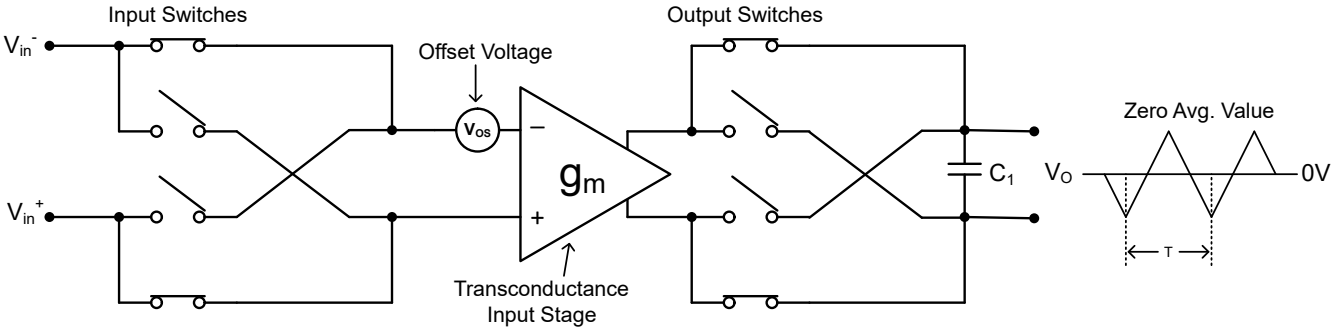


Figure 6-5. Chopper-Stabilized Amplifier

New-generation choppers are dramatically quieter, incorporating a switched-capacitor filter with multiple notches aligned with the chopping frequency and its odd harmonics, while the high frequency input signal bypasses chopping (DC) stage all together using fast-forward (GM_FF) stage – see Figure 6-6. A superior filtering is accomplished by integrating a charge for a full clock cycle before transferring its charge to the next stage of the op amp. Integrated over a full up-down cycle, its net value is zero. In the frequency domain, this creates a sinc(x) or sin(x)/x filter response with nulls that precisely align with the fundamental and all harmonics of the triangle wave. Since 1/f (flicker) noise is merely a slow time-varying offset voltage, choppers virtually eliminate this increased noise-spectral density in the low-frequency range. The chopping shifts the baseband signal to the chopping frequency beyond the input stage's 1/f region. Thus, the low-frequency signal range of choppers has a noise-spectral density equal to that of the amplifier's broadband frequency noise.

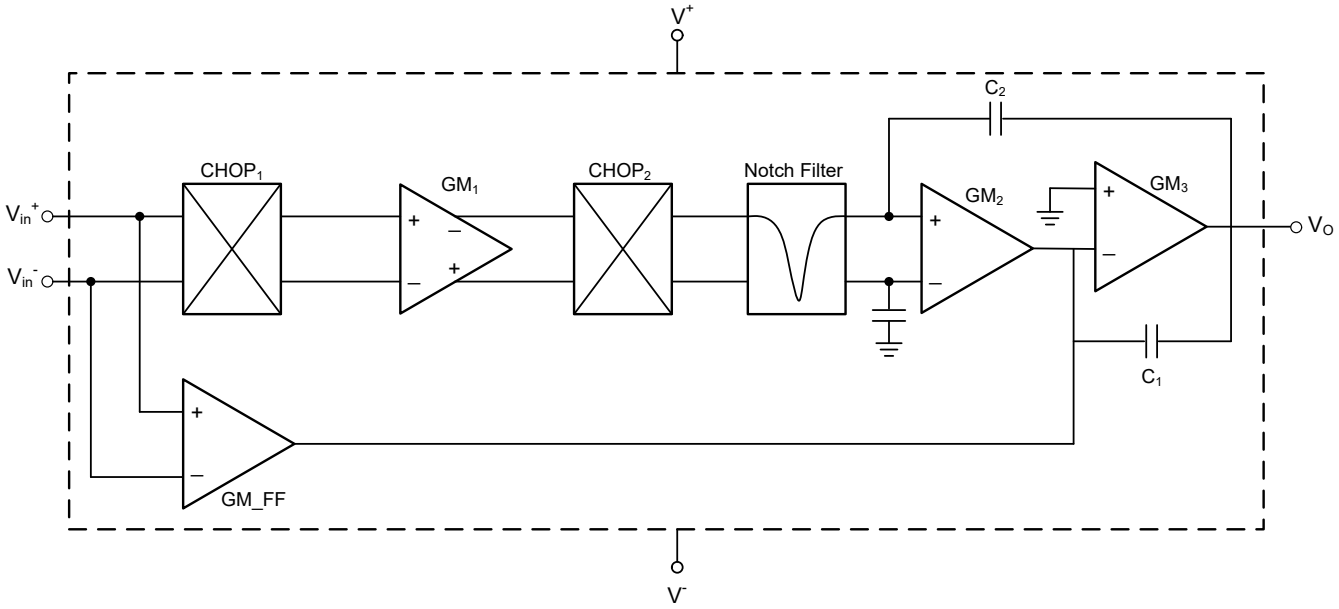


Figure 6-6. Chopper Functional Block Diagram

Some of the recent Texas Instruments' high-voltage chopper amplifiers like OPA182 achieve maximum offset voltage of ±4µV and maximum drift of ±12nV/°C with typical AOL, CMRR and PSRR above 166dB. TI's low-voltage supply choppers like OPA387 maximum offset and drift limits are ±2µV and ±12nV/°C, respectively, while its typical CMRR, PSRR and AOL are all above 145dB. However, the input bias current is affected by the charge and discharge current glitches of the input zero-drift circuitry. This effectively creates repetitive IB current pulses of opposite polarity in 100's of pA. For this reason, the zero-drift amplifiers are not recommended for applications with high source impedances. The amount of IB current sunk or sourced from the input stage is dependent on the combination of input impedance (resistance and capacitance), as well as the balance and matching of these impedances across the two inputs. These positive and negative input current pulses, integrated by the input capacitance, may cause a shift in the apparent "average bias current" that leads to offset voltage shift. Since the input bias average current may be dependent on the input impedance, it is difficult to estimate what the actual input bias current is without knowing the end-circuit and associated parasitic capacitors. For this reason, in order to minimize the offset voltage shift caused by unequal positive and negative I_B pulses, it is important to match the input impedances between the two input terminals.

7 Summary

The DC parameters represent internal errors that occur as the result of mismatches between devices and components inside the op amp. The precision of the op amp is determined by the magnitude of these errors. One of the primary DC errors is the input offset voltage (V_{OS}) and is defined as the voltage that must be applied between the two input terminals of an op amp to obtain zero volts at the output. V_{OS} is symbolically represented by a voltage source that is in series with either the positive or negative input terminal, that can have either negative or positive polarity, and that varies from device to device.

V_{OS} is caused by the mismatch of the input transistors and components, primarily in the input stage of the op amp. Such errors are mostly introduced during fabrication of the silicon die, with a minor contribution from stresses placed on the die during the packaging process. These effects collectively produce a mismatch of the bias currents that flow through the input circuit, resulting in a voltage differential at the input terminals of the op amp.

There are three general manufacturing processes into which most op amps can be grouped: CMOS, JFET, and bipolar. CMOS devices typically have the lowest V_{OS} of the three, and they have the least drift. JFET devices have the worst V_{OS} and temperature drift. Bipolar devices have a V_{OS} that is close to that of CMOS devices, and a low temperature drift.

All devices are tested prior to shipment to the customer to ensure their offset is below the maximum specified in the data sheet. DC parameters are measured using a servo loop and are normally trimmed during this measurement process. Devices in multiple packages often have less trim capability because of limited space available on the die. When this occurs, V_{OS} varies between the single, dual, and quad packages. The op amps with bipolar and JFET inputs use a Zener diode trim technique to reduce the offset voltages. Op amps with CMOS inputs use a fuse-link trim network because a CMOS diode structure is not available. Laser trim is another alternative that is often used to lower V_{OS}.

An op amp's V_{OS} can be found in the op amp's data sheet under the input specifications table. This is done with all the error sources because the actual output created by any error source depends on the closed-loop gain (A_{CL}) of the circuit as seen from the error source. V_{OS} is multiplied by A_{CL} for the non-inverting circuit to be referenced to the output. There are three major V_{OS} specifications that may be provided for an op amp: V_{OS} at 25°C, V_{OS} full range, and V_{OS} drift over temperature ($\Delta V_{OS}/\Delta T$). The specification is fully tested and assured when the maximum or minimum values are listed. Typical specifications are not assured. Data graphs only show typical specification information.

An error budget analysis helps determine all the DC error sources in the system and the maximum contribution the design allows for each section. When the op amp or other device fails to meet the specification for V_{OS}, they are compensated to remove or reduce the offset. Methods of reducing the effects of V_{OS} include AC-coupling and DC feedback. In some applications, the solution is to use devices that have some form of internal or external calibration such as chopper stabilization, an auto-zero loop, or offset trim.

Audio amplifiers, communications circuits, and converters often use AC-coupling to remove V_{OS}. DC feedback is often used in measurement systems that require precision. Many devices such as instrumentation amplifiers, data converters, codecs, processors, and CMOS chopper amplifiers and Self-Cal™ amplifiers correct the offsets internally. Most of these techniques minimize V_{OS} only, and at only one temperature. The chopper amplifiers provide continuous correction, even over a temperature range, so they have very low drift. There are drawbacks to each method of V_{OS} correction that must be considered for each design.

8 References

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2022) to Revision B (March 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated equation 8 *VGS* to *VOS*	6

Changes from Revision * (March 2001) to Revision A (October 2022)	Page
• Updated nomenclature, new devices, and op amp technologies	2

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