Application Report
SLMA007–April 2013

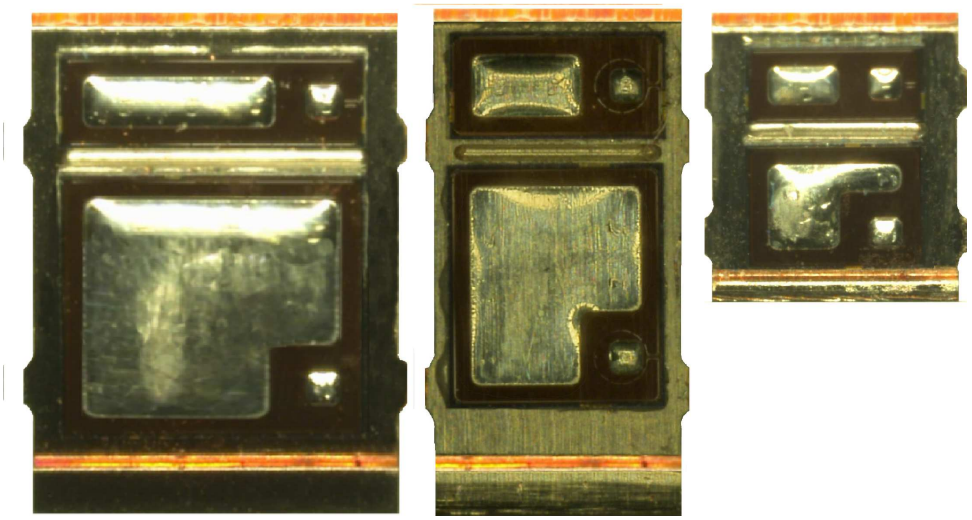
Design Summary Power Block II

High Volume Analog

ABSTRACT

Recent trends in Compact Form Factor Ultra-books and Tablet PCs are driving the electronics industry towards smaller packaging technologies. Texas Instruments (TI) addresses this trend by introducing Power Block II, a family of Synchronous Buck Dual MOSFETs that eliminates molding compound in the package and utilizes industry standard LGA concept in the silicon design. The small footprint, low height, low weight, and higher current capacity of these packages are ideal for a variety of power conversion applications where small-form-factor/space/weight limitations are essential. Power Block II packages are constructed utilizing high performance materials resulting in an ultra thin and thermally efficient packaging solution. Power Block II products reduces source inductance with respect to Industry standard Dual MOSFETs and enable high performance designs with less power dissipation. For more information, visit: www.ti.com

Topic **Page**



	Micro	Nano	Pico
Package Designator	**MPB**	**MPA**	**MPC**
Package [(1)]Width (W)	3,5	2,5	2,5
Package [(1)]Length (L)	5,0	5,0	3,0
Package Thickness (T) Max	0,48	0,48	0,48

(1) Nominal Dimensions Shown for Additional Information See Package Designator at www.ti.com

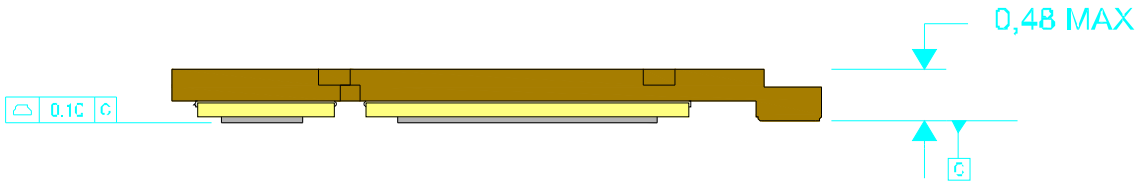


Figure 1. Power Block II Package Illustrated Cross-Section

1 PCB DESIGN GUIDELINES

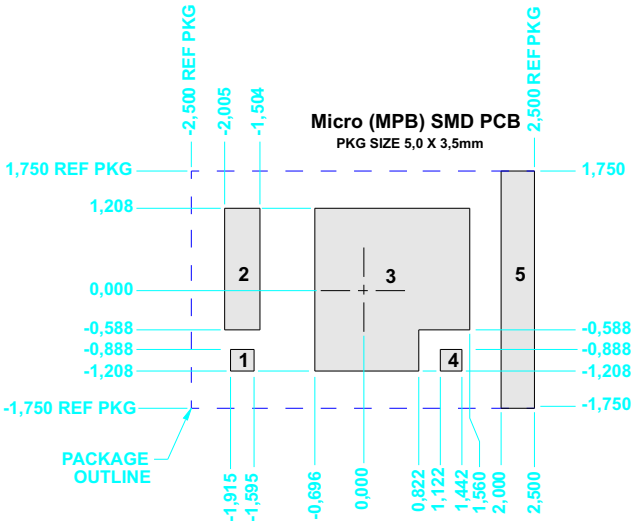


Figure 2. Micro (MPB) - Solder Mask Defined PCB Recommended Layout

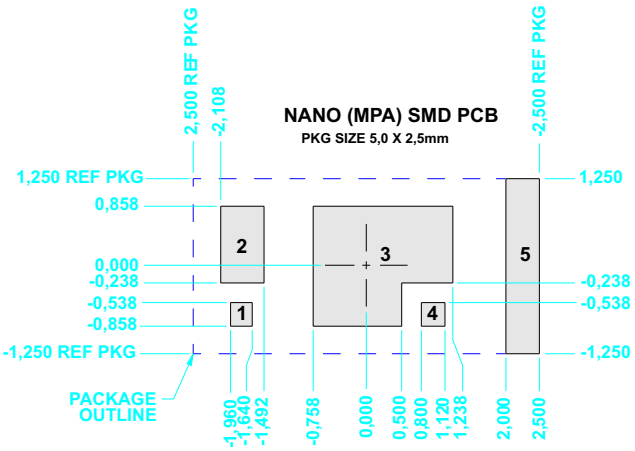


Figure 3. Nano (MPA) - Solder Mask Defined PCB Recommended Layout

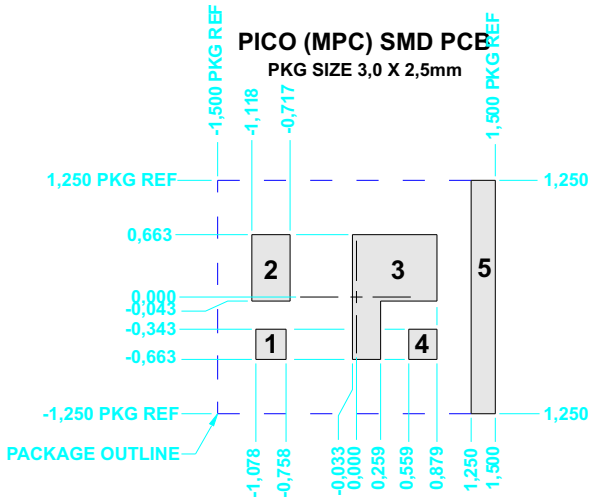


Figure 4. Pico (MPC) - Solder Mask Defined PCB Recommended Layout

2 STENCIL VITALS

TI recommends stencil manufacturing by either; laser cut / electro polished or electroform

2.1 Solder Paste

TI recommends the use of type 3 or finer solder paste when mounting Power Block II family. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the "no clean" compositions are preferred due to the difficulty in cleaning under the mounted components.

The power block II series packages do not require underfill to be utilized.

TI recommends controlled placement pressure in mounting the power block II series packages. Recommended force should be controlled to 5N maximum for static and 2.5N for impact

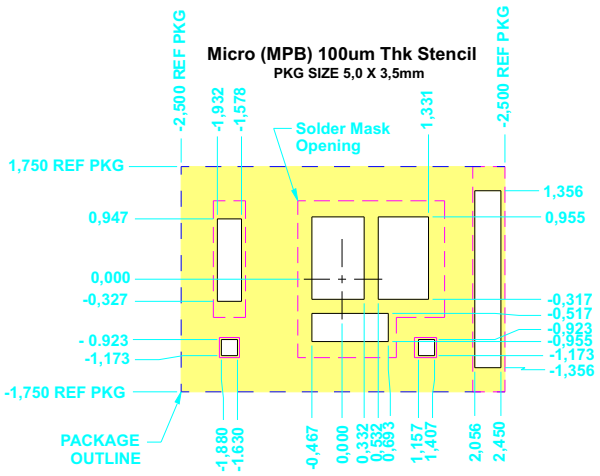


Figure 5. Micro (MPB) – 100µm Stencil Thickness Recommended Layout
Target Solder Thickness after Reflow – Die = 50µm (25/25µm by Dome Print, On TAB = 30µm)

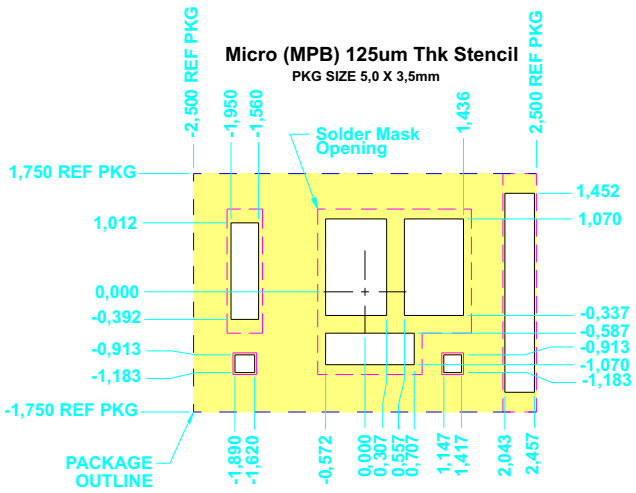


Figure 6. Micro (MPB) – 125µm Stencil Thickness Recommended Layout
Target Solder Thickness after Reflow – Die = 63µm (25/38µm by Dome Print, On TAB = 43µm)

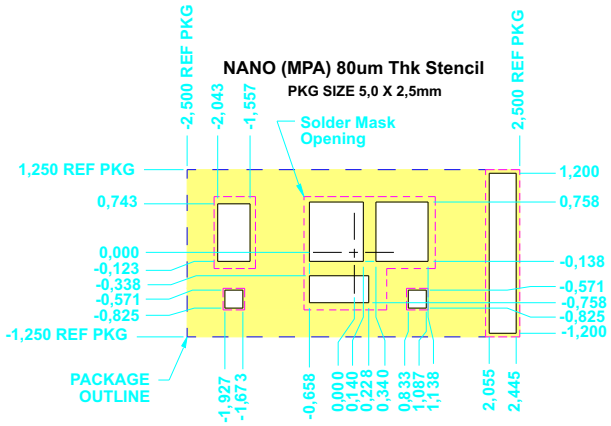


Figure 7. Nano (MPA) – 80µm Stencil Thickness Recommended Layout
Target Solder Thickness after Reflow – Die = 50µm (25/25µm by Dome Print, On TAB = 30µm)

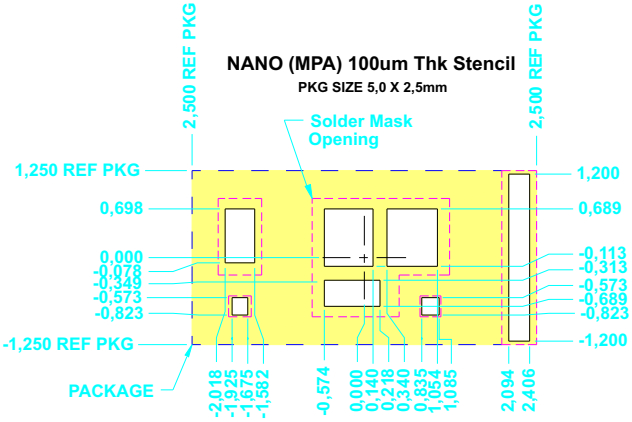


Figure 8. Nano (MPA) – 80µm Stencil Thickness Recommended Layout
Target Solder Thickness after Reflow – Die = 50µm (25/25µm by Dome Print, On TAB = 30µm)

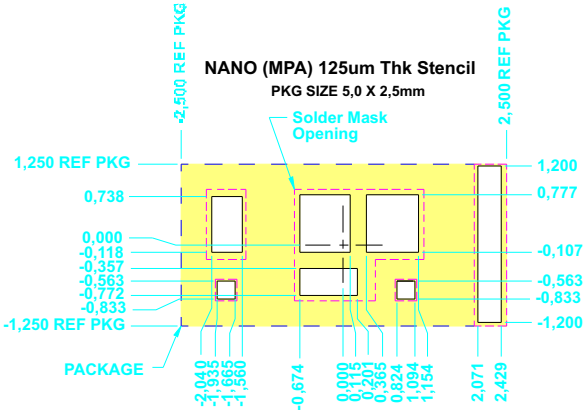


Figure 9. Nano (MPA) –125um Stencil Thickness Recommended Layout
Target Solder Thickness after Reflow – Die = 63um (25/38um by Dome Print, On TAB = 43um)

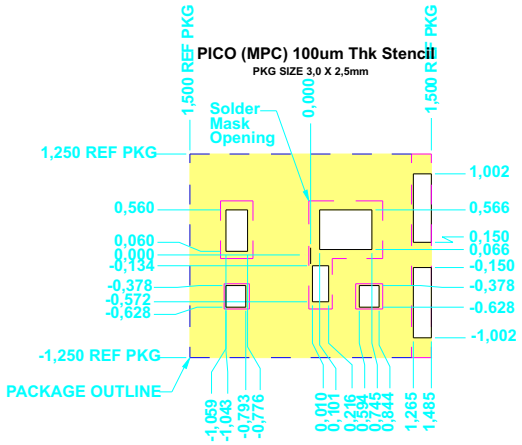


Figure 10. Pico (MPC) –100um Stencil Thickness Recommended Layout
Target Solder Thickness after Reflow – Die = 50um (25/25um by Dome Print, On TAB = 30um)

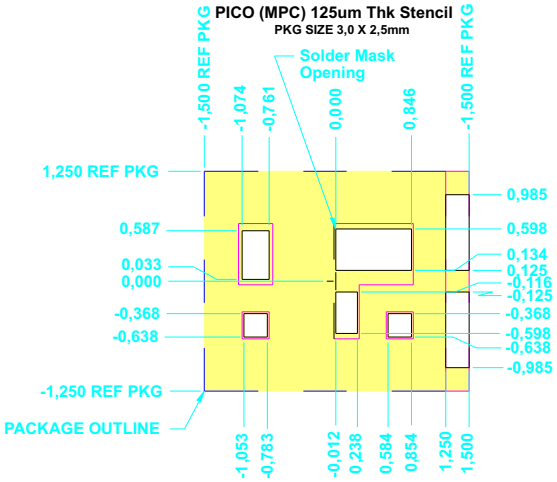
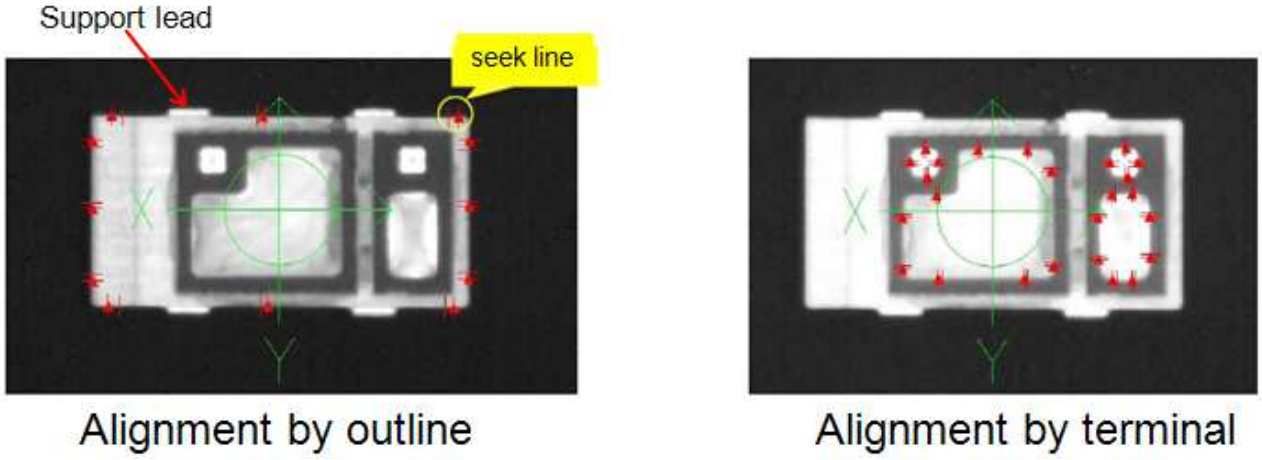


Figure 11. Pico (MPC) –125um Stencil Thickness Recommended Layout
Target Solder Thickness after Reflow – Die = 63um (25/38um by Dome Print, On TAB = 43um)

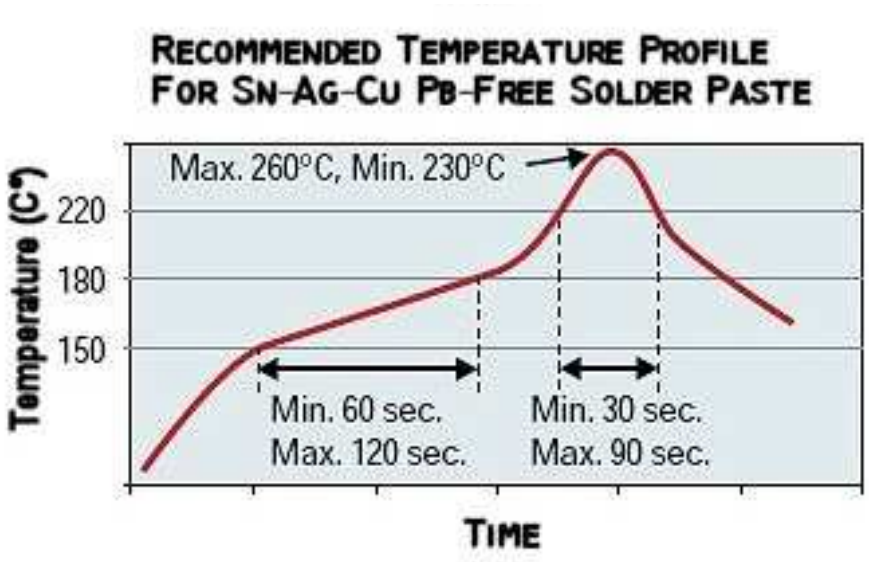
3 PACKAGE PLACEMENT

- Alignment should be done by package outline or terminals
- Package outline image recognition is recommended because it is more accurate



	JEDEC Pb Free Profile Example
Ramp Rate	3°C/sec. Max.
Preheat	150 to 180°C
	60 to 120 sec.
Time Above Liquidus	220°C
	30 to 90 sec.
Peak Temp.	260°C +0/-5°C
Time Within 5°C Peak Temp.	10 to 20 sec.
Ramp Down Rate	6°C/sec. Max.

Temperature profile above is JEDEC Pb Free reflow compliant and shown as example only,



4 QUESTIONS & ANSWERS

Q. Is package rework possible? Are tools available?
A. Yes, rework is possible, and there are several semi-automatic SMT rework machines and profiles available. However, TI does not guarantee the reliability of re-used packages. It is best to discard and replace any package that fails test. Please refer to the repair guideline section of this document for more details.

Q. Can the solder come off during shipping?
A. No, this has never been observed. The solder is 100 percent inspected for co-planarity and other physical properties prior to packing for shipment.

Q. What size land diameter for these packages viashould I design on my board?

A. Land size is the key to board-level reliability, and Texas Instruments strongly recommends following the design rules included within this summary.

Q. Can customers mount Power Block packages on the bottom side of the PCB board?

A. Yes, they can and the ideal 2nd reflow profile is the same as the 1st.

Q. Are there pressure requirements for mounting PBII packages?
A. TI recommends controlling the placement pressure in mounting the PBII package. Thus force should be controlled to 5N maximum for static and 2.5N for impact.

Q. If I want to add a heat sink to the package, what is recommended maximum torque force I can apply?

A. A heat sink can be added to package after its successfully mounted to PCB. A thermal pad is a recommended addition between package and heat sink to insure thermal conductivity. And torque force applying the heat sink should not exceed 2.7 pound-force lbs (12 N).

Q. Has TI developed a lead-free version of Power Block II?

A. Yes, Texas Instruments has developed the power block II series as Pb-Free option in order to comply with lead-free environmental policies.

Q: What routing choices do I have when using Power Block PBII packages?

A: The pad design is wide enough to allow for via-in-pad routing techniques to be employed on an economical basis.

Q. Can the solder joints be inspected after reflow?

A. Many customers are achieving satisfactory results during process setup using X-ray techniques

Q. Any EMI concerns for traces under the package and how can customers design their board to minimize EMI?
A. EMI can be controlled by minimizing any complex current loops on the PCB trace. Some helpful hints include:

- Solid ground and power planes can be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops increasing radiation.
- Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance causing signal degradation.
- Minimize power supply loops by keeping power and ground traces parallel and adjacent to each other. Significant package EMI can be reduced by using this method.

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