Driver Workarounds for TUSB73x0 USB3.0 xHCI Host Controller Errata

Consumer and Computing Interface

This document serves to capture errata items and corresponding driver workarounds on the TUSB7320 and TUSB7340 xHCI Host Controllers. The TI-provided Windows drivers incorporate these workarounds.

	Problem Description	Driver Workaround
1	Host controller port link state fails to go to Recovery when device initiates a U1_EXIT.	Disable U1/U2: Set PORTPMSC U1 timeout and U2 timeout to 0xFF.
2	When a RX data packet spans multiple data buffers, The host controller requires the start address of all data buffers except the first one to be system bus width (128-bit) aligned.	Use 16-byte aligned memory addresses for all TRBs.
3	When there are multiple event rings, a deadlock condition between event handler and BMU may occur when the BMU returns the DMA response for one event ring while the event handler requests the BMU to do a DMA for another event ring.	Use a single event ring.
4	The periodic EP scheduler always tries to schedule the EPs that have large intervals (interval equal to or greater than 128 microframes) into different microframes. So it maintains an internal counter and increments for each large interval EP added. When the counter is greater than 128, the scheduler rejects the new EP. So when the hub re-enumerated 128 times, it triggers this condition.	Use a maximum device endpoint interval of value of 7.
5	When processing a transfer TRB and the IOC bit is set, the xHCI generates an event TRB. The transfer length reported in the event TRB is wrong. This issue occurs if the TRBs are activated after receiving a short packet.	Serialize controller commands and do not use transfer length reported by the event TRB.
6	If an application issues a Stop EP command when the FS/LS endpoint behind an HS hub has started the split or has not completed all the splits, the endpoint stops before it completes all the splits. This causes the hub or the endpoint to be unresponsive to tokens when the endpoint runs again later.	Do not issue Stop EP command until split transactions are completed.

7	The core generated wrong event data when generating a transfer event for an Event Data TRB in a Stop EP command. This issue does not affect the systems in which the software does not use Event Data TRBs.	Do not use event data TRB when issuing Stop EP command.
8	The controller sometimes doesn't send Missed Service Error (MSE) events to tell software about isoch TDs that it is unable to execute in the required frame (the controller just ignores these Isoch TDs).	Expect the lack of MSE events.
9	If the link fails and enters the SS_INACTIVE state, the port status bit PE is not cleared.	Ignore port enabled status when in SS.Inactive state.
10	The host controller may not halt properly if the driver clears the Run/Stop bit of the USBCMD register to halt the host controller less than 125us for SS/HS or 1ms for FS/LS after a control transfer.	After a control transfer is completed, software waits at least 2ms before it tries to halt the host controller
11	Default transaction timeout of 32us may cause certain devices to hang if RxFIFO over-runs and packet is retried.	Increase transaction timeout to 200us: Set GUCTL register (BAR0 + 0xC12C) to 0x0002403F every time after the host controller is reset.
12	Maximum read transfer speed is not optimal.	Increase Rx Threshold: Set Rx Threshold register (BAR0 + 0xC10C) to 0x28400000 every time after the host controller is reset.
13	If software sets up an Event Ring with three or more segments, it is possible that the host core can halt.	Reduce the number of segments of the Event Ring to a maximum of two.
14	Host controller does not support 16-byte aligned stream contexts.	Use 64-byte aligned stream contexts.

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