EVM User's Guide: ISO6521REUEVM ISO6521

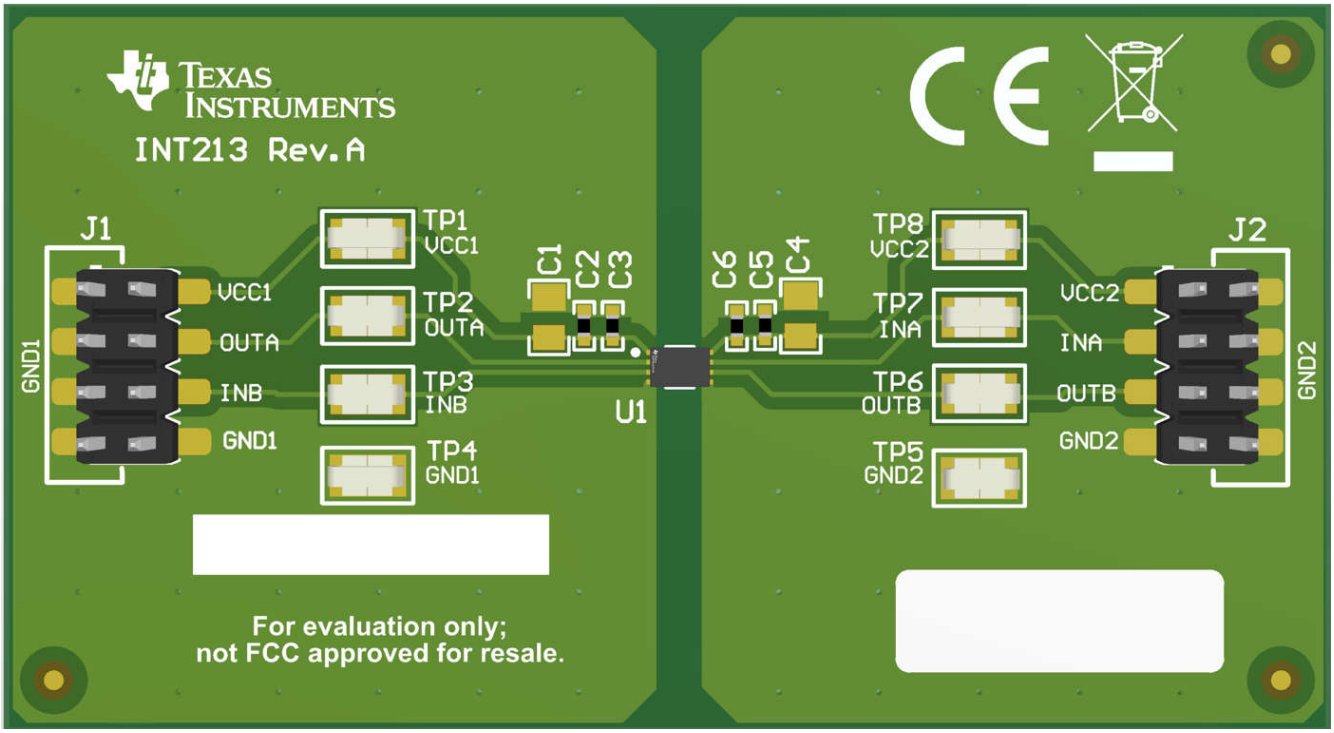
ISO6521 Dual-Channel Functional Isolator Evaluation Module

Description

ISO6521REUEVM is an evaluation module (EVM) used to evaluate the ISO6521 functional isolator in the 8-pin DFN package. The EVM features multiple test points and connection options to evaluate the device with minimal external components. Additionally, the inclusion of different bypass capacitor footprints on the power supply pins allows for multiple configurations to be evaluated.

Features

- 1.71 V to 1.89 V and 2.25 V to 5.5 V supply voltage range
- Low current consumption
- Power supply bypass capacitors
- Test points and connection pins



ISO6521REUEVM (Top View)

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1 Evaluation Module Overview

1.1 Introduction

CAUTION

This evaluation module is made available for evaluation of isolator parameter performance only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the recommended operating range.

This user's guide describes evaluation module (EVM) operation with respect to the ISO6521 dual-channel functional isolator. This guide also describes the EVM schematic and a typical laboratory setup for evaluation. A typical input and output waveform for the ISO6521 is also presented.

1.2 Kit Contents

This evaluation module contains one PCB evaluation board containing one ISO6521 device. The major components of the ISO6521 evaluation module are:

- ISO6521 isolator
- On-board test points and connections for each device pin
- Power supply bypass capacitors

To demonstrate functionality of the ISO6521, TI recommends the following (not included):

- DC power supply
- Oscilloscope
- Signal Generator

1.3 Specification

The ISO6521 is TI's new high performance, dual-channel digital isolator capable of functional isolation. These devices are designed to provide functional isolation for CMOS and LVCMOS digital I/O signals. The ISO6521 is also designed to operate with high electromagnetic immunity and low emissions at a low power consumption. When used, this isolator is an excellent choice for cost sensitive, space constrained designs that require isolation for non-safety applications.

1.4 Device Information

The evaluation module contains one ISO6521, a series of different connections and test points to help evaluate the device, and a small network of power supply bypass capacitors. All of the items previously listed are recommended for proper evaluation of the ISO6521. If necessary, any of the previously listed EVM components can be removed, added, or replaced to modify the evaluation conditions of the device.

For a full list of components included in the ISO6521 Evaluation Module, please see the Table 3-1.

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2 Hardware

2.1 Pin Configuration of the ISO6521 Device

Figure 2-1 shows the pin configuration for the ISO6521.

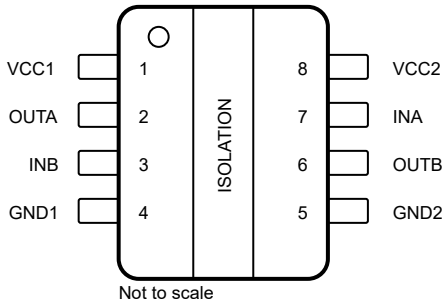

Figure 2-1. ISO6521 Functional Isolator Pin Configuration

2.2 EVM Board Block Diagram and Image

Figure 2-2 shows the top view of the EVM PCB.

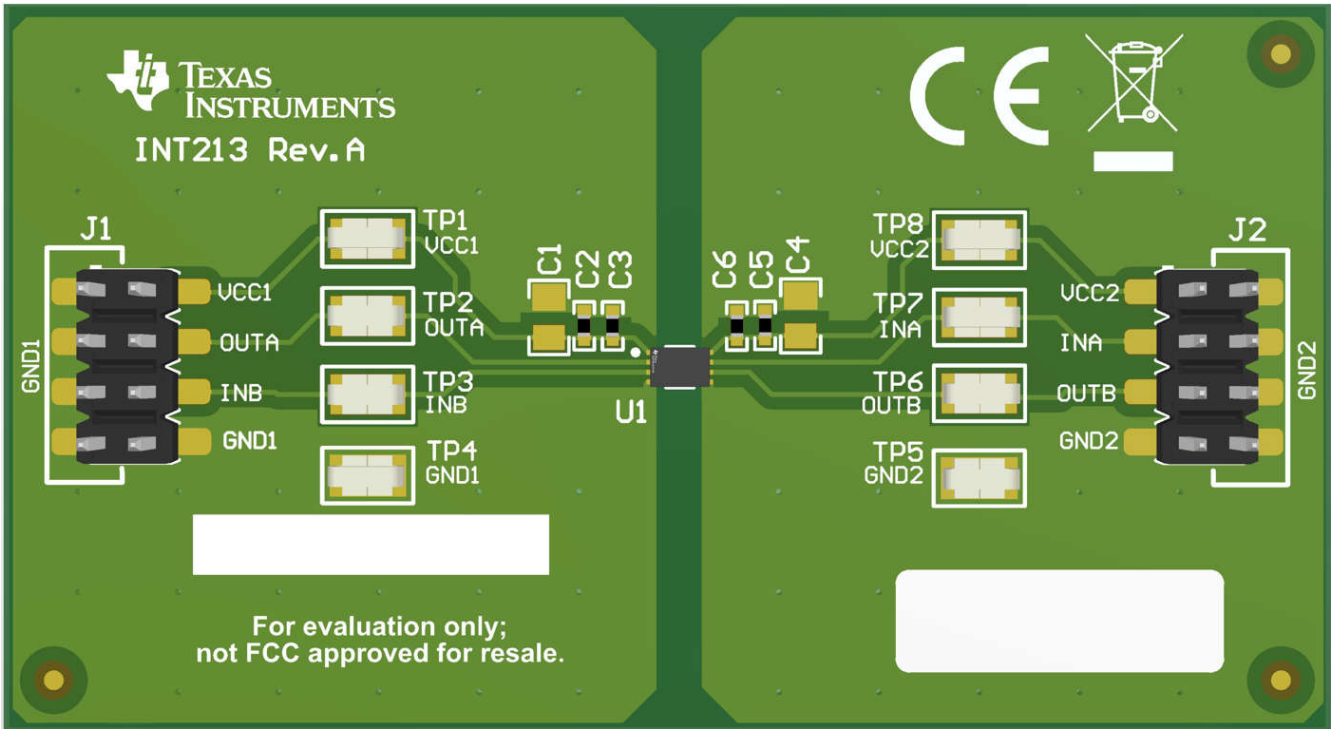

Figure 2-2. ISO6521REUEVM 3D Diagram

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2.3 EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 2-3 shows the configuration for operating the ISO6521 dual-channel functional isolator EVM using two power supplies.

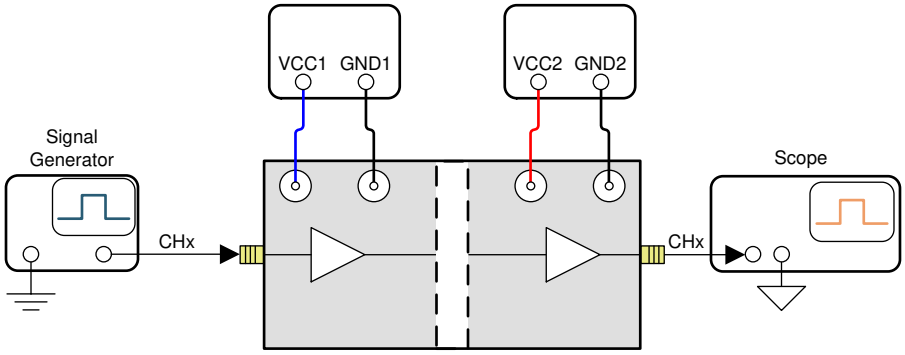

Figure 2-3. Basic EVM Operation

Figure 2-4 shows typical input and output waveforms of the EVM for a 1-MHz clock. The input is shown as channel 1, and the output is shown as channel 2.

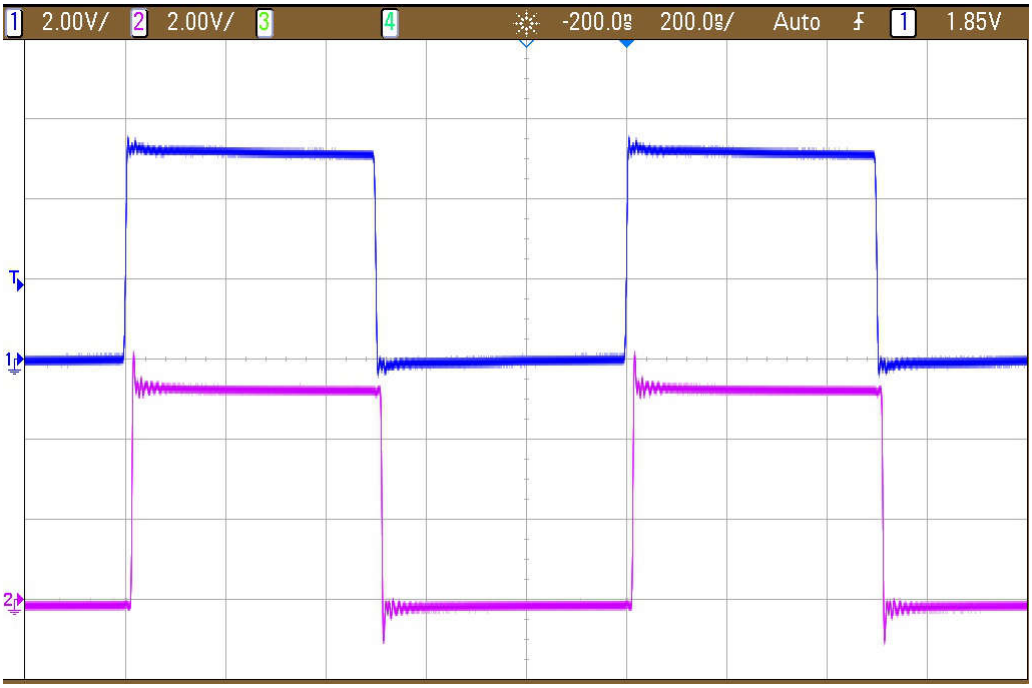

Figure 2-4. Typical Input and Output Waveform

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3 Hardware Design Files

3.1 Schematics

Figure 3-1 shows the ISO6521 EVM schematic.

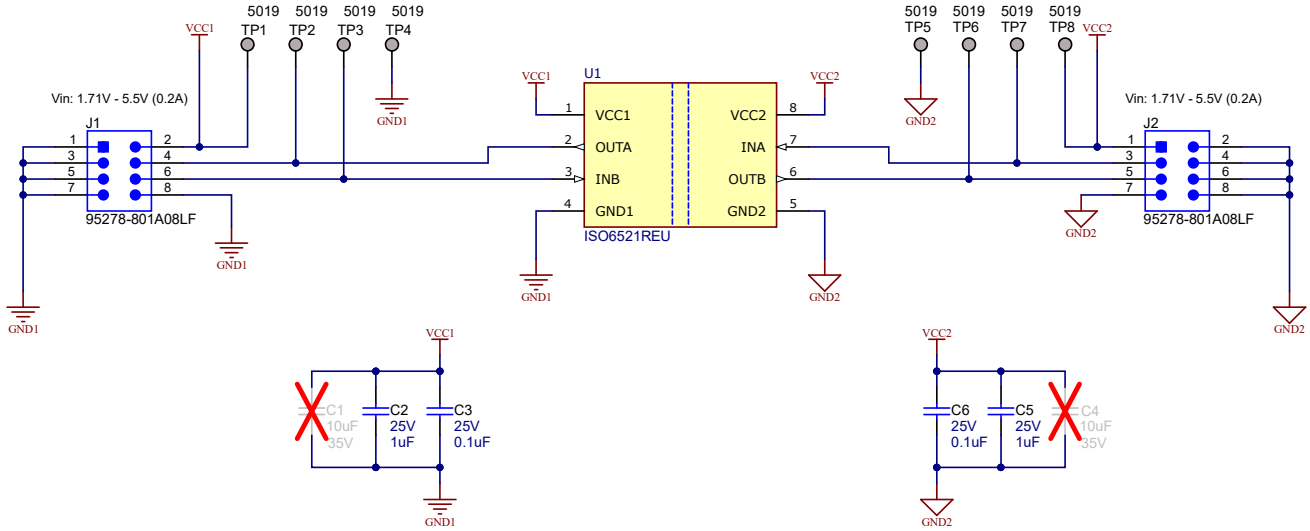

Figure 3-1. ISO6521REUEVM Schematic

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3.2 PCB Layouts

Figure 3-2 and Figure 3-4 shows the top and bottom views of the PCB layout of the EVM. Figure 3-3 shows the top layer of the EVM.

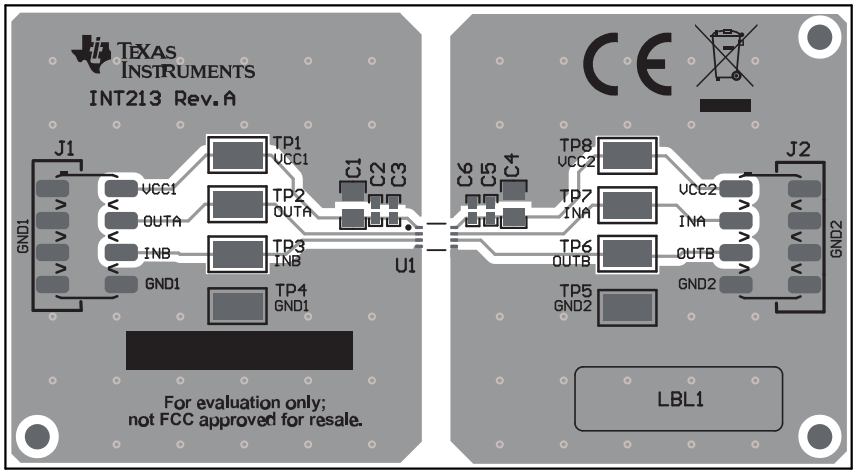

Figure 3-2. ISO6521REUEVM PCB Layout - Composite Top View

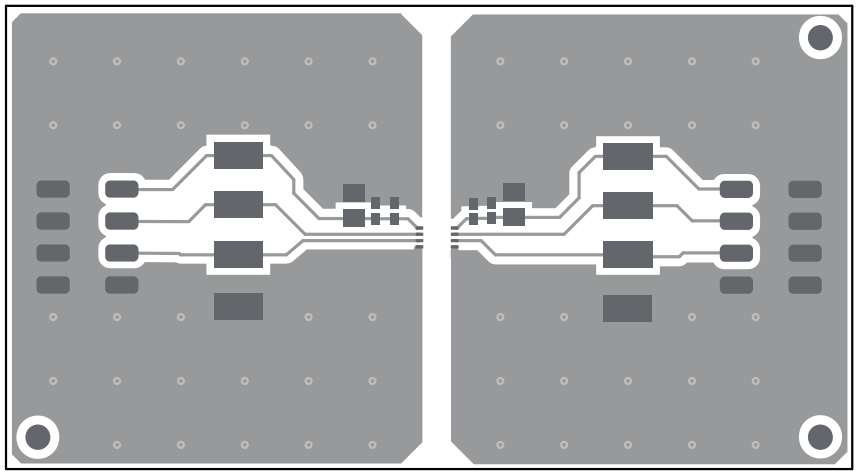

Figure 3-3. ISO6521REUEVM PCB Layout - Top Layer

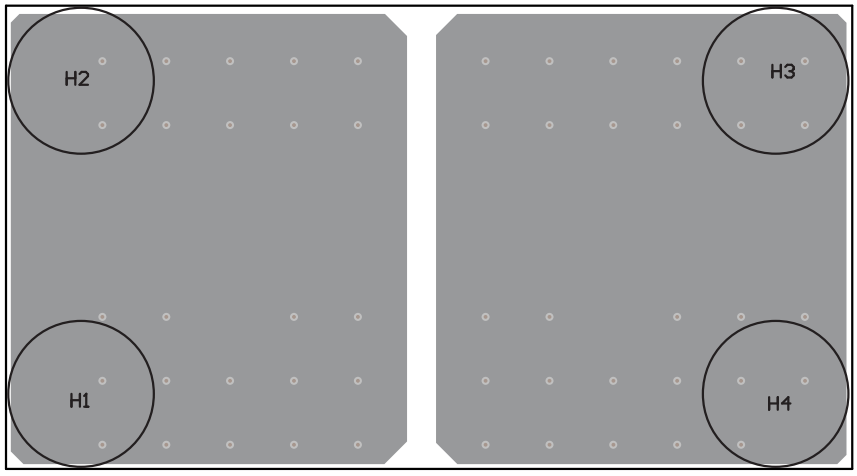

Figure 3-4. ISO6521REUEVM PCB Layout - Composite Bottom View

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3.3 Bill of Materials

Table 3-1 shows the bill of materials (BOM) for this EVM.

Table 3-1. Bill of Materials

Item	Designator	Description	Manufacturer	Part Number	Quantity
1	C2, C5	CAP, CERM, 1 uF, 25 V, +/- 10%, X5R, 0402	MuRata	GRM155R61E105KA12D	2
2	C3, C6	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402	MuRata	GRM155R71E104KE14D	2
3	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	4
5	J1, J2	Header, 2.54mm, 4x2, Gold, SMT	FCI	95278-801A08LF	2
6	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Test Point, Miniature, SMT	Keystone	5019	8
7	U1	General Purpose Dual-Channel Functional Isolators	Texas Instruments	ISO6521REU	1
8	C1, C4	CAP, CERM, 10 uF, 35 V, +/- 10%, X5R, 0805	MuRata	GRM21BR6YA106KE43L	0

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