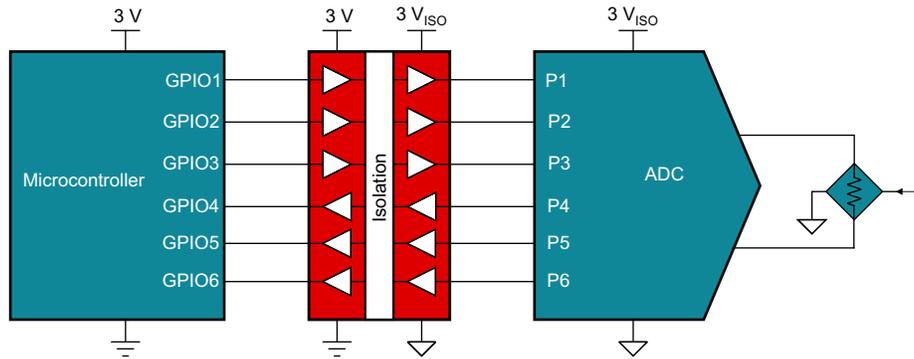


Product Overview

Isolating GPIO Signals



Example GPIO Isolation Block Diagram

Design Considerations

- Prevents DC and unwanted AC currents between controller devices and peripheral ICs
- Allows signal and power transfer between controller devices and peripheral ICs
- Protects low voltage parts in a system from high voltage circuits
- Diminishes the effect of ground potential difference
- [\[FAQ\] What is the difference between basic and reinforced digital isolators?](#)
- [\[FAQ\] Can unused channel pins on a digital isolator be left floating?](#)
- [Digital Isolator Design Guide](#)
- [Top Design Questions About Digital Isolators](#)
- Need additional assistance? Ask our engineers a question on the [TI E2E™ Isolation Support Forum](#)

Recommended Parts

Part Number	AEC-Q100	Channel Count	Voltage Range	Data Rate	Features
ISO67xx	✓	2-6	1.71 - 5.5 V	50 Mbps	High CMTI Reinforced and basic isolation General purpose
ISO77xx	✓	1-6	2.25 - 5.5 V	100 Mbps	High CMTI Reinforced and basic isolation High-speed
ISO70xx	✓	2,4	1.71 - 5.5 V	4 Mbps	Ultra-low power
ISOW77xx				100 Mbps	Digital isolator with integrated power Low-emissions
ISO78xx		1-4	2.25 - 5.5 V		Extra-wide creepage and clearance package

For more devices, browse through the [online parametric tool](#) where you can sort by desired voltage, channel numbers, and other features.

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