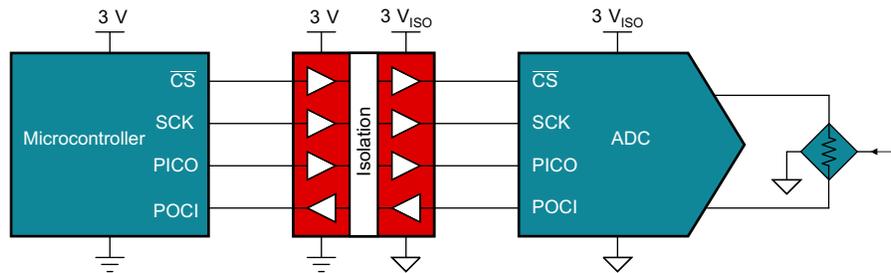


Product Overview

Isolating SPI Signals



Example SPI Isolation Block Diagram

Design Considerations

- Prevents DC and unwanted AC currents between controller devices and peripheral ICs
- Allows signal and power transfer between controller devices and peripheral ICs
- Protects low voltage parts in a system from high voltage circuits
- Diminishes the effect of ground potential difference
- [\[FAQ\] How to connect SPI MCU to multiple isolated SPI nodes?](#)
- [\[FAQ\] How to calculate the maximum SPI speed supported by a digital isolator?](#)
- [Digital Isolator Design Guide](#)
- [Top Design Questions About Digital Isolators](#)
- Need additional assistance? Ask our engineers a question on the [TI E2E™ Isolation Support Forum](#)

Recommended Parts

Part Number	AEC-Q100	Voltage Range	Minimum SPI Clock Frequency Supported at 5 V	Features
ISO6741		1.71 - 5.5 V	13.9 MHz	High CMTI Reinforced and basic isolation General purpose
ISO6741-Q1	✓			
ISO7741		2.25 - 5.5 V	15.6 MHz	High CMTI Reinforced and basic isolation High-speed 30 krad (Si) Total Ionizing Dose (TID) 600 V working voltage Space enhanced plastic
ISO7741-Q1	✓			
ISOS141-SEP				
ISO7041			1.4 MHz	Ultra low power
ISO7041-Q1	✓			
ISOW7741		1.71 - 5.5 V	15.9 MHz	Digital isolator with integrated power Low-emissions
ISO7841		2.25 - 5.5V	15.6 MHz	Extra-wide creepage and clearance package

For more devices, browse through the [online parametric tool](#) where you can sort by desired voltage, channel numbers, and other features.

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