Functional Safety Information

ISOW7742-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the ISOW7742-Q1 (20-DFM package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

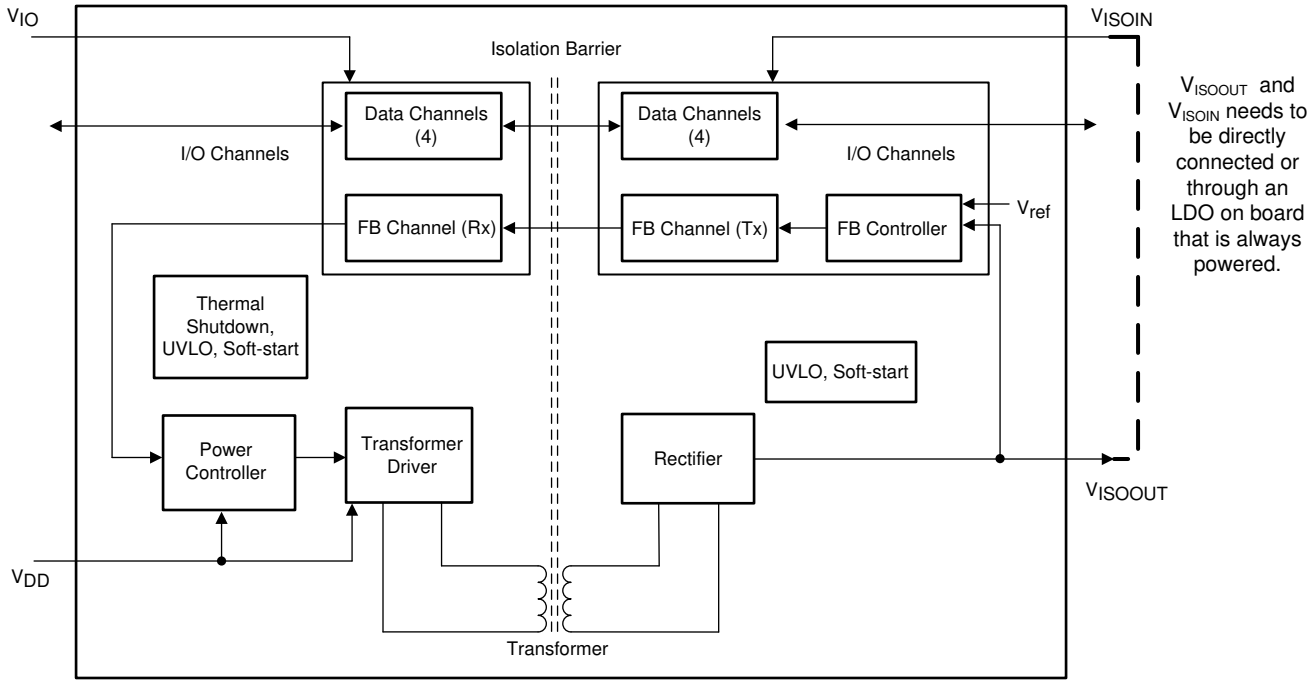

Figure 1-1. Functional Block Diagram

The ISOW7742-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the 20-DFM package of ISOW7742-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	61
Die FIT rate	17
Package FIT rate	44

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1480 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ISOW7742-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Isolated output supply VISO not in voltage or timing specification	50%
Isolated output supply VISO no output	21%
OUT not in timing or voltage specification	12%
OUT stuck to default state	9%
OUT state undetermined	5%
OUT stuck to non default state	1%
OUT stuck high	1%
OUT stuck low	1%

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ISOW7742-Q1 in 20-DFM package. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the ISOW7742-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ISOW7742-Q1 data sheet.

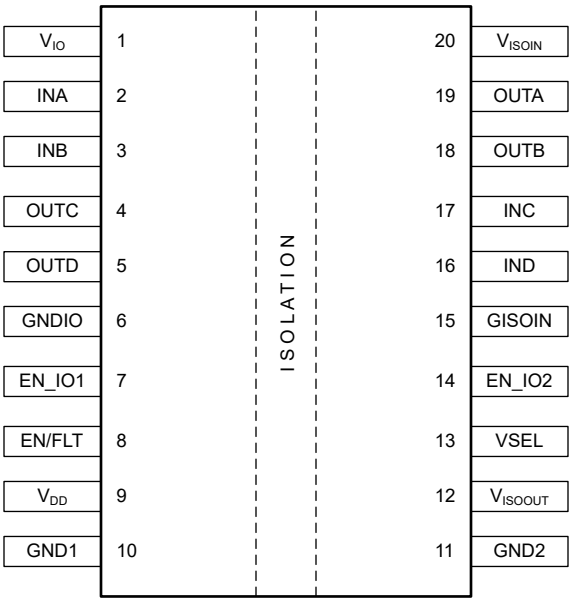

Figure 4-1. Pin Diagram (20-DFM) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIO	1	No power to the IO on side-1. Observe that the absolute maximum ratings for all IO pins of the device are met; otherwise device damage may be plausible. OUTx states undetermined.	A
INA	2	Input signal shorted to ground, so output (OUTA) stuck to low. Communication from INA to OUTA corrupted.	B
INB	3	Input signal shorted to ground, so output (OUTB) stuck to low. Communication from INB to OUTB corrupted.	B
OUTC	4	OUTC stuck low. Data communication from INC to OUTC lost. Device damage possible if INC is driven high for extended period of time.	A
OUTD	5	OUTD stuck low. Data communication from IND to OUTD lost. Device damage possible if IND is driven high for extended period of time.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GNDIO	6	Device continues to function as expected. Normal operation.	D
EN_IO1	7	Side 1 IO enable pin shorted to ground, so INA, INB and INC are disable and OUTD is in a high impedance state.	B
EN/FLT	8	Power converter enable pin shorted to ground, so the integrated DC-DC power converter is disabled	B
VDD	9	No power to side 1 DC-DC converter. Device damage may be plausible if high current flow from the VDD to ground	A
GND1	10	Device continues to function as expected. Normal operation.	D
GND2	11	Device continues to function as expected. Normal operation.	D
VISOOUT	12	Isolated power converter output pin shorted to ground. Device damage may be plausible if high current flow from the VISOOUT to ground	A
VSEL	13	VSEL shorted to ground, so VISOUT is stuck at 3.3V.	B
EN_IO2	14	Side 2 IO enable pin shorted to ground, so IND is disable and OUTA, OUTB and OUTC are in a high impedance state.	C
GISOIN	15	Device continues to function as expected. Normal operation.	D
IND	16	Input signal shorted to ground, so output (OUTD) stuck to low. Communication from IND to OUTD corrupted.	B
INC	17	Input signal shorted to ground, so output (OUTC) stuck to low. Communication from INC to OUTC corrupted.	B
OUTB	18	OUTB stuck low. Data communication from INB to OUTB lost. If INB is driven high, this failure can create short circuit of VISO to GND2.	B
OUTA	19	OUTA stuck low. Data communication from INA to OUTA lost. If INA is driven high, this failure can create short circuit of VISO to GND2.	B
VISOIN	20	Side 2 supply volatge shorted to ground, so no power to side 2. If VISOIN is connected to VISOOUT, device damage may be plausible if high current flow from the VDD to ground	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIO	1	Operation undetermined. Either device is unpowered and OUTx undetermined or through internal ESD diode on INA/INB/INC pin, device can power up if any IN is driven to logic high and has sourcing capability. ESD diode from IN to VCC conducts the regular operating current, hence device damage plausible.	A
INA	2	No communication to INA channel possible. OUTA stuck to default state (High for ISOW7742-Q1 and Low for ISOW7742F-Q1).	B
INB	3	No communication to INB channel possible. OUTB stuck to default state (High for ISOW7742-Q1 and Low for ISOW7742F-Q1).	B
OUTC	4	State of OUTC undetermined. Data communication from INC to OUTC lost.	B
OUTD	5	State of OUTD undetermined. Data communication from IND to OUTD lost.	B
GNDIO	6	No Return ground for IO. IO unpowered on side 1.	B
EN_IO1	7	Side 1 enable pin is open, so OUTD is always enabled.	B
EN/FLT	8	EN/FLT is open, so integrated DC/DC converter state is undefiend	B
VDD	9	No power to the integrated DC/DC converter. VISOOUT is undefined.	B
GND1	10	No Return ground for integrated DC/DC connverter. VISOOUT is undefined.	B
GND2	11	No Return ground for VISOOUT. Side 2 IO has no power.	B
VISOOUT	12	VISOOUT is open, so VISOIN has no power	B
VSEL	13	VSEL is open, so default to VISOOUT 5V	B
EN_IO2	14	Side 2 enable pin is open, so OUTA, OUTB, and OUTC are always enabled.	B
GISOIN	15	No Return ground for VISOIN. No power to the IO.	B
IND	16	No communication to IND channel possible. OUTD stuck to default state (High for ISOW7742-Q1 and Low for ISOW7742F-Q1).	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
INC	17	No communication to INC channel possible. OUTC stuck to default state (High for ISOW7742-Q1 and Low for ISOW7742F-Q1).	B
OUTB	18	State of OUTB undetermined. Data communication from INB to OUTB lost.	B
OUTA	19	State of OUTA undetermined. Data communication from INA to OUTA lost.	B
VISOIN	20	No power to VISOIN, so IO has no power.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VIO	1	INA	If INA is low, No power to the device on side-1. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage may be plausible.	A
INA	2	INB	ommunication corrupted for either INA or INB channel.	B
INB	3	OUTC	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTC	4	OUTD	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTD	5	GNDIO	OUTD shorted to ground. High current can flow between OUTD and ground and cause possible device damage.	A
GNDIO	6	EN_IO1	Disables OUTD output buffer. Communication for channel D corrupted.	B
EN_IO1	7	EN/FLT	IO and integrated DC/DC conveter are enabled or disabled simultaneously.	B
EN/FLT	8	VDD	Integrated DC/DC converter is always enabled	B
VDD	9	GND1	High current can flow between DC/DC converter supply and ground and cause possible device damage.	A
GND1	10	VDD	Already considered in above row.	A
GND2	11	VISOOUT	Integrated DC/DC converter output shorted to ground, so high current can flow between DC/DC converter output and ground and cause possible device damage.	A
VISOOUT	12	VSEL	If VSEL is logic low, high current can flow between VISOOUT and VSEL and cause possible device damage.	A
VSEL	13	EN_IO2	VSEL and EN_IO2 are coupled together.	B
EN_IO2	14	GISOIN	Side 2 IO is disabled, so IND is disable and OUTA, OUTB and OUTC are in a high impedance state.	B
GISOIN	15	IND	OUTD is always low.	B
IND	16	INC	Communication corrupted for either IND or INC channel	B
INC	17	OUTB	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTB	18	OUTA	Communication corrupted for either OUTA or OUTB channel. Device damage possible if INA and INB try to drive opposite logic state for extended duration creating a short between supply and ground on side-2.	A
OUTA	19	VISOIN	Side 2 has no power if OUTA is driven low.	B
VISOIN	20	OUTA	Already considered in above row.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIO	1	No effect. Normal operation.	D
INA	2	INA pin stuck high. Communication corrupted. OUTA state high.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
INB	3	INB pin stuck high. Communication corrupted. OUTB state high.	B
OUTC	4	OUTC stuck high. Data communication from INC to OUTC lost. Device damage possible if INC is driven low for extended period of time.	A
OUTD	5	OUTD stuck high. Data communication from INC to OUTC lost. Device damage possible if IND is driven low for extended period of time causing a short between supply and ground on side-1	A
GNDIO	6	This will create supply to ground short on PCB causing the device to turn off.	B
EN_IO1	7	Functionality to disable output buffer OUTD lost. Communication for all channels normal.	B
EN/FLT	8	Functionality to disable integrated DC/DC converter lost.	B
VDD	9	No effect. Normal operation.	D
GND1	10	This will create supply to ground short on PCB causing the device to turn off.	B
GND2	11	This will cause VISOOUT to ground short making the device go in short circuit protection mode.	B
VISOOUT	12	Device continues to function as expected. Normal operation.	D
VSEL	13	This will cause VISOOUT to default at 5V	B
EN_IO2	14	Functionality to disable output buffer OUTD lost. Communication for all channels normal.	B
GISOIN	15	No effect. Normal operation.	D
IND	16	IND pin stuck high. Communication corrupted. OUTD state high.	B
INC	17	INC pin stuck high. Communication corrupted. OUTC state high.	B
OUTB	18	OUTB stuck high. Communication disrupted. If INB is low for extended duration, OUTB being stuck high creates a short and can cause device go to short circuit protection mechanism.	B
OUTA	19	OUTA stuck high. Communication disrupted. If INA is low for extended duration, OUTA being stuck high creates a short and can cause device go to short circuit protection mechanism.	B
VISOIN	20	Device continues to function as expected. Normal operation.	D

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