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# SN65HVD82 Robust RS-485 Transceiver

Technical

Documents

#### Features 1

- **Bus I/O Protection** 
  - ±16-kV HBM Protection
  - ±12-kV IEC61000-4-2 Contact Discharge
  - +4-kV IEC61000-4-4 Fast Transient Burst
- Industrial Temperature Range –40°C to 85°C
- Large Receiver Hysteresis (60 mV Typical) for Noise Rejection
- Low-Power Consumption
  - <1-µA Standby Current</li>
  - <1-mA Quiescent Current</li>
- Signaling Rate Optimized for 250 kbps
- Create a Custom Design Using the SN65HVD82 With the WEBENCH<sup>®</sup> Power Designer

# 2 Applications

- **Electrical Meters** •
- **Building Automation**
- Industrial Networks
- Security Electronics

# **3** Description

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This device has robust drivers and receivers for demanding industrial applications. The bus pins are robust to ESD events, with high levels of protection to Human-Body Model, Air-Gap Discharge, and Contact Discharge specifications.

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The device combines a differential driver and a differential receiver, which operate from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. The device features a wide commonmode voltage range making the device suitable for multi-point applications over long cable runs. The device is characterized from -40°C to 85°C.

## Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD82	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.





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# Changes from Revision A (July 2015) to Revision B Page Added WEBENCH links to data sheet ...... 1

### Changes from Original (October 2012) to Revision A

Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device 

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# 5 Pin Configuration and Functions



#### **Pin Functions**

PIN		TYDE	DESCRIPTION	
NAME	NO.	ITPE	DESCRIPTION	
A	6	Bus input/output	Driver output or receiver input (complementary to B)	
В	7	Bus input/output	Driver output or receiver input (complementary to A)	
D	4	Digital input	Driver data input	
DE	3	Digital input	Driver enable, active high	
GND	5	Reference potential	Local device ground	
R	1	Digital output	Receive data output	
RE	2	Digital input	Receiver enable, active low	
V <sub>CC</sub>	8	Supply	4.5-V to 5.5-V supply	

# **6** Specifications

# 6.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	-0.5	7	V
	Voltage range at A or B Inputs	-18	18	V
	Input voltage range at any logic pin	-0.3	5.7	V
	Voltage input range, transient pulse, A and B, through $100\Omega$	-100	100	V
	Receiver output current	-24	24	mA
TJ	Junction temperature		170	°C
	Continuous total power dissipation	See Therma	I Information	
$T_{STG}$	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 6.2 ESD Ratings

				VALUE	UNIT	
V <sub>(ESD)</sub> Electrostatic discharge		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	)1 <sup>(1)</sup>	±4000		
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>				
	Electrostatic	Machine model (MM), JEDEC Standard 22		±400	V	
	discharge	IEC 61000-4-2 ESD (Contact Discharge)	harge) Bus terminals and GND ±	±12000	v	
		IEC 60749-26 ESD (Human Body Model) Bus terminals and	Bus terminals and GND	±16000		
		IEC 61000-4-4 EMC (Fast Transient Burst Immunity)	Bus terminals and GND	±4000		

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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# 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
VI	Input voltage at any bus terminal (separately or common mode) <sup>(1)</sup>	-7		12	V
VIH	High-level input voltage (D, DE and RE inputs)	2		$V_{CC}$	V
VIL	Low-level input voltage (D, DE and RE inputs)	0		0.8	V
$V_{ID}$	Differential input voltage (A and B inputs)	-12		12	V
	Output current, Driver	-60		60	mA
<b>ю</b>	Output current, Receiver	-8		8	mA
RL	Differential load resistance	54	60		Ω
CL	Differential load capacitance		50		pF
1/t <sub>UI</sub>	Signaling rate			250	kbps
T <sub>A</sub>	Operating free-air temperature (see <i>Application and Implementation</i> section for thermal information)	-40		85	°C
TJ	Junction Temperature	-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

# 6.4 Thermal Information

		SN65HVD82	
	THERMAL METRIC <sup>(1)</sup>	D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	60.8	°C/W
$R_{ heta JB}$	Junction-to-board thermal resistance	57.1	°C/W
ΨJT	Junction-to-top characterization parameter	13.9	°C/W
Ψјв	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

# 6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
		See Figure 5, $R_L = 60 \Omega$ , 375 $\Omega$ on	each output to -7 V to 12 V	1.5			V
V <sub>OD</sub>	Driver differential output voltage	R <sub>L</sub> = 54 Ω (RS-485)		1.5	2		V
magnitude		R <sub>L</sub> = 100 Ω (RS-422)	- See Figure 6	2	2.5		V
$\Delta  V_{OD} $	Change in magnitude of driver differential output voltage	$R_L = 54 \ \Omega, \ C_L = 50 \ pF$	See Figure 6	-0.2	0	0.2	V
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage	Center of two 27-Ω load resistors See Figure 6		1	V <sub>CC</sub> /2	3	V
$\Delta V_{OC}$	Change in differential driver output common-mode voltage			-0.2	0	0.2	V
V <sub>OC(PP)</sub>	Peak-to-peak driver common-mode output voltage				850		mV
C <sub>OD</sub>	Differential output capacitance				8		pF
V <sub>IT+</sub>	Positive-going receiver differential input voltage threshold			See (1)	-70	-20	mV
V <sub>IT-</sub>	Negative-going receiver differential input voltage threshold			-200	-150	See (1)	mV
V <sub>HYS</sub>	Receiver differential input voltage threshold hysteresis (V <sub>IT+</sub> – V <sub>IT</sub> –)			40	60		mV
V <sub>OH</sub>	Receiver high-level output voltage	I <sub>OH</sub> = -8 mA		4	V <sub>CC</sub> -0.3		V
V <sub>OL</sub>	Receiver low-level output voltage	I <sub>OL</sub> = 8 mA			0.2	0.4	V
I <sub>I</sub>	Driver input, driver enable, and receiver enable input current			-2		2	μΑ
I <sub>OZ</sub>	Receiver output high-impedance current	$V_0 = 0 V \text{ or } V_{CC}, \overline{RE} \text{ at } V_{CC}$		-10		10	μA
I <sub>OS</sub>	Driver short-circuit output current	$\mid I_{OS} \mid$ with $V_A$ or $V_B$ from –7 V to +1	2 V			150	mA
	Due input surrent (dischlad driver)	$V_{CC} = 4.5$ to 5.5 V or $V_{CC} = 0$ V,	V <sub>I</sub> = 12 V		75	125	
1	Bus input current (disabled driver)	DE at 0 V	$V_1 = -7 V$	-100	-40		μA
		Driver and Receiver enabled	DE = V <sub>CC</sub> , RE=GND, No load			900	
		Driver enabled, receiver disabled	$\label{eq:def} \begin{array}{l} DE=V_{CC}, \ RE=V_{CC},\\ No \ load \end{array}$			650	
I <sub>CC</sub>	Supply current (quiescent)	Driver disabled, receiver enabled	DE = GND, RE = GND, No load			650	μΑ
		Driver and receiver disabled			0.4	2	
	Supply current (dynamic)	See Typical Characteristics					

(1) Under any specific conditions,  $V_{\text{IT+}}$  is assured to be at least  $V_{\text{HYS}}$  higher than  $V_{\text{IT-}}.$ 

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### 6.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t <sub>r</sub> , t <sub>f</sub>	Driver differential output rise/fall time			400	700	1200	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Driver propagation delay	$R_{L} = 54 \Omega, C_{L} = 50$	) pF, See Figure 7	90	700	1000	ns
t <sub>SK(P)</sub>	Driver pulse skew,  t <sub>PHL</sub> – t <sub>PLH</sub>				25	200	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Driver disable time				50	500	ns
	Driver enable time	Receiver enabled	See Figure 8 and Figure 9		500	1000	ns
<sup>I</sup> PZH <sup>,</sup> <sup>I</sup> PZL	Driver enable time	Receiver disabled			3	9	μS
RECEIVER							
t <sub>r</sub> , t <sub>f</sub>	Receiver output rise/fall time	C <sub>L</sub> = 15 pF, See Figure 10			18	30	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Receiver propagation delay time				85	195	ns
t <sub>SK(P)</sub>	Receiver pulse skew,  t <sub>PHL</sub> – t <sub>PLH</sub>				1	15	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Receiver disable time				50	500	ns
$t_{PZL(1)}, t_{PZH(1)}$	Dessiver enable time	Driver enabled, Se	e Figure 11		20	130	ns
t <sub>PZL(2)</sub> , t <sub>PZH(2)</sub>		Driver disabled, Se	ee Figure 12		2	8	μS

# 6.7 Typical Characteristics





# 7 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.















D at 3V to test non-inverting output, D at 0V to test inverting output.

## Figure 8. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

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# Parameter Measurement Information (continued)



D at 0V to test non-inverting output, D at 3V to test inverting output.

## Figure 9. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load









8



 $V_{CC}$ A 0 V or 1.5 V - $R V_0$  $1 \text{ k}\Omega \pm 1\%$ 6 Л S1  $\Lambda \Lambda \Lambda$  $\cap$ В  $\overline{c}$  $C_L$  = 15 pF ±20% 1.5 V or 0 V RF C<sub>L</sub> Includes Fixture and Instrumentation Capacitance Input  $\leq 50 \Omega$ ν<sub>ι</sub> Generator h d- 3 V  $V_{I}$ 50% 0 V t<sub>PZH(2)</sub> →  $V_{\rm OH}$ A at 1.5 V Vo 50% B at 0 V S1 to GND GND t<sub>PZL(2)</sub>  $V_{CC}$ A at 0 V Vo B at 1.5 V 50% S1 to V<sub>CC</sub>  $\rm V_{OL}$ S0308-01

# **Parameter Measurement Information (continued)**

Figure 12. Measurement of Receiver Enable Times With Driver Disabled



# 8 Detailed Description

# 8.1 Overview

The SN65HVD82 device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 250 kbps over controlled-impedance transmission media (such as twisted-pair cabling). The device features a high level of internal transient protection, making it able to withstand up ESD strikes up to 12 kV (per IEC 61000-4-2) and EFT transients up to 4 kV (per IEC 61000-4-4) without incurring damage. Up to 256 units of SN65HVD82 may share a common RS-485 bus due to the device's low bus input currents. The device also features a low standby current consumption of 400 nA (typical).

# 8.2 Functional Block Diagram



Figure 13. Logic Diagram (Positive Logic)

# 8.3 Feature Description

## 8.3.1 Receiver Failsafe

The differential receiver is *failsafe* to invalid bus states caused by:

- open bus conditions such as a disconnected connector
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the "input indeterminate" range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input  $V_{ID}$  is more positive than 200 mV, and must output a Low when the  $V_{ID}$  is more negative than -200 mV. The receiver parameters which determine the failsafe performance are  $V_{IT+}$  and  $V_{HYS}$ . As seen in the Electrical Characteristics table, differential signals more negative than

-200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the  $V_{IT+}$  threshold, and the receiver output will be High. Only when the differential input is more negative than  $V_{IT-}$  will the receiver output transition to a Low state. So the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value  $V_{HYS}$  (the separation between  $V_{IT+}$  and  $V_{IT-}$ ) as well as the value of  $V_{IT+}$ .

Signals which transition from positive to negative (or from negative to positive) will transition only once, ensuring no spurious bits.

# 8.3.2 Low-Power Standby Mode

When both the driver and receiver are disabled (DE transitions to a low state and RE transitions to a high state) the device enters standby mode. If the enable inputs are in this state for a brief time (e.g. less than 100 ns), the device does not enter standby mode. This prevents inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state a sufficient duration (e.g. for 300 ns or more), the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the steady-state supply current is typically less than 400 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.



# 8.4 Device Functional Modes

INPUT	ENABLE	OUTPUTS		
D	DE	А	В	
Н	Н	Н	L	Actively drive bus High
L	Н	L	н	Actively drive bus Low
Х	L	Z	Z	Driver disabled
Х	OPEN	Z	Z	Driver disabled by default
OPEN	Н	Н	L	Actively drive bus High by default

## Table 1. Driver Function Table

# Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	Н	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
Х	Н	Z	Receiver disabled
Х	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	Н	Fail-safe high output
Short-circuit bus	L	Н	Fail-safe high output
Idle (terminated) bus	L	Н	Fail-safe high output





Figure 14. Equivalent Input and Output Schematic Diagrams



# 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

## 9.1.1 Device Configuration

The SN65HVD82 is a half-duplex, 250-kbps, RS-485 transceiver operating from a single 5-V supply. The driver and receiver enable pins allow for the configuration of different operating modes.



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Figure 15. SN65HVD82 Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single, direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver-enable to ground and controlling only the driver-enable input, also uses one control line only. In this configuration a node not only receives the data from the bus, but also the data it sends and thus can verify that the correct data have been transmitted.

### 9.1.2 Bus – Design

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R_T$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

# Application Information (continued)



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Figure 16. Typical RS-485 Network with SN65HVD82 Transceivers

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with  $Z_0 = 100 \Omega$ , and proper RS-485 cable with  $Z_0 = 120 \Omega$ .

Line measurements have shown that making  $R_T$  by up to 10% larger than  $Z_0$  improves signal quality. Typical cable sizes are AWG 22 and AWG 24.

The theoretical maximum bus length is assumed with 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB.

The theoretical maximum number of bus nodes is determined by the ratio of the RS-485 specified maximum of 32 unit loads (UL) and the actual unit load of the applied transceiver. For example, the SN65HVD82 is a 1/8 UL transceiver. Dividing 32 UL by 1/8 UL yields 256 transceivers that can be connected to one bus.

### 9.1.3 Cable-Length Versus Data Rate

There is an inverse relationship between data rate and cable length. That is, the higher the data rate the shorter the cable and conversely the lower the data rate the longer the cable. While most RS-485 systems utilize data rates between 10 kbps and 100 kbps, applications such as e-metering often operate at rates of up to 250 kbps even at distances of 4000 feet and above. This is possible by allowing for small signal jitter of up to 5 or 10%.



Figure 17. Cable Length vs Data Rate Characteristic



# **Application Information (continued)**

### 9.1.4 Stub – Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for this is that a stub presents a non-terminated piece of bus line which can introduce reflections if too long. As a rule of thumb the electrical length or round-trip delay of a stub should be less than one tenth of the driver's rise time, thus leading to a maximum physical stub length of:  $L_{Stub} \le 0.1 \times t_r \times v \times c$ , with  $t_r$  as the driver's 10/90 rise time, **c** as the speed of light (3 × 10<sup>8</sup> m/s or 9.8 × 10<sup>8</sup> ft/s), and **v** as the signal velocity of the cable (v = 78%) or trace (v = 45%) as a factor of **c**.

Thus, for the SN65HVD82 with a minimum rise time of 400 ns the maximum *cable* stub length yields  $L_{Stub} \le 0.1 \times 400 \times 10^{-9} \times 3 \times 10^8 \times 0.78 = 9.4$  m or 30.6 ft.



Figure 18. Stub Length

### 9.1.5 3-V to 5-V Interface

Interfacing the SN65HVD82 to a 3-V controller is easy. Because the 5-V logic inputs of the transceiver accept 3-V input signals they can be directly connected to the controller I/O. The 5-V receiver output, R, however must be level-shifted via a Schottky diode and a 10-kV resistor to connect to the controller input. When R is high, the diode is reverse biased and the controller supply potential lies at the controller input. When R is low, the diode is forward biased and conducts. In this case only the diode forward voltage of 0.2 V lies at the controller input.



Figure 19. 3 V – 5 V Interface

#### 9.1.6 Noise Immunity

The input sensitivity of a standard RS-485 transceiver is  $\pm 200 \text{ mV}$ . When the differential input voltage, V<sub>ID</sub>, is greater than  $\pm 200 \text{ mV}$ , the receiver output turns high, for V<sub>ID</sub>  $\leq 200 \text{ mV}$  the receiver outputs low. Bus voltages in between these levels can cause the receiver output to go high, or low, or even toggle between logic states. Small bus voltages however occur every time during the bus access hand-off from one driver to the next as the low-impedance termination resistors reduce the bus voltage to zero. To prevent receiver output toggling during bus idling, and thus increasing noise immunity, external bias resistors must be applied to create a bus voltage that is greater than the input sensitivity plus any expected differential noise.

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# **Application Information (continued)**



Figure 20. SN65HVD82 Noise Immunity

The SN65HVD82 transceiver circumvents idle-bus and differential noise issues by providing a positive input threshold of -20 mV and a typical hysteresis of 60 mV. In the case of an idle-bus condition therefore, a differential noise voltage of up to 160 mV<sub>PP</sub> can be present without causing the receiver output to change states from high to low. This increased noise immunity eliminates the need for idle-bus failsafe bias resistors and allows for long haul data transmissions in noisy environment.

### 9.1.7 Transient Protection

The bus terminals of the SN65HVD82 transceiver family possess on-chip ESD protection against ±15 kV human body model (HBM) and ±12 kV IEC61000-4-2 contact discharge. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, CS, and 78% lower discharge resistance, RD of the IEC-model produce significantly higher discharge currents than the HBM-model.



Figure 21. HBM and IEC-ESD Models and Currents in Comparison

EFTs are usually caused by relay contact bounce or the interruption of inductive loads, while surge transients often results from lightning strikes (direct strike or induced voltages and currents due to an indirect strike), or the switching of power systems including load changes and short circuits switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.



## **Application Information (continued)**

Figure 22 compares the pulse-power of the EFT and surge transients with the power caused by an IEC-ESD transient. As can be seen the tiny blue blip in the bottom left corner of the left diagram represents the power of a 10-kV ESD transient, which already dwarfs against the significantly higher EFT power spike and certainly against the 500-V surge transient. This type of transient power is well representative for factory environments in industrial and process automation. The right diagram compares the enormous power of a 6-kV surge transient, which more likely occurs in e-metering applications of power generating and power grid systems, with the aforementioned 500-V surge transient. Note that the unit of the pulse-power changes from kW to MW, thus making the power of the 500-V surge transient almost dropping off the scale.



Figure 22. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, their long pulse duration and slowly decreasing pulse power signifies high energy content.

The electrical energy of a transient that is dumped onto the transceiver's internal protections cells is converted into thermal energy, or heat that literally fries the protection cells, thus destroying the transceiver. Figure 23 showcases the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

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# Application Information (continued)





Figure 24 suggests two circuit designs providing protection against surge transients. Table 3 presents the associated bill of material.

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3V, 250kbps RS-485 Transceiver	SN65HVD82D	ТІ
R1,R2	10 $\Omega$ , Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1,TBU2	Bidirectional. 200mA Transient Blocking Unit	TBU-CA-065-200-WH	Bourns
MOV1,MOV2	200V, Metal-Oxide Varistor	MOV-10D201K	Bourns

Table 3. Bill of Materials



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Both circuits are designed for 10-kV ESD and 4-kV EFT transient protection. The left however provides surge protection of  $\geq$  500-V transients only, while the right protection circuits can withstand 5-kV surge transients.



# 9.2 Typical Application



Figure 25. Isolated Bus Node With Transient Protection

### 9.2.1 Design Requirements

The following list outlines sample design requirements for the typical application example found in Figure 25

- RS-485-compliant bus interface (needs differential signal amplitude of at least 1.5 V under fully-loaded conditions – essentially, maximum number of nodes connected and with dual 120-Ω termination).
- Galvanic isolation of both signal and power supply lines.
- Able to withstand ESD transients up to 10 kV (per IEC 61000-4-2) and EFTs up to 4 kV (per IEC 61000-4-4).
- Full control of data flow on bus in order to prevent contention (for half-duplex communication).

### 9.2.2 Detailed Design Procedure

### 9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the SN65HVD82 device with the WEBENCH® Power Designer.

- 1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
- 2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
- 3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance



# **Typical Application (continued)**

- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

# 9.2.2.2 Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 25).

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TPS76350

Signal isolation utilizes the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7-k $\Omega$  resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure 24 (left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

R<sub>VH</sub> refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge  $C_{HV}$ , if it is expected that fast transients might charge  $C_{HV}$  to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components,  $C_{HV}$  and  $R_{HV}$ , are connecting to the chassis at the other end.



# 9.2.3 Application Curve

Figure 26. SN65GVD82 D Input (Top), Differential Output (Middle), and R Output (Bottom), 250 kbps Operation, PRBS Data Pattern



# **10** Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

# 11 Layout

# 11.1 Layout Guidelines

## 11.1.1 Design and Layout Considerations For Transient Protection

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

- 1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- 2. Use Vcc and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
- 3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
- 4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the Vcc-pins of transceiver, UART, controller ICs on the board.
- 5. Use at least two vias for Vcc and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- 6. Use  $1-k\Omega$  to  $10-k\Omega$  pullup or pulldown resistors for enable lines to limit noise currents in theses lines during transient events.
- 7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- 8. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to some 200 mA.

# 11.2 Layout Example







# **12 Device and Documentation Support**

# 12.1 Device Support

## 12.1.1 Third-Party Products Disclaimer

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# 12.1.2 Custom Design With WEBENCH® Tools

Click here to create a custom design using the SN65HVD82 device with the WEBENCH® Power Designer.

- 1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
- 2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
- 3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## **12.2 Community Resources**

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E<sup>™</sup> Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

# 12.3 Trademarks

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# 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# 12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.



# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



# **PACKAGING INFORMATION**

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN65HVD82D	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82
SN65HVD82D.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82
SN65HVD82D.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82
SN65HVD82DR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82
SN65HVD82DR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82
SN65HVD82DR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82
SN65HVD82DRG4.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82
SN65HVD82DRG4.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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# TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Davias	Baakaga	Dookoo
*All dimensions are nominal		

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD82DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1



# PACKAGE MATERIALS INFORMATION

23-May-2025



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD82DR	SOIC	D	8	2500	353.0	353.0	32.0

# TEXAS INSTRUMENTS

www.ti.com

23-May-2025

# TUBE



# - B - Alignment groove width

#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
SN65HVD82D	D	SOIC	8	75	507	8	3940	4.32
SN65HVD82D.A	D	SOIC	8	75	507	8	3940	4.32
SN65HVD82D.B	D	SOIC	8	75	507	8	3940	4.32

# D0008A



# **PACKAGE OUTLINE**

# SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



# D0008A

# **EXAMPLE BOARD LAYOUT**

# SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# D0008A

# **EXAMPLE STENCIL DESIGN**

# SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



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