SN65DSI85 MIPI® DSI Bridge to FlatLink™ LVDS Dual Channel DSI to Dual-Link LVDS Bridge

1 Features

- Implements MIPI® D-PHY version 1.00.00 physical layer front-end and display serial interface (DSI) version 1.02.00
- Dual-channel DSI receiver configurable for one, two, three, or four D-PHY data lanes per channel operating up to 1 Gbps per lane
- Supports 18-bpp and 24-bpp DSI video packets with RGB666 and RGB888 formats
- Suitable for 60 fps WQXGA 2560 × 1600 resolution at 18-bpp and 24-bpp color, and WUXGA 1920 × 1200 resolution with 3D graphics at 60 fps (120 fps equivalent)
- MIPI® front-end configurable for single-channel or dual-channel DSI configurations
- FlatLink™ output configurable for single-link or dual-link LVDS
- Supports dual-channel DSI ODD or EVEN and LEFT or RIGHT operating modes
- Supports two single-channel DSI to two single-link LVDS operating mode
- LVDS output clock range of 25 MHz to 154 MHz in dual-link or single-link mode
- LVDS pixel clock may be sourced from free-running continuous D-PHY clock or external reference clock (REFCLK)
- 1.8-V main V_{CC} power supply
- Low-power features include shutdown mode, reduced LVDS output voltage swing, common mode, and MIPI® ultra-low power state (ULPS) support
- LVDS channel swap, LVDS pin order reverse feature for ease of PCB routing
- ESD rating ±2 kV (HBM)
- Packaged in 64-pin 5 mm x 5 mm nFBGA (ZXH)
- Temperature range: –40°C to 85°C

2 Applications

- PC & notebooks
- Tablets
- Connected peripherals & printers

3 Description

The SN65DSI85 DSI to FlatLink bridge features a dual-channel MIPI D-PHY receiver front-end configuration with 4 lanes per channel operating at 1 Gbps per lane; a maximum input bandwidth of 8 Gbps. The bridge decodes MIPI DSI 18-bpp RGB666 and 24-bpp RGB888 packets and converts the formatted video data stream to a FlatLink compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Dual-Link LVDS, Single-Link LVDS, or two Single-Link LVDS interface(s) with four data lanes per link.

The SN65DSI85 is well suited for WQXGA (2560 × 1600) at 60 frames per second, as well as 3D Graphics at WUXGA and True HD (1920 × 1080) resolutions at an equivalent 120 fps with up to 24 bits-per-pixel. Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and LVDS interfaces.

Designed with industry-compliant interface technology, the SN65DSI85 is compatible with a wide range of micro-processors, and is designed with a range of power management features including low-swing LVDS outputs, and the MIPI® defined ultra-low power state (ULPS) support.

The SN65DSI85 is implemented in a small outline 5-mm × 5-mm nFBGA at 0.5-mm pitch package, and operates across a temperature range from –40°C to 85°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65DSI85	nFBGA (64)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (June 2018) to Revision G (October 2020)	Page
• Changed u*jr ZQE to nFBGA ZXH	1
• Changed u*jr ZQE to nFBGA ZXH	4
• Changed u*jr ZQE to nFBGA ZXH. Updated thermal information	7
• Changed u*jr ZQE to nFBGA ZXH	47

Changes from Revision E (August 2015) to Revision F (June 2018)	Page
• Deleted figure *RESET and Initialization Timing Definition While V_{CC} is High*	12
• Changed the paragraph following Figure 7-3	16
• Changed *Recommended Initialization Sequence* To: *Initialization Sequence*	17
• Changed Table 7-5	17
• Changed item 3 in *Video Stop and Restart Sequence* From: Drive all DSI input lanes including DSI CLK lane to LP11. To: Drive all DSI data lanes to LP11, but keep the DSI CLK lanes in HS.	38

Changes from Revision D (September 2013) to Revision E (August 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed item 3 of the ULPS sequence list for clarification.	14
• Changed description of the Init seq 7 - Recommended Initialization Sequence for clarification.	17
• Changed description of Address 0x0A, Bit 7 in Table 7-8, CSR Bit Field Definitions - Reset and Clock Registers	25
• Changed Address 0x18, Bits 3 and 2 Description, Address 0x18, Bit 1 Description, and Address 0x18, Bit 0 Description in Table 7-10 for clarification	25
• Changed Section 8.1.1, step 1 of the STOP sequence from " ...0(CSR 0x0A.7)" to "....0(CSR 0x0D.0)" and step 3 of the Restart sequence from "Wait for the PLL_LOCK bit to be set(CSR 0x0A.7)." to "Wait for a minimum of 3 ms."	38

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Changes from Revision * (August 2012) to Revision A (December 2012) **Page**

- Changed the t_{setup} and t_{hold} NOM value of 1.5 to a MIN value of 1.5 ... 7
- Changed the value of V_{OH} From: 1.3 MIN To: 1.25 MIN ... 8
- Changed the I_{CC} TYP value From: 125 To: 127 and MAX value From: 200 To: 212 ... 8
- Added a TYP value of 7.7 to I_{ULPS} ... 8
- Changed the I_{RST} TYP value From: 0.05 To: 0.04 and MAX value From: 0.2 To: 0.06 ... 8
- changed the values of |VOD| ... 8
- changed the values of |VOD| ... 8
- Changed the values of $V_{OC(SS)}$ for test conditions CSR 0x19.6 = 0 and, or CSR 0x19.4 = 0 ... 8
- Added table note 2 ... 8
- Added table note 3 ... 8
- Changed the SWITCHING CHARACTERISTICS table ... 10
- Changed the description of CHA_LVDS_VOD_SWING ... 25
- Changed the description of CHB_LVDS_VOD_SWING ... 25

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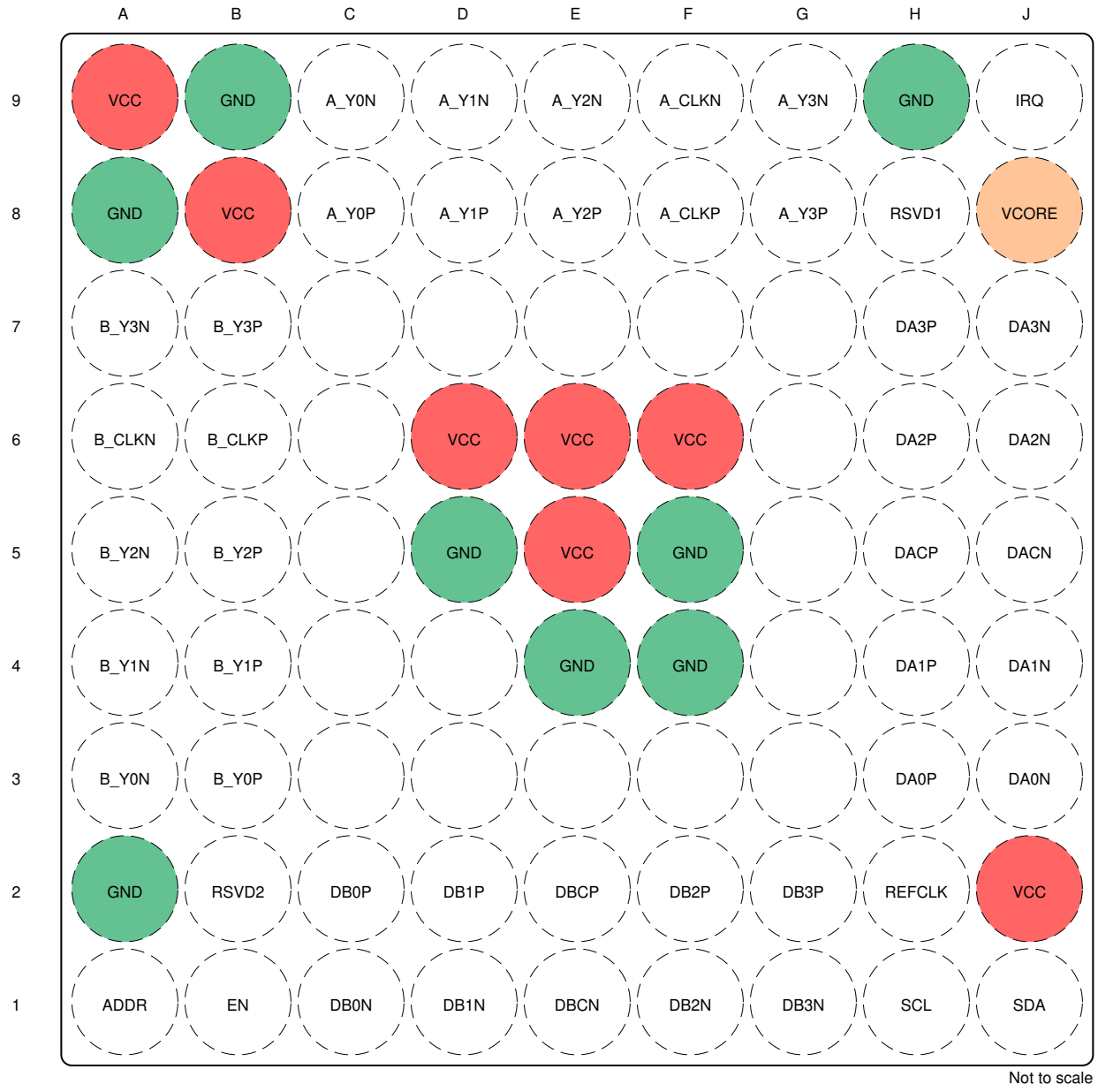
5 Pin Configuration and Functions



Not to scale

To minimize the power supply noise floor, provide good decoupling near the SN65DSI85 power pins. The use of four ceramic capacitors (2x 0.1 µF and 2x 0.01 µF) provides good performance. At the least, it is recommended to install one 0.1 µF and one 0.01 µF capacitor near the SN65DSI85. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized. Placing the capacitor underneath the SN65DSI85 on the bottom of the PCB is often a good choice.

Figure 5-1. ZXH Package 64-Pin nFBGA (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADDR	A1	CMOS Input/Output	Local I^2C Interface Target Address Select. See Table 7-6. In normal operation this pin is an input. When the ADDR pin is programmed high, it should be tied to the same 1.8 V power rails where the SN65DSI85 VCC 1.8 V power rail is connected.
A_Y0N	C9	LVDS Output	FlatLink™ Channel A LVDS Data Output 0.
A_Y0P	C8		

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Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
A_Y1N	D9		FlatLink™ Channel A LVDS Data Output 1.
A_Y1P	D8		
A_Y2N	E9		FlatLink™ Channel A LVDS Data Output 2.
A_Y2P	E8		
A_Y3N	G9		FlatLink™ Channel A LVDS Data Output 3. A_Y3P and A_Y3N shall be left NC for 18 bpp panels.
A_Y3P	G8		
A_CLKN	F9		FlatLink™ Channel A LVDS Clock
A_CLKP	F8		
B_Y0N	A3		FlatLink™ Channel B LVDS Data Output 0.
B_Y0P	B3		
B_Y1N	A4		FlatLink™ Channel B LVDS Data Output 1.
B_Y1P	B4		
B_Y2N	A5		FlatLink™ Channel B LVDS Data Output 2.
B_Y2P	B5		
B_Y3N	A7		FlatLink™ Channel B LVDS Data Output 3. B_Y3P and B_Y3N shall be left NC for 18 bpp panels.
B_Y3P	B7		
B_CLKN	A6		FlatLink™ Channel B LVDS Clock.
B_CLKP	B6		
DA0N	J3	LVDS Input (HS) CMOS Input (LS) (Failsafe)	MIPI® D-PHY Channel A Data Lane 0; data rate up to 1 Gbps.
DA0P	H3		
DA1N	J4		MIPI® D-PHY Channel A Data Lane 1; data rate up to 1 Gbps.
DA1P	H4		
DA2N	J6		MIPI® D-PHY Channel A Data Lane 2; data rate up to 1 Gbps.
DA2P	H6		
DA3N	J7		MIPI® D-PHY Channel A Data Lane 3; data rate up to 1 Gbps.
DA3P	H7		
DACN	J5		MIPI® D-PHY Channel A Clock Lane; operates up to 500 MHz.
DACP	H5		
DB0N	C1		MIPI® D-PHY Channel B Data Lane 0; data rate up to 1 Gbps.
DB0P	C2		
DB1N	D1		MIPI® D-PHY Channel B Data Lane 1; data rate up to 1 Gbps.
DB1P	D2		
DB2N	F1		MIPI® D-PHY Channel B Data Lane 2; data rate up to 1 Gbps.
DB2P	F2		
DB3N	G1		MIPI® D-PHY Channel B Data Lane 3; data rate up to 1 Gbps.
DB3P	G2		
DBCN	E1		MIPI® D-PHY Channel B Clock Lane; operates up to 500 MHz.
DBCP	E2		
EN	B1	CMOS Input with pullup (Failsafe)	Chip Enable and Reset. Device is reset (shutdown) when EN is low.
GND	A2, A8, B9, D5, E4, F4, F5, H9	Power Supply	Reference Ground.
IRQ	J9	CMOS Output	Interrupt Signal.
RSVD1	H8	CMOS Input/Output with pulldown	Reserved. This pin should be left unconnected for normal operation.
RSVD2	B2	CMOS Input with pulldown	Reserved. This pin should be left unconnected for normal operation.
REFCLK	H2	CMOS Input (Failsafe)	Optional External Reference Clock for LVDS Pixel Clock. If an External Reference Clock is not used, this pin should be pulled to GND with an external resistor. The source of the reference clock should be placed as close as possible with a series resistor near the source to reduce EMI.

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Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SCL	H1		Local I^2C Interface Clock.
SDA	J1	Open Drain Input/ Output (Failsafe)	Local I^2C Interface Bi-directional Data Signal.
VCC	A9, B8, D6, E5, E6, F6, J2	Power Supply	1.8 V Power Supply.
VCORE	J8		1.1 V Output from Voltage Regulator. This pin must have a 1 µF external capacitor to GND.

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6 Specifications

6.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply Voltage	V_{CC}	–0.3	2.175	V
Input Voltage	CMOS Input Terminals	–0.5	2.175	V
	DSI Input Terminals (DA x P/N, DB x P/N)	–0.4	1.4	V
Storage Temperature, T_S		–65	105	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	V_{CC} Power supply	1.65	1.8	1.95	V
V_{PSN}	Supply noise on any V_{CC} pin	$f_{(noise)}$ > 1MHz		0.05	V
T_A	Operating free-air temperature	-40		85	°C
T_{CASE}	Case temperature			92.2	°C
V_{DSI_PIN}	DSI input pin voltage range	-50		1350	mV
$f_{(I2C)}$	Local I^2C input frequency			400	kHz
f_{HS_CLK}	DSI HS clock input frequency	40		500	MHz
t_{setup}	DSI HS data to clock setup time	0.15			UI (1)
t_{hold}	DSI HS data to clock hold time; see Figure 7-3	0.15			UI (1)
Z_L	LVDS output differential impedance	90		132	Ω

(1) The unit interval (UI) is one half of the period of the HS clock; at 500 MHz the minimum setup and hold time is 150 ps

6.4 Thermal Information

THERMAL METRIC(1)		SN65DSI85 ZXH (nFBGA) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IL}	Low-level control signal input voltage				0.3 x VCC	V
V_{IH}	High-level control signal input voltage		0.7 × VCC			V
V_{OH}	High-level output voltage	I_{OH} = –4 mA	1.25			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_{LKG}	Input failsafe leakage current	V_{CC} = 0; $V_{CC(PIN)}$ = 1.8 V			±30	µA
I_{IH}	High level input current	Any input terminal			±30	µA
I_{IL}	Low level input current	Any input terminal			±30	µA
I_{OZ}	High-impedance output current	Any output terminal			±10	µA
I_{OS}	Short-circuit output current	Any output driving GND short			±20	mA
I_{CC}	Device active current	See [2]		127	212	mA
I_{ULPS}	Device standby current	All data and clock lanes are in ultra-low power state (ULPS)		7.7	10	mA
I_{RST}	Shutdown current	EN = 0		0.04	0.06	mA
R_{EN}	EN control input resistor			200		kΩ
MIPI DSI INTERFACE						
V_{IH-LP}	LP receiver input high threshold	See Figure 6-1	880			mV
V_{IL-LP}	LP receiver input low threshold	See Figure 6-1			550	mV
$\|V_{ID}\|$	HS differential input voltage		70		270	mV
$\|V_{IDT}\|$	HS differential input voltage threshold				50	mV
$V_{IL-ULPS}$	LP receiver input low threshold; ultra-low power state (ULPS)				300	mV
V_{CM-HS}	HS common mode voltage; steady-state		70		330	mV
ΔV_{CM-HS}	HS common mode peak-to-peak variation including symbol delta and interference				100	mV
V_{IH-HS}	HS single-ended input high voltage	See Figure 6-1			460	mV
V_{IL-HS}	HS single-ended input low voltage	See Figure 6-1	-40			mV
$V_{TERM-EN}$	HS termination enable; single-ended input voltage (both Dp AND Dn apply to enable)	Termination is switched simultaneous for Dn and Dp			450	mV
$R_{DIFF-HS}$	HS mode differential input impedance		80		125	Ω

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
FLATLINK LVDS OUTPUT						
$\|V_{OD}\|$	Steady-state differential output voltage A_Y x P/N and B_Y x P/N	CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 100Ω near end termination	180	245	313	mV
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 100Ω near end termination	215	293	372	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 100Ω near end termination	250	341	430	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 100Ω near end termination	290	389	488	
		CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 200Ω near end termination	150	204	261	
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 200Ω near end termination	200	271	346	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 200Ω near end termination	250	337	428	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 200Ω near end termination	300	402	511	
$\|V_{OD}\|$	Steady-state differential output voltage for A_CLKP/N and B_CLKP/N	CSR 0x19.3:2=00 and/or CSR 0x19.1:0=00 near end termination	140	191	244	mV
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 100Ω near end termination	168	229	290	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 100Ω near end termination	195	266	335	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 100Ω near end termination	226	303	381	
		CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 200Ω near end termination	117	159	204	
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 200Ω near end termination	156	211	270	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 200Ω near end termination	195	263	334	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 200Ω near end termination	234	314	399	
$\Delta\|V_{OD}\|$	Change in steady-state differential output voltage between opposite binary states	RL = 100Ω			35	mV
$V_{OC(SS)}$	Steady state common-mode output voltage(3)	CSR 0x19.6 = 1 and CSR 0x1B.6 = 1; and, or CSR 0x19.4 = 1 and CSR 0x1B.4 = 1; see Figure 6-2	0.8	0.9	1	V
		CSR 0x19.6 = 0 and, or CSR 0x19.4 = 0; see Figure 6-2	1.15	1.25	1.35	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	see Figure 6-2			35	mV
R_{LVDS_DIS}	Pull-down resistance for disabled LVDS outputs			1		kΩ

(1) All typical values are at V_{CC} = 1.8V and T_A = 25°C
(2) SN65DSI85: DUAL Channel DSI to DUAL Channel LVDS, 1920 x 1200

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- number of LVDS lanes = 2x(3 data lanes + 1 CLK lane)
- number of DSI lanes = 2x(4 data lanes + 1 CLK lane
- LVDS CLK OUT = 81.6M
- DSI CLK = 490M
- RGB888, LVDS18bpp

Maximum values are at V_{CC} = 1.95 V and T_A = 85°C

(3) Tested at V_{CC} = 1.8V , T_A = -40°C for MIN, T_A = 25°C for TYP, T_A = 85°C for MAX.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DSI						
t_{GS}	DSI LP glitch suppression pulse width				300	ps
t_{SK}	Skew time from DSI Channel A to Channel B in dual DSI operation	See Figure 7-12				
LVDS						
t_c	Output clock period		6.49		40	ns
t_w	High-level output clock (CLK) pulse duration			4/7 t_c		ns
t_0	Delay time, CLK↑ to 1st serial bit position	t_c = 6.49 ns; Input clock jitter < 25 ps (REFCLK)	–0.15		0.15	ns
t_1	Delay time, CLK↑ to 2nd serial bit position		1/7 t_c – 0.15		1/7 t_c + 0.15	ns
t_2	Delay time, CLK↑ to 3rd serial bit position		2/7 t_c – 0.15		2/7 t_c + 0.15	ns
t_3	Delay time, CLK↑ to 4th serial bit position		3/7 t_c – 0.15		3/7 t_c + 0.15	ns
t_4	Delay time, CLK↑ to 5th serial bit position		4/7 t_c – 0.15		4/7 t_c + 0.15	ns
t_5	Delay time, CLK↑ to 6th serial bit position		5/7 t_c – 0.15		5/7 t_c + 0.15	ns
t_6	Delay time, CLK↑ to 7th serial bit position		6/7 t_c – 0.15		6/7 t_c + 0.15	ns
t_r	Differential output rise-time	see Figure 7-1	180		500	ps
t_f	Differential output fall-time					
	LVDS CLK A to CLK B skew		–10		10	ps
EN, ULPS, RESET						
t_{en}	Enable time from EN or ULPS	$t_{c(o)}$ = 12.9 ns			1	ms
t_{dis}	Disable time to standby	$t_{c(o)}$ = 12.9 ns			0.1	ms
t_{reset}	Reset Time		10			ms
REFCLK						
F_{REFCLK}	REFCLK Freqeuncy. Supported frequencies: 25 MHz - 15 4MHz		25		154	MHz
t_r, t_f	REFCLK rise and fall time		100ps		1ns	s
t_{pj}	REFCLK Peak-to-Peak Phase Jitter				50	ps
Duty	REFCLK Duty Cycle		40%	50%	60%	
REFCLK or DSI CLK (DACP/N, DBCP/N)						
SSC_CLKIN	SSC enabled Input CLK center spread depth(2)		0.5%	1%	2%	
	Modulation Frequency Range		30		60	kHz

(1) All typical values are at V_{CC} = 1.8 V and T_A = 25°C

(2) For EMI reduction purpose, SN65DSI85 supports the center spreading of the LVDS CLK output through the REFCLK or DSI CLK input. The center spread CLK input to the REFCLK or DSI CLK is passed through to the LVDS CLK output A_CLKP/N and/or B_CLKP/N.

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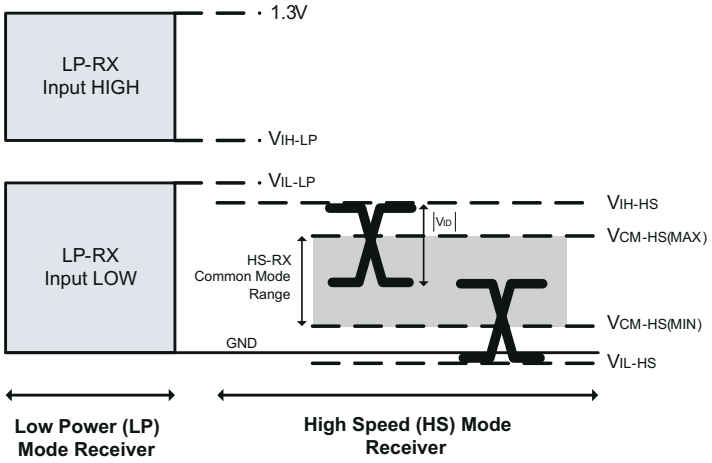

Figure 6-1. DSI Receiver Voltage Definitions

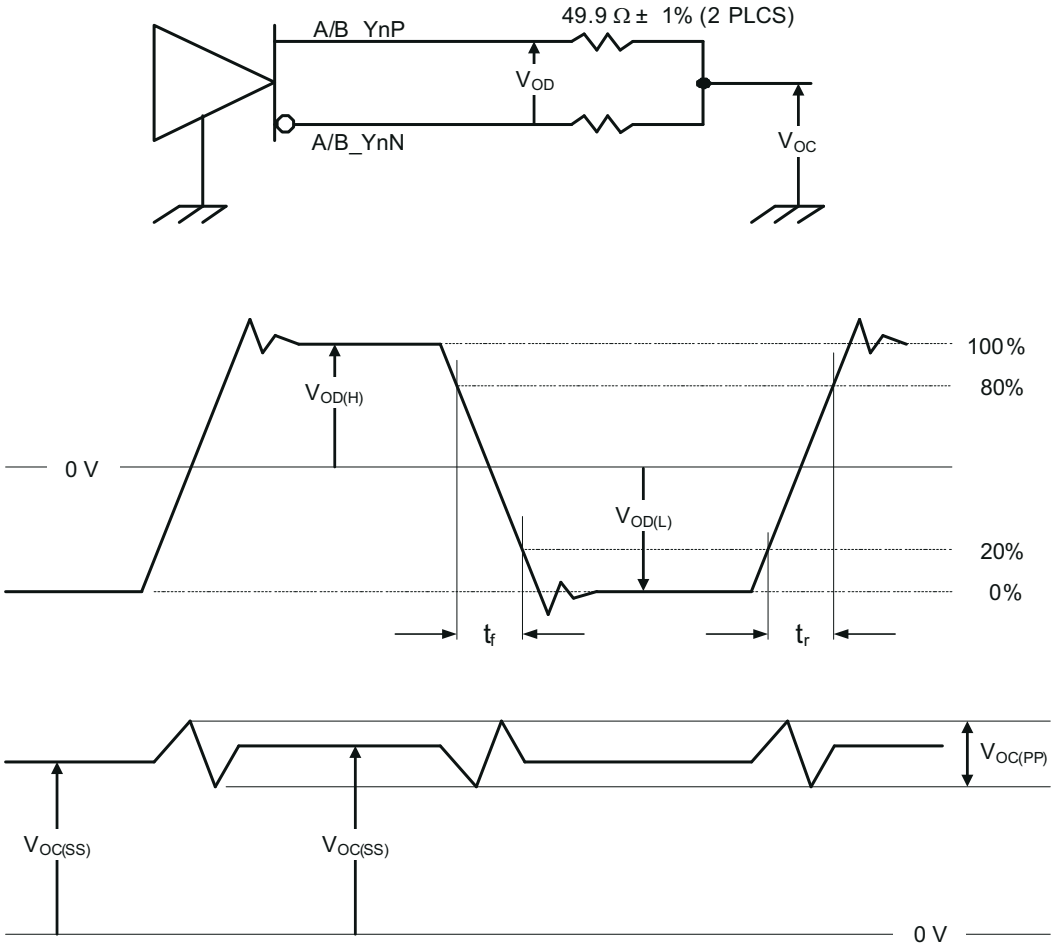

Figure 6-2. Test Load and Voltage Definitions for FlatLink™ Outputs

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Parameter Measurement Information

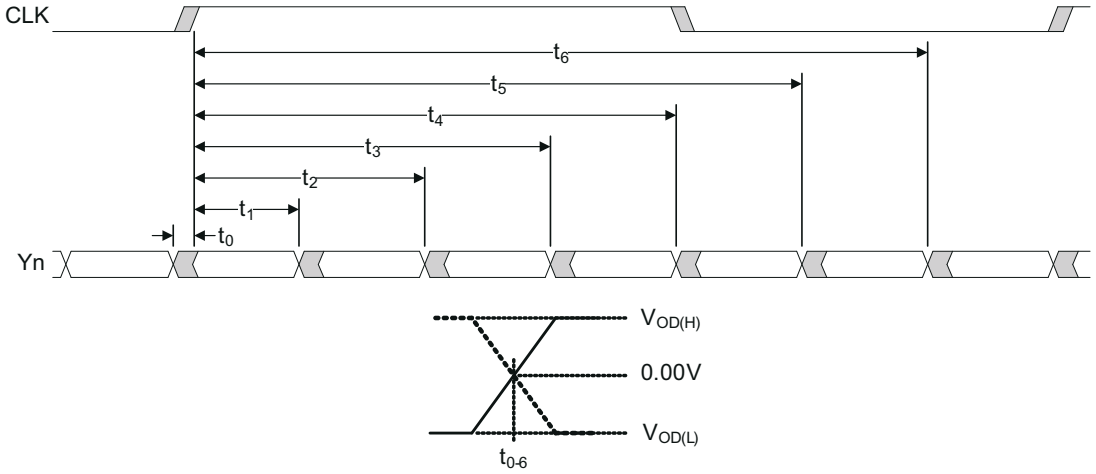
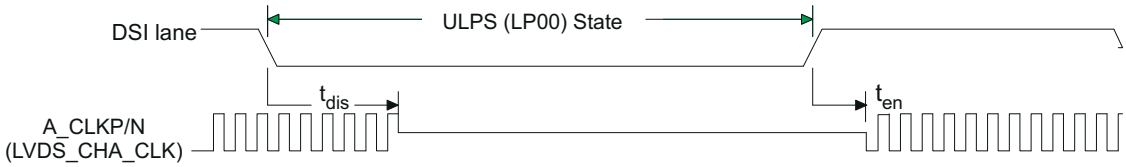


Figure 7-1. SN65DSI85 FlatLink™ Timing Definitions



A. See the ULPS section of the data sheet for the ULPS entry and exit sequence.
B. ULPS entry and exit protocol and timing requirements must be met per MIPI® DPHY specification.

Figure 7-2. ULPS Timing Definition

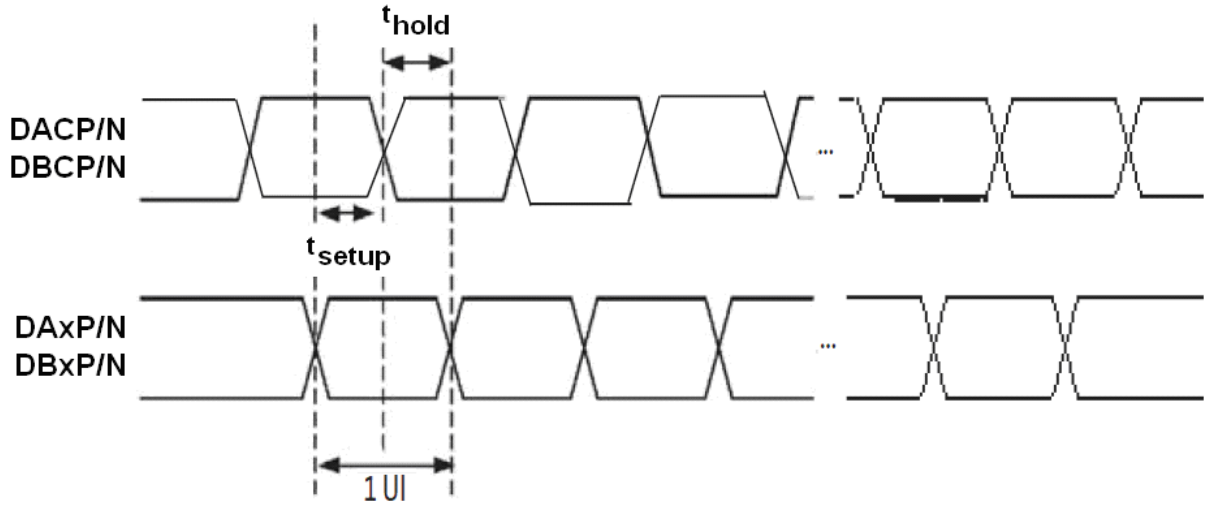


Figure 7-3. DSI HS Mode Receiver Timing Definitions

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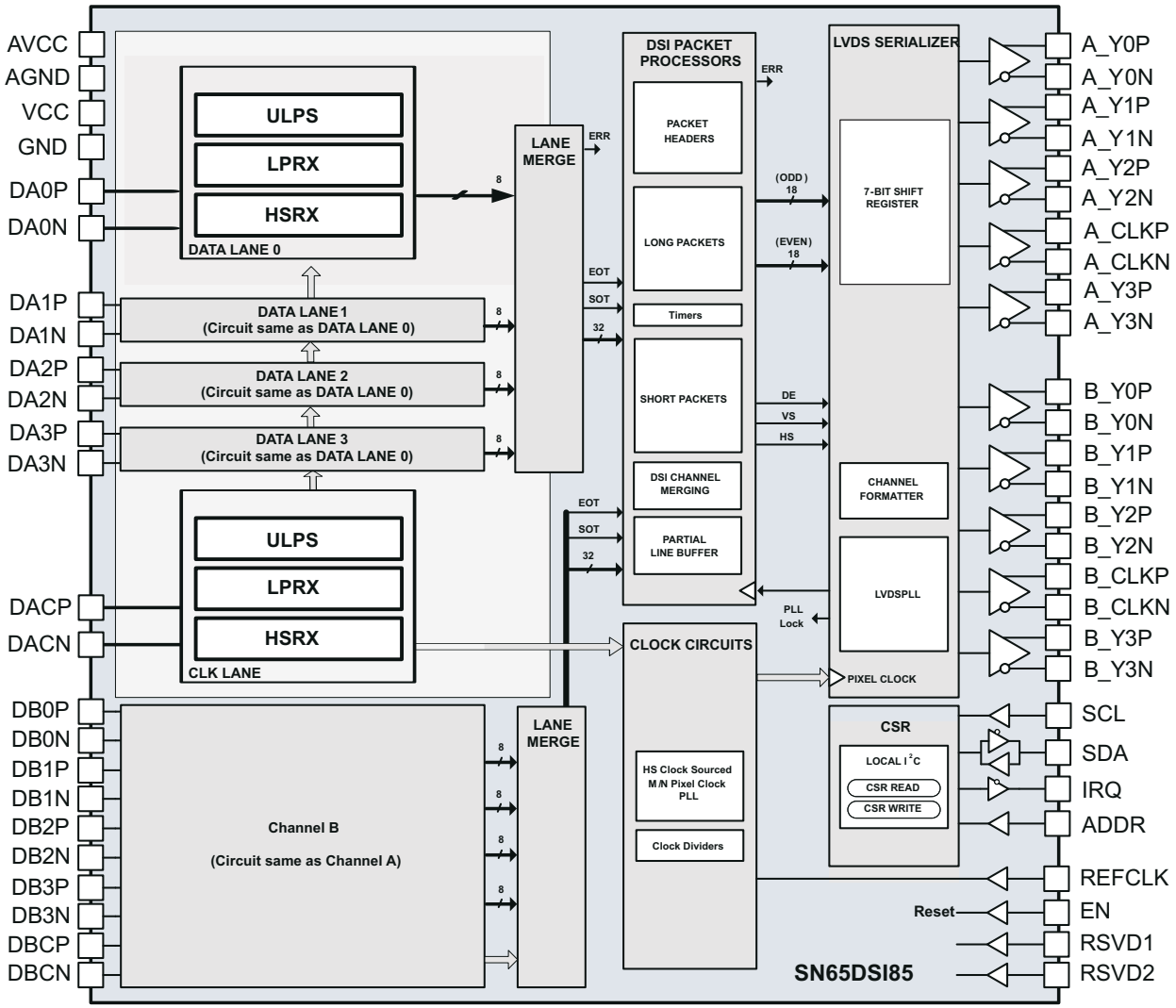
7 Detailed Description

7.1 Overview

The SN65DSI85 to FlatLink bridge features a dual-channel MIPI D-PHY receiver front-end configuration with 4 lanes per channel operating a 1 Gbps per lane; a maximum input bandwidth of 8 Gbps. The bridge decodes MIPI DSI 18bpp RGB666 and 24 bpp RGB8888 packets and converts the formatted video data stream to a FlatLink compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Dual-Link LVDS Single-Link LVDS, or two Single-Link LVDS interface(s) with four data lanes per link.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Clock Configurations and Multipliers

The FlatLink™ LVDS clock may be derived from the DSI channel A clock, or from an external reference clock source. When the MIPI® D-PHY channel A HS clock is used as the LVDS clock source, the D-PHY clock lane must operate in HS free-running (continuous) mode; this feature eliminates the need for an external reference clock reducing system costs

The reference clock source is selected by HS_CLK_SRC (CSR 0x0A.0) programmed through the local I2C interface. If an external reference clock is selected, it is multiplied by the factor in REFCLK_MULTIPLIER (CSR 0x0B.1:0) to generate the FlatLink™ LVDS output clock. When an external reference clock is selected, it must be between 25 MHz and 154 MHz. If the DSI channel A clock is selected, it is divided by the factor in DSI_CLK_DIVIDER (CSR 0x0B.7:3) to generate the FlatLink™ LVDS output clock. Additionally, LVDS_CLK_RANGE (CSR 0x0A.3:1) and CH_DSI_CLK_RANGE(CSR 0x12) must be set to the frequency range of the FlatLink™ LVDS output clock and DSI Channel A input clock respectively for the internal PLL to operate correctly. After these settings are programmed, PLL_EN (CSR 0x0D.0) must be set to enable the internal PLL.

7.3.2 ULPS

The SN65DSI85 supports the MIPI® defined ultra-low power state (ULPS). While the device is in the ULPS, the CSR registers are accessible via I2C interface. ULPS sequence should be issued to all active DSI CLK and/or DSI data lanes of the enabled DSI Channels for the SN65DSI85 enter the ULPS. The Following sequence should be followed to enter and exit the ULPS.

1. Host issues a ULPS entry sequence to all DSI CLK and data lanes enabled.
2. When host is ready to exit the ULPS mode, host issues a ULPS exit sequence to all DSI CLK and data lanes that need to be active in normal operation.
3. Wait for a minimum of 3 ms.
4. Set the SOFT_RESET bit (CSR 0x09.0).
5. Device resumes normal operation.(i.e video streaming resumes on the panel).

7.3.3 LVDS Pattern Generation

The SN65DSI85 supports a pattern generation feature on LVDS Channels. This feature can be used to test the LVDS output path and LVDS panels in a system platform. The pattern generation feature can be enabled by setting the CHA_TEST_PATTERN bit at address 0x3C. No DSI data is received while the pattern generation feature is enabled.

There are three modes available for LVDS test pattern generation. The mode of test pattern generation is determined by register configuration as shown in the tables below.

Table 7-1. Test Pattern Generation

Test Pattern Generation Mode	Register Configurations
Single LVDS configuration mode	LVDS_LINK_CFG(CSR 0x18.4) = 1b DSI_CH_MODE(CSR 0x10.6:5) = XXb CHA_TEST_PATTERN(CSR 0x3C.4) = 1b CHB_TEST_PATTERN(CSR 0x3C.0) = 0b
Dual LVDS configuration mode	LVDS_LINK_CFG(CSR 0x18.4) = 0b DSI_CH_MODE(CSR 0x10.6:5) = 0Xb CHA_TEST_PATTERN(CSR 0x3C.4) = 1b CHB_TEST_PATTERN(CSR 0x3C.0) = 0b
Two independent LVDS configuration mode	LVDS_LINK_CFG(CSR 0x18.4) = 0b DSI_CH_MODE(CSR 0x10.6:5) = 10b CHA_TEST_PATTERN(CSR 0x3C.4) = 1b CHB_TEST_PATTERN(CSR 0x3C.0) = 1b

The following tables show lists of video registers that need to be configured for test pattern generation video parameters.

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1. Single LVDS configuration

Table 7-2. Video Registers

Bit Address	Register Name
0x20.7:0	CHA_ACTIVE_LINE_LENGTH_LOW
0x21.3:0	CHA_ACTIVE_LINE_LENGTH_HIGH
0x24.7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW
0x25.3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH
0x2C.7:0	CHA_HSYNC_PULSE_WIDTH_LOW
0x2D.1:0	CHA_HSYNC_PULSE_WIDTH_HIGH
0x30.7:0	CHA_VSYNC_PULSE_WIDTH_LOW
0x31.1:0	CHA_VSYNC_PULSE_WIDTH_HIGH
0x34.7:0	CHA_HORIZONTAL_BACK_PORCH
0x36.7:0	CHA_VERTICAL_BACK_PORCH
0x38.7:0	CHA_HORIZONTAL_FRONT_PORCH
0x3A.7:0	CHA_VERTICAL_FRONT_PORCH

2. Dual LVDS configuration
   - Same set of video registers are used as in single LVDS configuration.
3. Two independent LVDS configuration mode.

   Both Channel A and Channel B register parameters need to be configured.

Table 7-3. Channel A and B Registers

Bit Address	Register Name
Channel A	
0x20.7:0	CHA_ACTIVE_LINE_LENGTH_LOW
0x21.3:0	CHA_ACTIVE_LINE_LENGTH_HIGH
0x24.7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW
0x25.3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH
0x2C.7:0	CHA_HSYNC_PULSE_WIDTH_LOW
0x2D.1:0	CHA_HSYNC_PULSE_WIDTH_HIGH
0x30.7:0	CHA_VSYNC_PULSE_WIDTH_LOW
0x31.1:0	CHA_VSYNC_PULSE_WIDTH_HIGH
0x34.7:0	CHA_HORIZONTAL_BACK_PORCH
0x36.7:0	CHA_VERTICAL_BACK_PORCH
0x38.7:0	CHA_HORIZONTAL_FRONT_PORCH
0x3A.7:0	CHA_VERTICAL_FRONT_PORCH
Channel B	
0x22.7:0	CHB_ACTIVE_LINE_LENGTH_LOW
0x23.3:0	CHB_ACTIVE_LINE_LENGTH_HIGH
0x26.7:0	CHB_VERTICAL_DISPLAY_SIZE_LOW
0x27.3:0	CHB_VERTICAL_DISPLAY_SIZE_HIGH
0x2E.7:0	CHB_HSYNC_PULSE_WIDTH_LOW
0x2F.1:0	CHB_HSYNC_PULSE_WIDTH_HIGH
0x32.7:0	CHB_VSYNC_PULSE_WIDTH_LOW
0x33.1:0	CHB_VSYNC_PULSE_WIDTH_HIGH
0x35.7:0	CHB_HORIZONTAL_BACK_PORCH
0x37.7:0	CHB_VERTICAL_BACK_PORCH
0x39.7:0	CHB_HORIZONTAL_FRONT_PORCH

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Table 7-3. Channel A and B Registers (continued)

Bit Address	Register Name
0x3B.7:0	CHB_VERTICAL_FRONT_PORCH

7.4 Device Functional Modes

7.4.1 Operating Modes

The SN65DSI85 can be configured for several different operating modes via LVDS_LINK_CFG (CSR 0x18.4), LEFT_RIGHT_PIXELS (CSR 0x10.7), and DSI_CHANNEL_MODE (CSR 0x10.6:5). These modes are summarized in Table 7-4. In each of the modes, video data can be 18 bpp or 24 bpp.

7.4.2

Table 7-4. SN65DSI85 Operating Modes

MODE	CSR 0x18.4	CSR 0x10.7	CSR 0x10.6:5	DESCRIPTION
	LVDS_LINK_CFG	LEFT_RIGHT_PIXES	DSI_CH_MODE	
Single DSI Input to Single-Link LVDS	1	N/A	01	Single DSI Input on Channel A to Single-Link LVDS output on Channel A.
Single DSI Input to Dual-Link LVDS	0	N/A	01	Single DSI Input on Channel A to Dual-Link LVDS output with Odd pixels on Channel A and Even pixels on Channel B.
Dual DSI Input (Odd/Even) to Single-Link LVDS (1)	1	0	00	Dual DSI Input with Odd pixels received on Channel A and Even pixels received on Channel B. Data is output to Single-Link LVDS on Channel A.
Dual DSI Input (Odd/Even) to Dual-Link LVDS (1)	0	0	00	Dual DSI Input with Odd pixels received on Channel A and Even pixels received on Channel B. Data is output to Dual-Link LVDS with Odd pixels on Channel A and Even pixels on Channel B.
Dual DSI Input (Left/Right) to Single-Link LVDS (2)	1	1	00	Dual DSI Input with Left pixels received on Channel A and Right pixels received on Channel B. Data is output to Single-Link LVDS on Channel A.
Dual DSI Input (Left/Right) to Dual-Link LVDS (2)	0	1	00	Dual DSI Input with Left pixels received on Channel A and Right pixels received on Channel B. Data is output to Dual-Link LVDS with Odd pixels on Channel A and Even pixels on Channel B.
Dual DSI Inputs (two streams) to two Single-Link LVDS (3)	0	N/A	10	One video stream input on DSI Channel A and output to Single-Link LVDS on Channel A. Another video stream input on DSI Channel B and output to Single-Link LVDS on Channel B.

(1) In these modes, DSI Channel A and DSI Channel B must be set to have the same number of data lanes enabled and the data format must be the same for both lanes.

(2) In these modes, DSI Channel A and DSI Channel B can each have a different number of data lanes enabled, but the data format must be the same for both lanes.

(3) In this mode, DSI Channel A and DSI Channel B can each have a different number of data lanes enabled, and the data format for each Channel can be different.

7.4.3 Reset Implementation

When EN is de-asserted (low), the SN65DSI85 is in SHUTDOWN or RESET state. In this state, CMOS inputs are ignored, the MIPI® D-PHY inputs are disabled and outputs are high impedance. It is critical to transition the EN input from a low to a high level after the V_{CC} supply has reached the minimum operating voltage as shown in Figure 7-1. This is achieved by a control signal to the EN input, or by an external capacitor connected between EN and GND.

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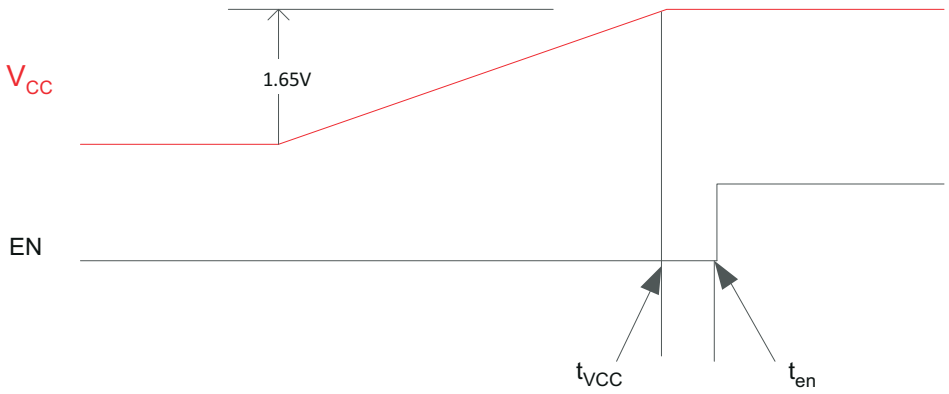

Figure 7-1. Cold Start V_{CC} Ramp up to EN

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{CC} supply, where a slower ramp-up results in a larger value external capacitor. See the latest reference schematic for the SN65DSI85 device and, or consider approximately 200 nF capacitor as a reasonable first estimate for the size of the external capacitor.

Both EN implementations are shown in Figure 7-2 and Figure 7-3.

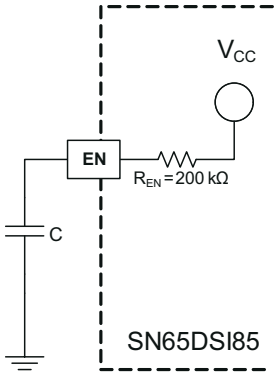

Figure 7-2. External Capacitor Controlled EN

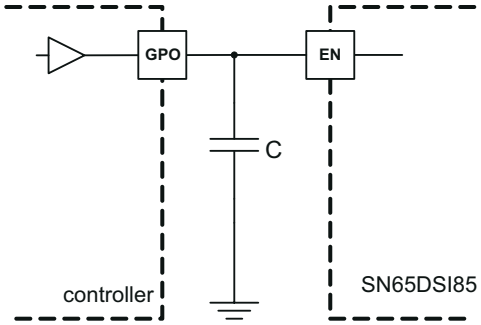

Figure 7-3. EN Input from Active Controller

When the SN65DSI85 is reset while V_{CC} is high, the EN pin must be held low for at least 10 ms before being asserted high as described in Table 7-5 to be sure that the device is properly reset. The DSI CLK lane MUST be in HS and the DSI data lanes MUST be driven to LP11 while the device is in reset before the EN pin is asserted per the timing described in Table 7-5.

7.4.4 Initialization Sequence

Use the following initialization sequence to setup the SN65DSI85. This sequence is required for proper operation of the device. Steps 9 through 11 in the sequence are optional.

Table 7-5. Initialization Sequence

INITIALIZATION SEQUENCE NUMBER	INITIALIZATION SEQUENCE DESCRIPTION
Init seq 1	Power on
Init seq 2	After power is applied and stable, the DSI CLK lanes MUST be in HS state and the DSI data lanes MUST be driven to LP11 state
Init seq 3	Set EN pin to Low
Wait 10 ms (1)	
Init seq 4	Tie EN pin to High

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Table 7-5. Initialization Sequence (continued)

INITIALIZATION SEQUENCE NUMBER	INITIALIZATION SEQUENCE DESCRIPTION
Wait 10 ms (1)	
Init seq 5	Initialize all CSR registers to their appropriate values based on the implementation (The SN65DSI8x is not functional until the CSR registers are initialized)
Init seq 6	Set the PLL_EN bit (CSR 0x0D.0)
Wait 10 ms (1)	
Init seq 7	Set the SOFT_RESET bit (CSR 0x09.0)
Wait 10 ms (1)	
Init seq 8	Change DSI data lanes to HS state and start DSI video stream
Wait 5 ms (1)	
Init seq 9	Read back all resisters and confirm they were correctly written
Init seq 10	Write 0xFF to CSR 0xE5 and CSR 0xE6 to clear the error registers
Wait 1 ms (1)	
Init seq 11	Read CSR 0xE5 and CSR 0xE6. If CSR 0xE5 and CSR 0xE6 != 0x00, then go back to step #2 and re-initialize

(1) Minimum recommended delay. It is fine to exceed these.

7.4.5 LVDS Output Formats

The SN65DSI85 processes DSI packets and produces video data driven to the FlatLink™ LVDS interface in an industry standard format. Single-Link LVDS and Dual-Link LVDS are supported by the SN65DSI85; when the FlatLink™ output is implemented in a Dual-Link configuration, channel A carries the odd pixel data, and channel B carries the even pixel data. During conditions such as the default condition, and some video synchronization periods, where no video stream data is passing from the DSI input to the LVDS output, the SN65DSI85 transmits zero value pixel data on the LVDS outputs while maintaining transmission of the vertical sync and horizontal sync status.

Figure 7-4 illustrates a Single-Link LVDS 18 bpp application.

Figure 7-5 illustrates a Dual-Link 24 bpp application using Format 2, controlled by CHA_24BPP_FORMAT1 (CSR 0x18.1) and CHB_24BPP_FORMAT1 (CSR 0x18.0). In data Format 2, the two MSB per color are transferred on the Y3P/N LVDS lane.

Figure 7-6 illustrates a 24 bpp Single-Link application using Format 1. In data Format 1, the two LSB per color are transferred on the Y3P/N LVDS lane.

Figure 7-7 illustrates a Single-Link LVDS application where 24 bpp data is received from DSI and converted to 18 bpp data for transmission to an 18 bpp panel. This application is configured by setting CHA_24BPP_FORMAT1 (CSR 0x18.1) to 1 and CHA_24BPP_MODE (CSR 0x18.3) to 0. In this configuration, the SN65DSI85 will not transmit the 2 LSB per color since the Y3P/N LVDS lane is disabled.

Note

Note: Figure 7-4, Figure 7-5, Figure 7-6, and Figure 7-7 only illustrate a few example applications for the SN65DSI85. Other applications are also supported.

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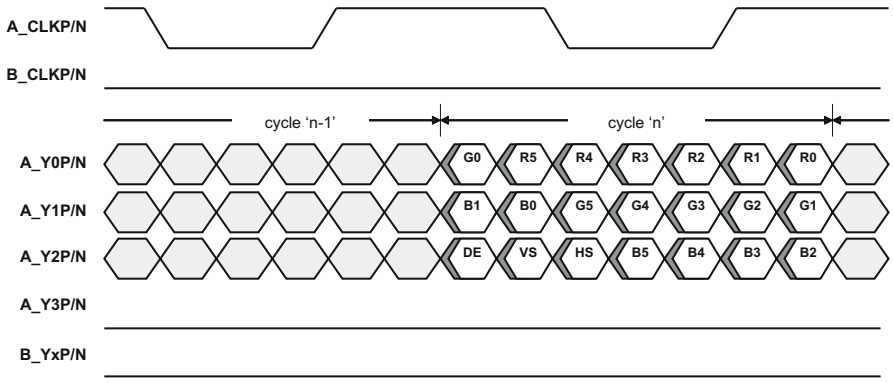
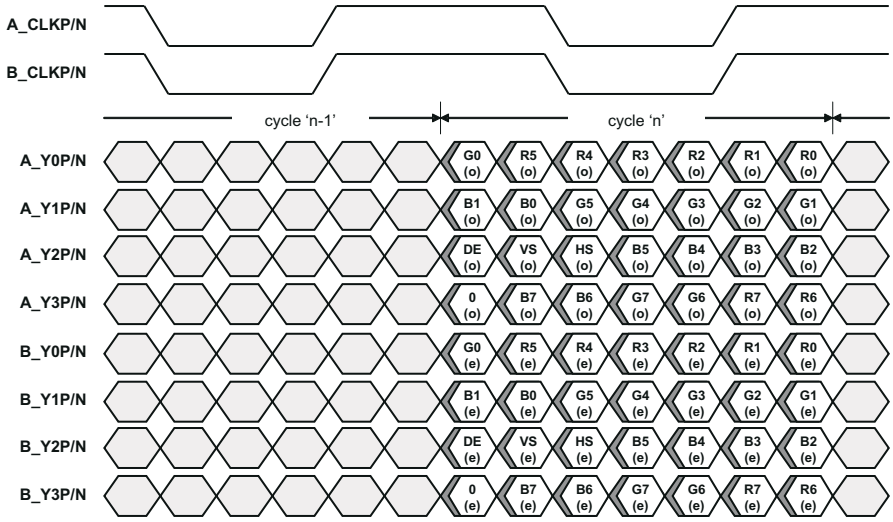


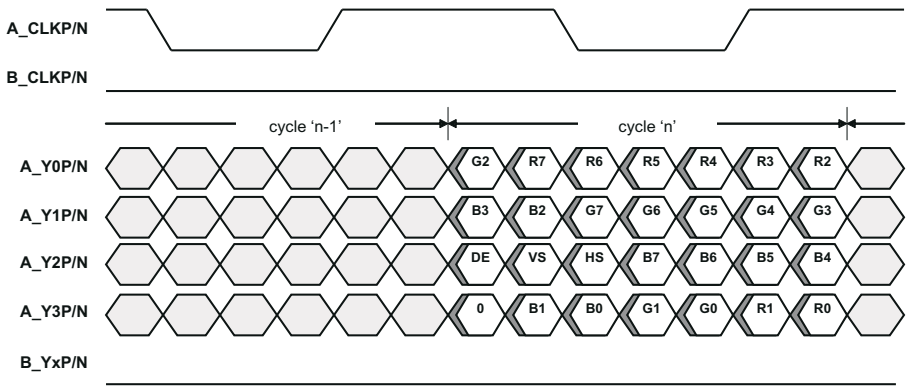
DE = Data Enable; Channel B Clock, Channel B Data, and A_Y3P/N are Output Low

Figure 7-4. FlatLink™ Output Data; Single-Link 18 bpp



DE = Data Enable; (o) = Odd Pixels; (e) = Even Pixels

Figure 7-5. FlatLink™ Output Data (Format 2); Dual-Link 24 bpp



DE = Data Enable; Channel B Clock and Data are Output Low

Figure 7-6. FlatLink™ Output Data (Format 1); Single-Link 24 bpp

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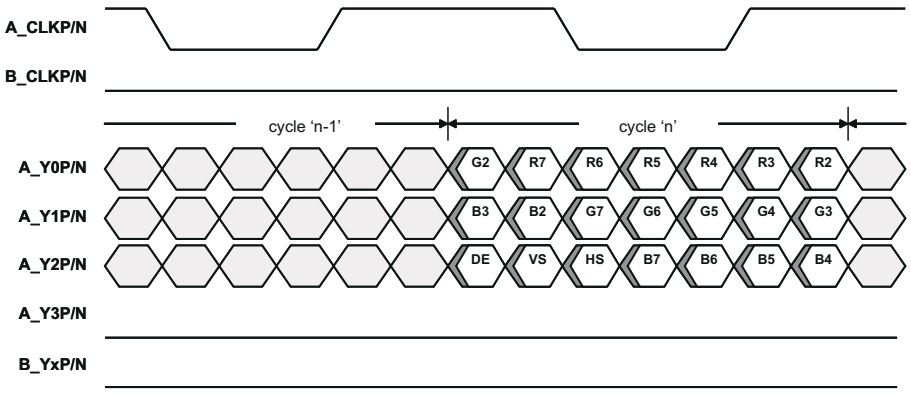

DE = Data Enable; Channel B Clock, Channel B Data, and A_Y3P/N are Output Low; Channel B Clock, Channel B Data, and A_Y3P/N are Output Low

Figure 7-7. FlatLink™ Output Data (Format 1); 24 bpp to Single-Link 18 bpp Conversion

7.4.6 DSI Lane Merging

The SN65DSI85 supports four DSI data lanes per input channel, and may be configured to support one, two, or three DSI data lanes per channel. Unused DSI input pins on the SN65DSI85 should be left unconnected or driven to LP11 state.The bytes received from the data lanes are merged in HS mode to form packets that carry the video stream. DSI data lanes are bit and byte aligned.

Figure 7-8 illustrates the lane merging function for each channel; 4-Lane, 3-Lane, and 2-Lane modes are shown.

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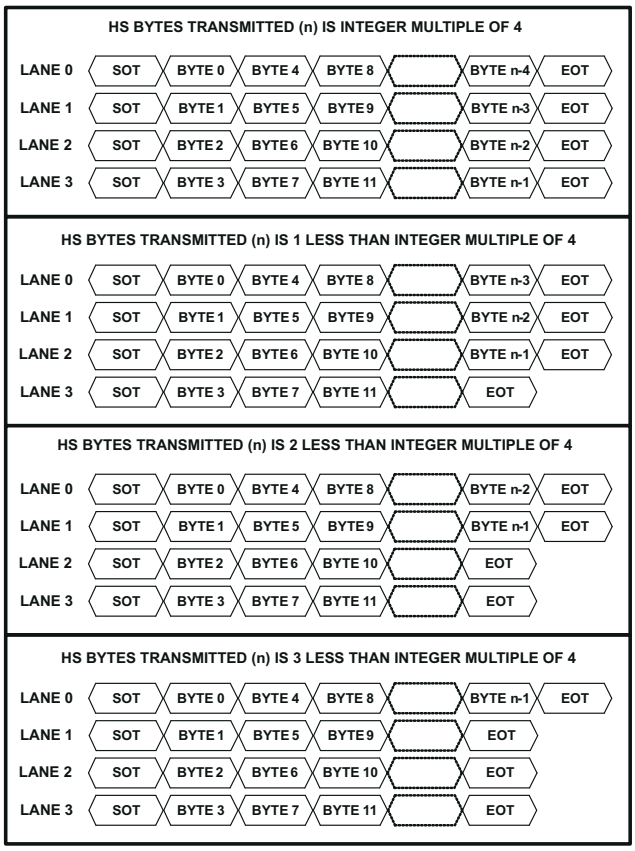
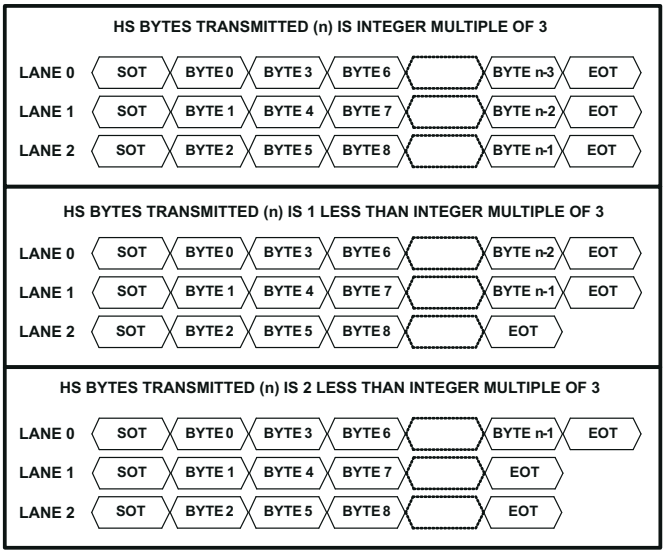
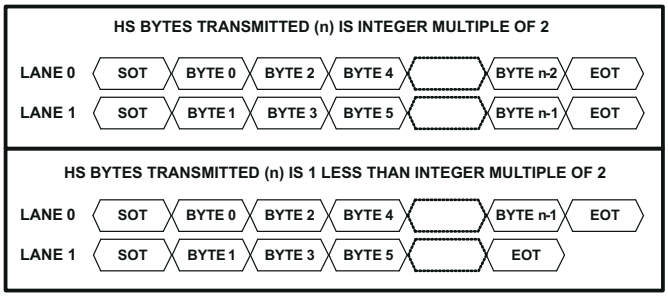


4 DSI Data Lane Configuration (default)



3 DSI Data Lane Configuration



2 DSI Data Lane Configuration

Figure 7-8. SN65DSI85 DSI Lane Merging Illustration

7.4.7 DSI Pixel Stream Packets

The SN65DSI85 processes 18 bpp (RGB666) and 24 bpp (RGB888) DSI packets on each channel as shown in Figure 7-9, Figure 7-10, and Figure 7-11.

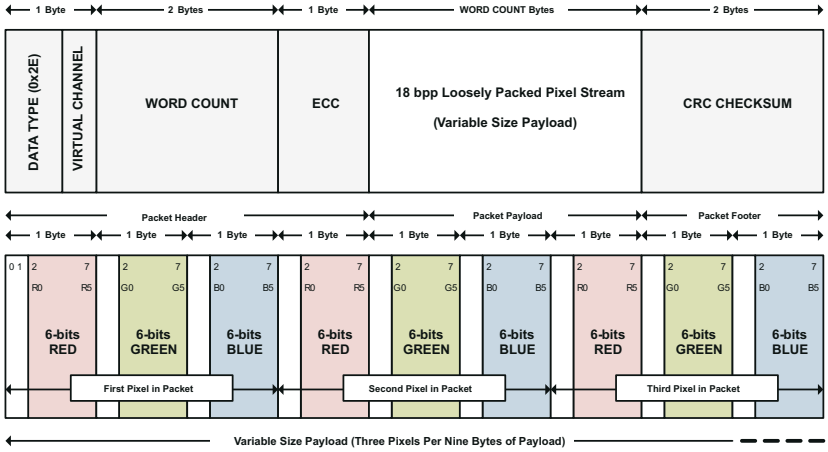


Figure 7-9. 18 bpp (Loosely Packed) DSI Packet Structure

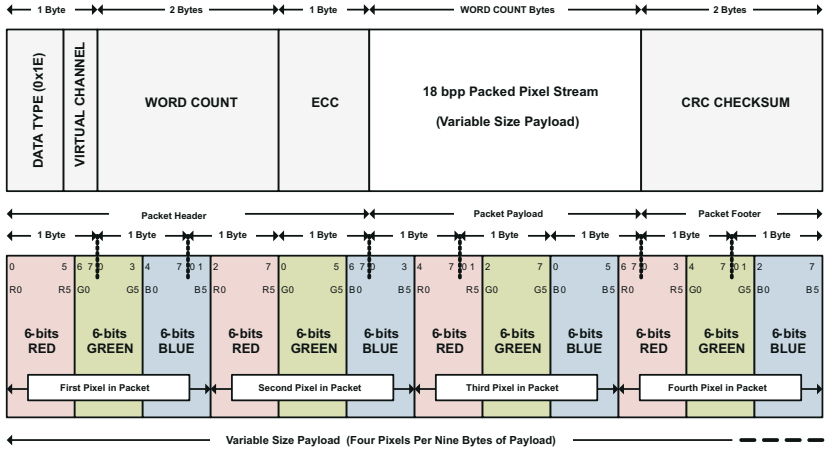


Figure 7-10. 18 bpp (Tightly Packed) DSI Packet Structure

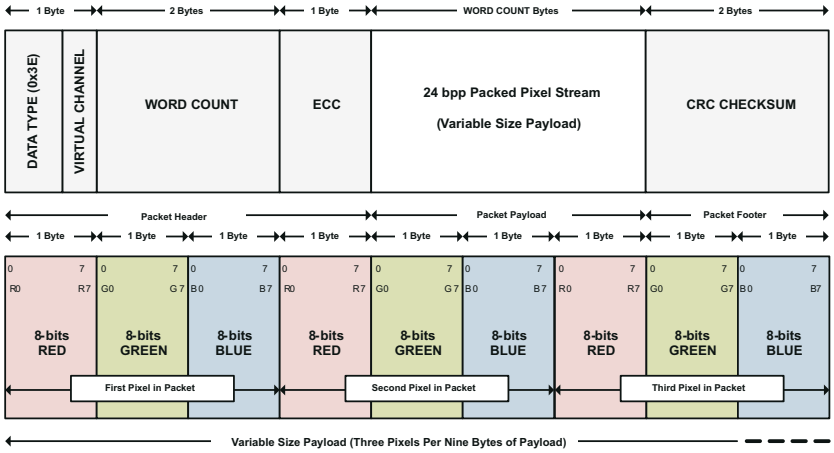


Figure 7-11. 24 bpp DSI Packet Structure

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7.4.8 DSI Video Transmission Specifications

The SN65DSI85 supports burst video mode and non-burst video mode with sync events or with sync pulses packet transmission as described in the DSI specification. The burst mode supports time-compressed pixel stream packets that leave added time per scan line for power savings LP mode. The SN65DSI85 requires a transition to LP mode once per frame to enable PHY synchronization with the DSI host processor; however, for a robust and low-power implementation, the transition to LP mode is recommended on every video line.

Figure 7-12 illustrates the DSI video transmission applied to SN65DSI85 applications. In all applications, the LVDS output rate must be less than or equal to the DSI input rate. The first line of a video frame shall start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance since this has a direct impact on the visual performance of the display panel; that is, these packets generate the HS and VS (horizontal and vertical sync) signals on the LVDS interface after the delay programmed into CHA_SYNC_DELAY_LOW/HIGH (CSR 0x28.7:0 and 0x29.3:0) and/or CHB_SYNC_DELAY_LOW/HIGH (CSR 0x2A.7:0 and 0x2B.3:0). When configured for dual DSI channels, the SN65DSI85 uses the VSS, VSE, and HSS packets from channel A to generate the HS and VS (horizontal and vertical sync) signals on the LVDS interface, and the VSS, VSE, and HSS packets from channel B are ignored.

As required in the DSI specification, the SN65DSI85 requires that pixel stream packets contain an integer number of pixels (i.e. end on a pixel boundary); it is recommended to transmit an entire scan line on one pixel stream packet. When a scan line is broken in to multiple packets, inter-packet latency shall be considered such that the video pipeline (ie. pixel queue or partial line buffer) does not run empty (i.e. under-run); during scan line processing, if the pixel queue runs empty, the SN65DSI85 transmits zero data (18’b0 or 24’b0) on the LVDS interface.

When configured for dual DSI channels, the SN65DSI85 supports ODD/EVEN configurations and LEFT/RIGHT configurations. In the ODD/EVEN configuration, the odd pixels for each scan line are received on channel A, and the even pixels are received on channel B. In LEFT/RIGHT mode, the LEFT portion of the line is received on channel A, and the right portion of the line is received on channel B. Neither the channel A LEFT portion input or the channel B RIGHT portion input per line shall exceed 1408 pixels, which is defined as ½ of the maximum line size (2560 pixels in WQXGA 2560x1600 mode) plus 10% headroom. The pixels received on channel B in LEFT/RIGHT mode are buffered during the LEFT side transmission to LVDS, and begin transmission to LVDS when the LEFT-side input buffer runs empty.

When configured for two single DSI channels, the SN65DSI85 requires that the LVDS output clocks for both video data streams be the same.

Note

When the HS clock is used as a source for the LVDS pixel clock, the LP mode transitions apply only to the data lanes, and the DSI clock lane remains in the HS mode during the entire video transmission.

The DSI85 does not support the DSI Virtual Channel capability or reverse direction (peripheral to processor) transmissions.

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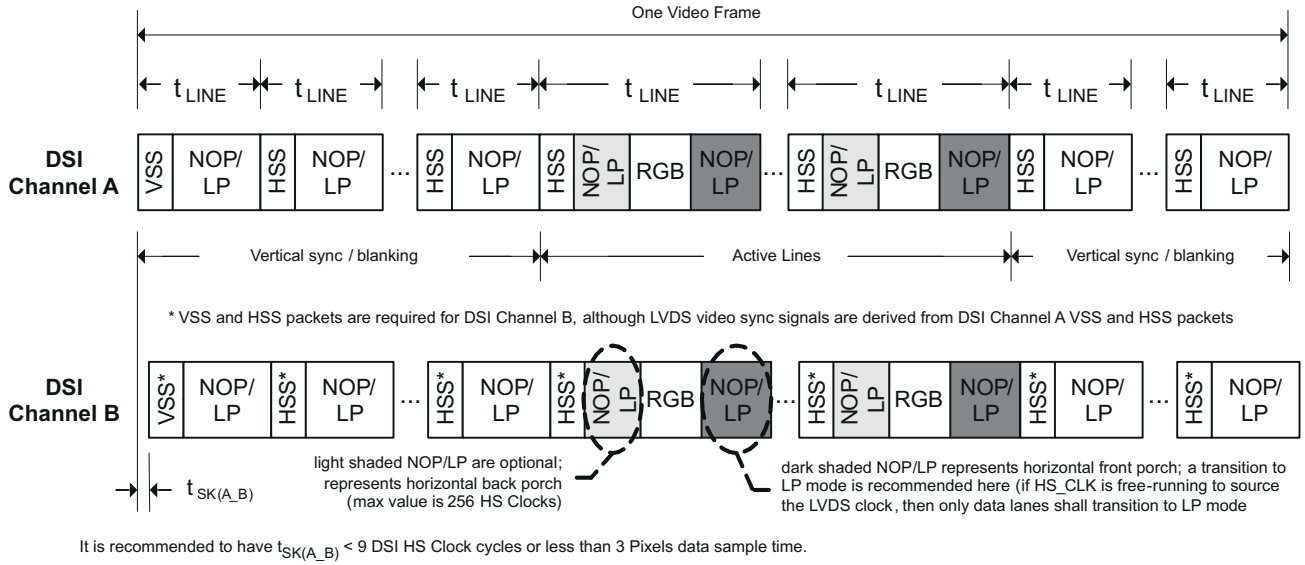
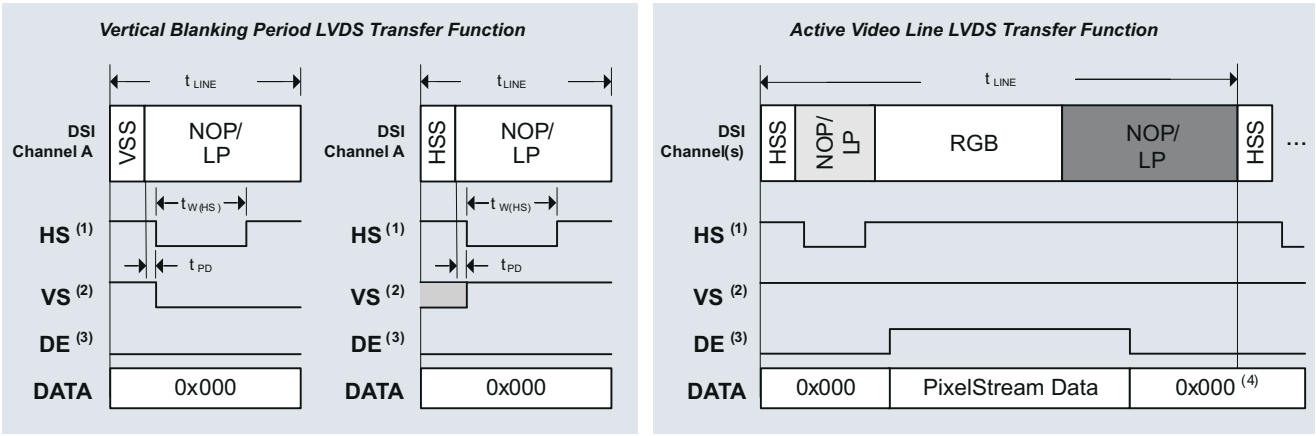


More delay between DSI Channel A and B can be tolerated by SN65DSI85, contact Texas Instruments for SN65DSI8X device configuration information that would allow longer delay between DSI Channel A and B.



(1) The assertion of HS is delayed (t_{PD}) by a programmable number of pixel clocks from the last bit of VSS/HSS packet received on DSI. The HS pulse width ($t_{W(HS)}$) is also programmable. The illustration shows HS active low.

(2) VS is signaled for a programmable number of lines (t_{LINE}) and is asserted when HS is asserted for the first line of the frame . VS is de -asserted when HS is asserted after the number of lines programmed has been reached. The illustration shows VS active low

(3) DE is asserted when active pixel data is transmitted on LVDS, and polarity is set independent to HS/VS. The illustration shows DE active high

(4) After the last pixel in an active line is output to LVDS, the LVDS data is output zero

LEGEND	
VSS	DSI Sync Event Packet: V Sync Start
HSS	DSI Sync Event Packet: H Sync Start
RGB	A sequence of DSI Pixel Stream Packets and Null Packets
NOP/LP	DSI Null Packet , Blanking Packet , or a transition to LP Mode

Figure 7-12. DSI Channel Transmission and Transfer Function

7.5 Programming

7.5.1 Local I²C Interface Overview

The SN65DSI85 local I²C interface is enabled when EN is input high, access to the CSR registers is supported during ultra-low power state (ULPS). The SCL and SDA terminals are used for I²C clock and I²C data respectively. The SN65DSI85 I²C interface conforms to the two-wire serial interface defined by the I²C Bus Specification, Version 2.1 (January 2000), and supports fast mode transfers up to 400 kbps.

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The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for SN65DSI85 is factory preset to 010110X with the least significant bit being determined by the ADDR control input. Table 7-6 clarifies the SN65DSI85 target address.

Table 7-6. SN65DSI85 I²C Target Address Description (1) (2)

SN65DSI85 I2C TARGET ADDRESS							
BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	1	0	1	1	0	ADDR	0/1

(1) When ADDR=1, Address Cycle is 0x5A (Write) and 0x5B (Read)
(2) When ADDR=0, Address Cycle is 0x58 (Write) and 0x59 (Read)

The following procedure is followed to write to the SN65DSI85 I²C registers.

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI85 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The SN65DSI85 acknowledges the address cycle.
3. The master presents the sub-address (I2C register within SN65DSI85) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSI85 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I²C register.
6. The SN65DSI85 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SN65DSI85.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure is followed to read the SN65DSI85 I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN65DSI85 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The SN65DSI85 acknowledges the address cycle.
3. The SN65DSI85 transmit the contents of the memory registers MSB-first starting at register 00h. If a write to the SN65DSI85 I2C register occurred prior to the read, then the SN65DSI85 will start at the sub-address specified in the write.
4. The SN65DSI85 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I2C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the SN65DSI85 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure is followed for setting a starting sub-address for I²C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI85 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The SN65DSI85 acknowledges the address cycle.
3. The master presents the sub-address (I²C register within SN65DSI85) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSI85 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

7.6 Register Maps

7.6.1 Control and Status Registers Overview

Many of the SN65DSI85 functions are controlled by the Control and Status Registers (CSR). All CSR registers are accessible through the local I²C interface.

See the following tables for the SN65DSI85 CSR descriptions. Reserved or undefined bit fields should not be modified. Otherwise, the device may operate incorrectly.

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Table 7-7. CSR Bit Field Definitions – ID Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS(1)
0x00 – 0x08	7:0	Reserved Addresses 0x08 - 0x00 = {0x01, 0x20, 0x20, 0x20, 0x44, 0x53, 0x49, 0x38, 0x35}	Reserved	RO

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write 1 to Clear; WO = Write Only (reads return undetermined values)

Table 7-8. CSR Bit Field Definitions – Reset and Clock Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x09	0	SOFT_RESET This bit automatically clears when set to 1 and returns zeros when read. This bit must be set after the CSR's are updated. This bit must also be set after making any changes to the DSI clock rate or after changing between DSI burst and non-burst modes. 0 – No action (default) 1 – Reset device to default condition excluding the CSR bits.	0	WO
0x0A	7	PLL_EN_STAT After PLL_EN_STAT = 1, wait at least 3 ms for PLL to lock. 0 – PLL not enabled (default) 1 – PLL enabled	0	RO
	3:1	LVDS_CLK_RANGE This field selects the frequency range of the LVDS output clock. 000 – 25 MHz ≤ LVDS_CLK < 37.5 MHz 001 – 37.5 MHz ≤ LVDS_CLK < 62.5 MHz 010 – 62.5 MHz ≤ LVDS_CLK < 87.5 MHz 011 – 87.5 MHz ≤ LVDS_CLK < 112.5 MHz 100 – 112.5 MHz ≤ LVDS_CLK < 137.5 MHz 101 – 137.5 MHz ≤ LVDS_CLK ≤ 154 MHz (default) 110 – Reserved 111 – Reserved	101	RW
	0	HS_CLK_SRC 0 – LVDS pixel clock derived from input REFCLK (default) 1 – LVDS pixel clock derived from MIPI D-PHY channel A HS continuous clock	0	RW
0x0B	7:3	DSI_CLK_DIVIDER When CSR 0x0A.0 = 1, this field controls the divider used to generate the LVDS output clock from the MIPI D-PHY Channel A HS continuous clock. When CSR 0x0A.0 = 0, this field must be programmed to 00000. 00000 – LVDS clock = source clock (default) 00001 – Divide by 2 00010 – Divide by 3 00011 – Divide by 4 • • • 10111 – Divide by 24 11000 – Divide by 25 11001 through 11111 – Reserved	00000	RW
	1:0	REFCLK_MULTIPLIER When CSR 0x0A.0 = 0, this field controls the multiplier used to generate the LVDS output clock from the input REFCLK. When CSR 0x0A.0 = 1, this field must be programmed to 00. 00 – LVDS clock = source clock (default) 01 – Multiply by 2 10 – Multiply by 3 11 – Multiply by 4	00	RW

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Table 7-8. CSR Bit Field Definitions – Reset and Clock Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x0D	0	PLL_EN When this bit is set, the PLL is enabled with the settings programmed into CSR 0x0A and CSR 0x0B. The PLL should be disabled before changing any of the settings in CSR 0x0A and CSR 0x0B. The input clock source must be active and stable before the PLL is enabled. 0 – PLL disabled (default) 1 – PLL enabled	0	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write 1 to Clear; WO = Write Only (reads return undetermined values)

Table 7-9. CSR Bit Field Definitions – DSI Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x10	7	LEFT_RIGHT_PIXELS This bit selects the pixel arrangement in dual channel DSI implementations. 0 – DSI channel A receives ODD pixels and channel B receives EVEN (default) 1 – DSI channel A receives LEFT image pixels and channel B receives RIGHT image pixels	0	RW
	6:5	DSI_CHANNEL_MODE 00 – Dual-channel DSI receiver 01 – Single channel DSI receiver (default) 10 – Two single channel DSI receivers 11 – Reserved	01	RW
	4:3	CHA_DSI_LANES This field controls the number of lanes that are enabled for DSI Channel A. 00 – Four lanes are enabled 01 – Three lanes are enabled 10 – Two lanes are enabled 11 – One lane is enabled (default) Note: Unused DSI input pins on the SN65DSI85 should be left unconnected.	11	RW
	2:1	CHB_DSI_LANES This field controls the number of lanes that are enabled for DSI Channel B. 00 – Four lanes are enabled 01 – Three lanes are enabled 10 – Two lanes are enabled 11 – One lane is enabled (default) Note: Unused DSI input pins on the SN65DSI85 should be left unconnected.	11	RW
	0	SOT_ERR_TOL_DIS 0 – Single bit errors are tolerated for the start of transaction SoT leader sequence (default) 1 – No SoT bit errors are tolerated	0	RW
0x11	7:6	CHA_DSI_DATA_EQ This field controls the equalization for the DSI Channel A Data Lanes 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization	00	RW
	5:4	CHB_DSI_DATA_EQ This field controls the equalization for the DSI Channel B Data Lanes 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization	00	RW
	3:2	CHA_DSI_CLK_EQ This field controls the equalization for the DSI Channel A Clock 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization	00	RW

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Table 7-9. CSR Bit Field Definitions – DSI Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
	1:0	CHB_DSI_CLK_EQ This field controls the equalization for the DSI Channel A Clock 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization	00	RW
0x12	7:0	CHA_DSI_CLK_RANGE This field specifies the DSI Clock frequency range in 5 MHz increments for the DSI Channel A Clock 0x00 through 0x07 – Reserved 0x08 – 40 ≤ frequency < 45 MHz 0x09 – 45 ≤ frequency < 50 MHz • • • 0x63 – 495 ≤ frequency < 500 MHz 0x64 – 500 MHz 0x65 through 0xFF – Reserved	0	RW
0x13	7:0	CHB_DSI_CLK_RANGE This field specifies the DSI Clock frequency range in 5 MHz increments for the DSI Channel B Clock 0x00 through 0x07 – Reserved 0x08 – 40 ≤ frequency < 45 MHz 0x09 – 45 ≤ frequency < 50 MHz • • • 0x63 – 495 ≤ frequency < 500 MHz 0x64 – 500 MHz 0x65 through 0xFF – Reserved	0	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write 1 to Clear; WO = Write Only (reads return undetermined values)

Table 7-10. CSR Bit Field Definitions – LVDS Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x18	7	DE_NEG_POLARITY 0 – DE is positive polarity driven 1 during active pixel transmission on LVDS (default) 1 – DE is negative polarity driven 0 during active pixel transmission on LVDS	0	RW
	6	HS_NEG_POLARITY 0 – HS is positive polarity driven 1 during corresponding sync conditions 1 – HS is negative polarity driven 0 during corresponding sync (default)	1	RW
	5	VS_NEG_POLARITY 0 – VS is positive polarity driven 1 during corresponding sync conditions 1 – VS is negative polarity driven 0 during corresponding sync (default)	1	RW
	4	LVDS_LINK_CFG 0 – LVDS Channel A and Channel B outputs enabled When CSR 0x10.6:5 = 00 or 01, the LVDS is in Dual-Link configuration When CSR 0x10.6:5 = 10, the LVDS is in two Single-Link configuration 1 – LVDS Single-Link configuration; Channel A output enabled and Channel B output disabled (default)	1	RW
	3	CHA_24BPP_MODE 0 – Force 18bpp; LVDS channel A lane 4 (A_Y3P/N) is disabled (default) 1 – Force 24bpp; LVDS channel A lane 4 (B_Y3P/N) is enabled	0	RW
	2	CHB_24BPP_MODE 0 – Force 18bpp; LVDS channel B lane 4 (A_Y3P/N) is disabled (default) 1 – Force 24bpp; LVDS channel B lane 4 (B_Y3P/N) is enabled	0	RW

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Table 7-10. CSR Bit Field Definitions – LVDS Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
	1	CHA_24BPP_FORMAT1 This field selects the 24bpp data format 0 – LVDS channel A lane A_Y3P/N transmits the 2 most significant bits (MSB) per color; Format 2 (default) 1 – LVDS channel B lane A_Y3P/N transmits the 2 least significant bits (LSB) per color; Format 1 Note1: This field must be 0 when 18bpp data is received from DSI. Note2: If this field is set to 1 and CHA_24BPP_MODE is 0, the SN65DSI85 will convert 24bpp data to 18bpp data for transmission to an 18bpp panel. In this configuration, the SN65DSI85 will not transmit the 2 LSB per color on LVDS channel A, since LVDS channel A lane A_Y3P/N is disabled.	0	RW
	0	CHB_24BPP_FORMAT1 This field selects the 24bpp data format 0 – LVDS channel B lane B_Y3P/N transmits the 2 most significant bits (MSB) per color; Format 2 (default) 1 – LVDS channel B lane B_Y3P/N transmits the 2 least significant bits (LSB) per color; Format 1 Note1: This field must be 0 when 18bpp data is received from DSI. Note2: If this field is set to 1 and CHB_24BPP_MODE is 0, the SN65DSI85 will convert 24bpp data to 18bpp data for transmission to an 18bpp panel. In this configuration, the SN65DSI85 will not transmit the 2 LSB per color on LVDS channel B, since LVDS channel B lane B_Y3P/N is disabled.	0	RW
0x19	6	CHA_LVDS_VOCM This field controls the common mode output voltage for LVDS Channel A 0 – 1.2V (default) 1 – 0.9V (CSR 0x1B.5:4 CHA_LVDS_CM_ADJUST must be set to 01b)	0	RW
	4	CHB_LVDS_VOCM This field controls the common mode output voltage for LVDS Channel B 0 – 1.2V (default) 1 – 0.9V (CSR 0x1B.1:0 CHB_LVDS_CM_ADJUST must be set to 01b)	0	RW
	3:2	CHA_LVDS_VOD_SWING This field controls the differential output voltage for LVDS Channel A. See the *Section 6.5* for $\|V_{OD}\|$ for each setting: 00, 01 (default), 10, 11	01	RW
	1:0	CHB_LVDS_VOD_SWING This field controls the differential output voltage for LVDS Channel B. See the *Section 6.5* for $\|V_{OD}\|$ for each setting: 00, 01 (default), 10, 11	01	RW
0x1A	6	EVEN_ODD_SWAP 0 – Odd pixels routed to LVDS Channel A and Even pixels routed to LVDS Channel B (default) 1 – Odd pixels routed to LVDS Channel B and Even pixels routed to LVDS Channel A Note: When the SN65DSI85 is in two stream mode (CSR 0x10.6:5 = 10), setting this bit to 1 will cause the video stream from DSI Channel A to be routed to LVDS Channel B and the video stream from DSI Channel B to be routed to LVDS Channel A.	0	RW

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Table 7-10. CSR Bit Field Definitions – LVDS Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
	5	CHA_REVERSE_LVDS This bit controls the order of the LVDS pins for Channel A. 0 – Normal LVDS Channel A pin order. LVDS Channel A pin order is the same as listed in the Terminal Assignments Section. (default) 1 – Reversed LVDS Channel A pin order. LVDS Channel A pin order is remapped as follows: • A_Y0P → A_Y3P • A_Y0N → A_Y3N • A_Y1P → A_CLKP • A_Y1N → A_CLKN • A_Y2P → A_Y2P • A_Y2N → A_Y2N • A_CLKP → A_Y1P • A_CLKN → A_Y1N • A_Y3P → A_Y0P • A_Y3N → A_Y0N	0	RW
	4	CHB_REVERSE_LVDS This bit controls the order of the LVDS pins for Channel B. 0 – Normal LVDS Channel B pin order. LVDS Channel B pin order is the same as listed in the Terminal Assignments Section. (default) 1 – Reversed LVDS Channel B pin order. LVDS Channel B pin order is remapped as follows: • B_Y0P → B_Y3P • B_Y0N → B_Y3N • B_Y1P → B_CLKP • B_Y1N → B_CLKN • B_Y2P → B_Y2P • B_Y2N → B_Y2N • B_CLKP → B_Y1P • B_CLKN → B_Y1N • B_Y3P → B_Y0P • B_Y3N → B_Y0N	0	RW
	1	CHA_LVDS_TERM This bit controls the near end differential termination for LVDS Channel A. This bit also affects the output voltage for LVDS Channel A. 0 – 100Ω differential termination 1 – 200Ω differential termination (default)	1	RW
	0	CHB_LVDS_TERM This bit controls the near end differential termination for LVDS Channel B. This bit also affects the output voltage for LVDS Channel B. 0 – 100Ω differential termination 1 – 200Ω differential termination (default)	1	RW
0x1B	5:4	CHA_LVDS_CM_ADJUST This field can be used to adjust the common mode output voltage for LVDS Channel A. 00 – No change to common mode voltage (default) 01 – Adjust common mode voltage down 3% 10 – Adjust common mode voltage up 3% 11 – Adjust common mode voltage up 6%	00	RW
	1:0	CHB_LVDS_CM_ADJUST This field can be used to adjust the common mode output voltage for LVDS Channel B. 00 – No change to common mode voltage (default) 01 – Adjust common mode voltage down 3% 10 – Adjust common mode voltage up 3% 11 – Adjust common mode voltage up 6%	00	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write 1 to Clear; WO = Write Only (reads return undetermined values)

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Notes:

1. TEST PATTERN GENERATION PURPOSE ONLY registers are for test pattern generation use only. Others are for normal operation unless the test pattern generation feature is enabled. CHB* registers are used only when the device is configured for two stream mode -both LVDS output channels are enabled(CSR 0x18.4=0) and DSI channel mode configured as two stream(CSR 0x10.6:5 = 0X10b). CH*_SYNC_DELAY_HIGH/LOW registers are not used for test pattern generation. In all other configurations, CHA* registers are used for test pattern generation.
2. The CHB* register fields with a note “This field is only applicable when CSR 0x10.6:5 = 10.” are used only when the device is configured as two stream mode with CSR 0x18.4=’0’ and CSR 0x10.6:5 = 10.

Table 7-11. CSR Bit Field Definitions – Video Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x20	7:0	CHA_ACTIVE_LINE_LENGTH_LOW When the SN65DSI85 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line. When configured for Dual DSI inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI Channel A and output to LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0) with DSI_CHANNEL_MODE set to 01 or 00(CSR 0x10.6:5) . When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI Channel A and output to LVDS Channel A. When configured for Dual DSI inputs in two stream mode, this field controls the number of pixels in the active horizontal line for the video stream received on DSI Channel A and output to LVDS Channel A. The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length. Note: When the SN65DSI85 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.	0	RW
0x21	3:0	CHA_ACTIVE_LINE_LENGTH_HIGH When the SN65DSI85 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line. When configured for Dual DSI inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI Channel A and output to LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0) with DSI_CHANNEL_MODE set to 01 or 00(CSR 0x10.6:5). When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI Channel A and output to LVDS Channel A. When configured for Dual DSI inputs in two stream mode, this field controls the number of pixels in the active horizontal line for the video stream received on DSI Channel A and output to LVDS Channel A. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. Note: When the SN65DSI85 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.	0	RW

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Table 7-11. CSR Bit Field Definitions – Video Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x22	7:0	CHB_ACTIVE_LINE_LENGTH_LOW When the SN65DSI85 is configured for a single DSI input, this field is not applicable. When configured for Dual DSI inputs in Odd/Even mode, this field controls the number of even pixels in the active horizontal line that are received on DSI Channel B. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of right pixels in the active horizontal line that are received on DSI Channel B and output to LVDS Channel B. When configured for Dual DSI inputs in two stream mode, this field controls the number of pixels in the active horizontal line for the video stream received on DSI Channel B and output to LVDS Channel B. The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length. Note: When the SN65DSI85 is configured for dual DSI inputs in Left/Right mode and RIGHT_CROP field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied.	0	RW
0x23	3:0	CHB_ACTIVE_LINE_LENGTH_HIGH When the SN65DSI85 is configured for a single DSI input, this field is not applicable. When configured for Dual DSI inputs in Odd/Even mode, this field controls the number of even pixels in the active horizontal line that are received on DSI Channel B. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of right pixels in the active horizontal line that are received on DSI Channel B and output to LVDS Channel B. When configured for Dual DSI inputs in two stream mode, this field controls the number of pixels in the active horizontal line for the video stream received on DSI Channel B and output to LVDS Channel B. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. Note: When the SN65DSI85 is configured for dual DSI inputs in Left/Right mode and RIGHT_CROP field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied	0	RW
0x24	7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW TEST PATTERN GENERATION PURPOSE ONLY This field controls the vertical display size in lines for LVDS Channel A/B test pattern generation. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size.	0	RW
0x25	3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines forLVDS Channel A/B test pattern generation. The value in this field is the upper 4 bits of the 12-bit value for the vertical display size	0	RW
0x26	7:0	CHB_VERTICAL_DISPLAY_SIZE_LOW TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS Channel B test pattern generation. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size. This field is only applicable when CSR 0x10.6:5 = 10	0	RW
0x27	3:0	CHB_VERTICAL_DISPLAY_SIZE_HIGH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS Channel B test pattern generation. The value in this field is the upper 4 bits of the 12-bit value for the vertical display size. This field is only applicable when CSR 0x10.6:5 = 10 .	0	RW

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Table 7-11. CSR Bit Field Definitions – Video Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x28	7:0	CHA_SYNC_DELAY_LOW This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0) with DSI_CHANNEL_MODE set to 01 or 00(CSR 0x10.6:5).. The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI85. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the lower 8 bits of the 12-bit value for the Sync delay.	0	RW
0x29	3:0	CHA_SYNC_DELAY_HIGH This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0) with DSI_CHANNEL_MODE set to 01 or 00(CSR 0x10.6:5).. The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI85. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the upper 4 bits of the 12-bit value for the Sync delay.	0	RW
0x2A	7:0	CHB_SYNC_DELAY_LOW This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel B when the SN65DSI85 is configured as two single stream mode with CSR 0x18.4=0 and CSR 0x10.6:5 = 10. The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI85. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the lower 8 bits of the 12-bit value for the Sync delay	0	RW
0x2B	3:0	CHB_SYNC_DELAY_HIGH This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel B when the SN65DSI85 is configured as two single stream mode with CSR 0x18.4=0 and CSR 0x10.6:5 = 10. The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI85. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the upper 4 bits of the 12-bit value for the Sync delay.	0	RW
0x2C	7:0	CHA_HSYNC_PULSE_WIDTH_LOW This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0) with DSI_CHANNEL_MODE set to 01 or 00(CSR 0x10.6:5). The value in this field is the lower 8 bits of the 10-bit value for the HSync Pulse Width.	0	RW
0x2D	1:0	CHA_HSYNC_PULSE_WIDTH_HIGH This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0) with DSI_CHANNEL_MODE set to 01 or 00(CSR 0x10.6:5). The value in this field is the upper 2 bits of the 10-bit value for the HSync Pulse Width.	0	RW
0x2E	7:0	CHB_HSYNC_PULSE_WIDTH_LOW This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel B. The value in this field is the lower 8 bits of the 10-bit value for the HSync Pulse Width. This field is only applicable when CSR 0x10.6:5 = 10.	0	RW
0x2F	1:0	CHB_HSYNC_PULSE_WIDTH_HIGH This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel B. The value in this field is the upper 2 bits of the 10-bit value for the HSync Pulse Width. This field is only applicable when CSR 0x10.6:5 = 10.	0	RW

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Table 7-11. CSR Bit Field Definitions – Video Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x30	7:0	CHA_VSYNC_PULSE_WIDTH_LOW This field controls the length in lines of the VSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0) with DSI_CHANNEL_MODE set to 01 or 00(CSR 0x10.6:5). The value in this field is the lower 8 bits of the 10-bit value for the VSync Pulse Width.	0	RW
0x31	1:0	CHA_VSYNC_PULSE_WIDTH_HIGH This field controls the length in lines of the VSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0) with DSI_CHANNEL_MODE set to 01 or 00(CSR 0x10.6:5). The value in this field is the upper 2 bits of the 10-bit value for the VSync Pulse Width.	0	RW
0x32	7:0	CHB_VSYNC_PULSE_WIDTH_LOW This field controls the length in lines of the VSync Pulse Width for LVDS Channel B. The value in this field is the lower 8 bits of the 10-bit value for the VSync Pulse Width. This field is only applicable when CSR 0x10.6:5 = 10.	0	RW
0x33	1:0	CHB_VSYNC_PULSE_WIDTH_HIGH This field controls the length in lines of the VSync Pulse Width for LVDS Channel B. The value in this field is the upper 2 bits of the 10-bit value for the VSync Pulse Width. This field is only applicable when CSR 0x10.6:5 = 10.	0	RW
0x34	7:0	CHA_HORIZONTAL_BACK_PORCH This field controls the time in pixel clocks between the end of the HSync Pulse and the start of the active video data for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0) with DSI_CHANNEL_MODE set to 01 or 00(CSR 0x10.6:5).	0	RW
0x35	7:0	CHB_HORIZONTAL_BACK_PORCH This field controls the time in pixel clocks between the end of the HSync Pulse and the start of the active video data for LVDS Channel B. This field is only applicable when CSR 0x10.6:5 = 10.	0	RW
0x36	7:0	CHA_VERTICAL_BACK_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the VSync Pulse and the start of the active video data for Channel A/B.	0	RW
0x37	7:0	CHB_VERTICAL_BACK_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the VSync Pulse and the start of the active video data for Channel B. This field is only applicable when CSR 0x10.6:5 = 10 .	0	RW
0x38	7:0	CHA_HORIZONTAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the time in pixel clocks between the end of the active video data and the start of the HSync Pulse for Channel A/B.	0	RW
0x39	7:0	CHB_HORIZONTAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the time in pixel clocks between the end of the active video data and the start of the HSync Pulse for Channel B. This field is only applicable when CSR 0x10.6:5 = 10.	0	RW
0x3A	7:0	CHA_VERTICAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the active video data and the start of the VSync Pulse for Channel A/B.	0	RW
0x3B	7:0	CHB_VERTICAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the active video data and the start of the VSync Pulse for Channel B. This field is only applicable when CSR 0x10.6:5 = 10.	0	RW

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Table 7-11. CSR Bit Field Definitions – Video Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x3C	4	CHA_TEST_PATTERN TEST PATTERN GENERATION PURPOSE ONLY. When this bit is set, the SN65DSI85 will generate a video test pattern for Channel A based on the values programmed into the Video Registers for Channel A	0	RW
	0	CHB_TEST_PATTERN TEST PATTERN GENERATION PURPOSE ONLY. When this bit is set, the SN65DSI85 will generate a video test pattern for Channel B based on the values programmed into the Video Registers for Channel B. This field is only applicable when CSR 0x10.6:5 = 10	0	RW
0x3D	7:0	RIGHT_CROP This field controls the number of pixels removed from the beginning of the active video line for DSI Channel B. This field only has meaning if LEFT_RIGHT_PIXELS = 1. This field defaults to 0x00. Note1: When the SN65DSI85 is configured for dual DSI inputs in Left/Right mode and this field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied.	0	RW
0x3E	7:0	LEFT_CROP This field controls the number of pixels removed from the end of the active video line for DSI Channel A. This field only has meaning if LEFT_RIGHT_PIXELS = 1. This field defaults to 0x00. Note1: When the SN65DSI85 is configured for dual DSI inputs in Left/Right mode and this field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.	0	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write 1 to Clear; WO = Write Only (reads return undetermined values)

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Table 7-12. CSR Bit Field Definitions – IRQ Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0xE0	0	IRQ_EN When enabled by this field, the IRQ output is driven high to communicate IRQ events. 0 – IRQ output is high-impedance (default) 1 – IRQ output is driven high when a bit is set in registers 0xE5 or 0xE6 that also has the corresponding IRQ_EN bit set to enable the interrupt condition	0	RW
0xE1	7	CHA_SYNCH_ERR_EN 0 – CHA_SYNCH_ERR is masked 1 – CHA_SYNCH_ERR is enabled to generate IRQ events	0	RW
	6	CHA_CRC_ERR_EN 0 – CHA_CRC_ERR is masked 1 – CHA_CRC_ERR is enabled to generate IRQ events	0	RW
	5	CHA_UNC_ECC_ERR_EN 0 – CHA_UNC_ECC_ERR is masked 1 – CHA_UNC_ECC_ERR is enabled to generate IRQ events	0	RW
	4	CHA_COR_ECC_ERR_EN 0 – CHA_COR_ECC_ERR is masked 1 – CHA_COR_ECC_ERR is enabled to generate IRQ events	0	RW
	3	CHA_LLP_ERR_EN 0 – CHA_LLP_ERR is masked 1 – CHA_ LLP_ERR is enabled to generate IRQ events	0	RW
	2	CHA_SOT_BIT_ERR_EN 0 – CHA_SOT_BIT_ERR is masked 1 – CHA_SOT_BIT_ERR is enabled to generate IRQ events	0	RW
	0	PLL_UNLOCK_EN 0 – PLL_UNLOCK is masked 1 – PLL_UNLOCK is enabled to generate IRQ events	0	RW
0xE2	7	CHB_SYNCH_ERR_EN 0 – CHB_SYNCH_ERR is masked 1 – CHB_SYNCH_ERR is enabled to generate IRQ events	0	RW
	6	CHB_CRC_ERR_EN 0 – CHB_CRC_ERR is masked 1 – CHB_CRC_ERR is enabled to generate IRQ events	0	RW
	5	CHB_UNC_ECC_ERR_EN 0 – CHB_UNC_ECC_ERR is masked 1 – CHB_UNC_ECC_ERR is enabled to generate IRQ events	0	RW
	4	CHB_COR_ECC_ERR_EN 0 – CHB_COR_ECC_ERR is masked 1 – CHB_COR_ECC_ERR is enabled to generate IRQ events	0	RW
	3	CHB_LLP_ERR_EN 0 – CHB_LLP_ERR is masked 1 – CHB_ LLP_ERR is enabled to generate IRQ events	0	RW
	2	CHB_SOT_BIT_ERR_EN 0 – CHB_SOT_BIT_ERR is masked 1 – CHB_SOT_BIT_ERR is enabled to generate IRQ events	0	RW
0xE5	7	CHA_SYNCH_ERR When the DSI channel A packet processor detects an HS or VS synchronization error, that is, an unexpected sync packet; this bit is set; this bit is cleared by writing a 1 value.	0	RW1C
	6	CHA_CRC_ERR When the DSI channel A packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a 1 value.	0	RW1C
	5	CHA_UNC_ECC_ERR When the DSI channel A packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a 1 value.	0	RW1C
	4	CHA_COR_ECC_ERR When the DSI channel A packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a 1 value.	0	RW1C

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Table 7-12. CSR Bit Field Definitions – IRQ Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
	3	CHA_LLP_ERR When the DSI channel A packet processor detects a low level protocol error, this bit is set; this bit is cleared by writing a 1 value. Low level protocol errors include SoT and EoT sync errors, Escape Mode entry command errors, LP transmission sync errors, and false control errors. Lane merge errors are reported by this status condition.	0	RW1C
	2	CHA_SOT_BIT_ERR When the DSI channel A packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a 1 value.	0	RW1C
	0	PLL_UNLOCK This bit is set whenever the PLL Lock status transitions from LOCK to UNLOCK.	1	RW1C
0xE6	7	CHB_SYNCH_ERR When the DSI channel B packet processor detects an HS or VS synchronization error, that is, an unexpected sync packet; this bit is set; this bit is cleared by writing a 1 value.	0	RW1C
	6	CHB_CRC_ERR When the DSI channel B packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a 1 value.	0	RW1C
	5	CHB_UNC_ECC_ERR When the DSI channel B packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a 1 value.	0	RW1C
	4	CHB_COR_ECC_ERR When the DSI channel B packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a 1 value.	0	RW1C
	3	CHB_LLP_ERR When the DSI channel B packet processor detects a low level protocol error, this bit is set; this bit is cleared by writing a 1 value. Low level protocol errors include SoT and EoT sync errors, Escape Mode entry command errors, LP transmission sync errors, and false control errors. Lane merge errors are reported by this status condition.	0	RW1C
	2	CHB_SOT_BIT_ERR When the DSI channel B packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a 1 value.	0	RW1C

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write 1 to Clear; WO = Write Only (reads return undetermined values)

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Video STOP and Restart Sequence

When the system requires to stop outputting video to the display, it is recommended to use the following sequence for the SN65DSI85:

1. Clear the PLL_EN bit to 0 (CSR 0x0D.0)
2. Stop video streaming on DSI inputs
3. Drive all DSI data lanes to LP11, but keep the DSI CLK lanes in HS.

When the system is ready to restart the video streaming.

1. Start video streaming on DSI inputs.
2. Set the PLL_EN bit to 1 (CSR 0x0D.0).
3. Wait for a minimum of 3 ms.
4. Set the SOFT_RESET bit (0x09.0).

8.1.2 Reverse LVDS Pin Order Option

For ease of PCB routing, the SN65DSI85 supports swapping/reversing the channel or pin order via configuration register programming. The order of the LVDS pin for LVDS Channel A or Channel B can be reversed by setting the address 0x1A bit 5 CHA_REVERSE_LVDS or bit 4 CHB_REVERSE_LVDS. The LVDS Channel A and Channel B can be swapped by setting the 0x1A.6 EVEN_ODD_SWAP bit. See the corresponding register bit definition for details.

8.1.3 IRQ Usage

The SN65DSI85 provides an IRQ pin that can be used to indicate when certain errors occur on DSI. The IRQ output is enabled through the IRQ_EN bit (CSR 0xE0.0). Individual error conditions for DSI Channel A are enabled through the Channel A Error Enable bits (CSR 0xE1.7:2). Individual error conditions for DSI Channel B are enabled through the Channel B Error Enable bits (CSR 0xE2.7:2). The IRQ pin will be asserted when an error occurs on DSI, the corresponding error enable bit is set, and the IRQ_EN bit is set. An error is cleared by writing a 1 to the corresponding error status bit.

Note

If the SOFT_RESET bit is set while the DSI video stream is active, some of the error status bits may be set.

If the DSI video stream is stopped, some of the error status bits may be set. These error status bits should be cleared before restarting the video stream.

If the DSI video stream starts before the device is configured, some of the error status bits may be set. It is recommended to start streaming after the device is correctly configured as recommended in the initialization sequence in the *Recommended Initialization Sequence* section.

8.2 Typical Applications

8.2.1 Typical WUXGA 18-bpp Application

Figure 8-1 illustrates a typical application using the SN65DSI85 configured for a single channel DSI receiver to interface a single-channel DSI application processor to an LVDS Dual-Link 18 bit-per-pixel panel supporting 1920 x 1200 WUXGA resolutions at 60 frames per second.

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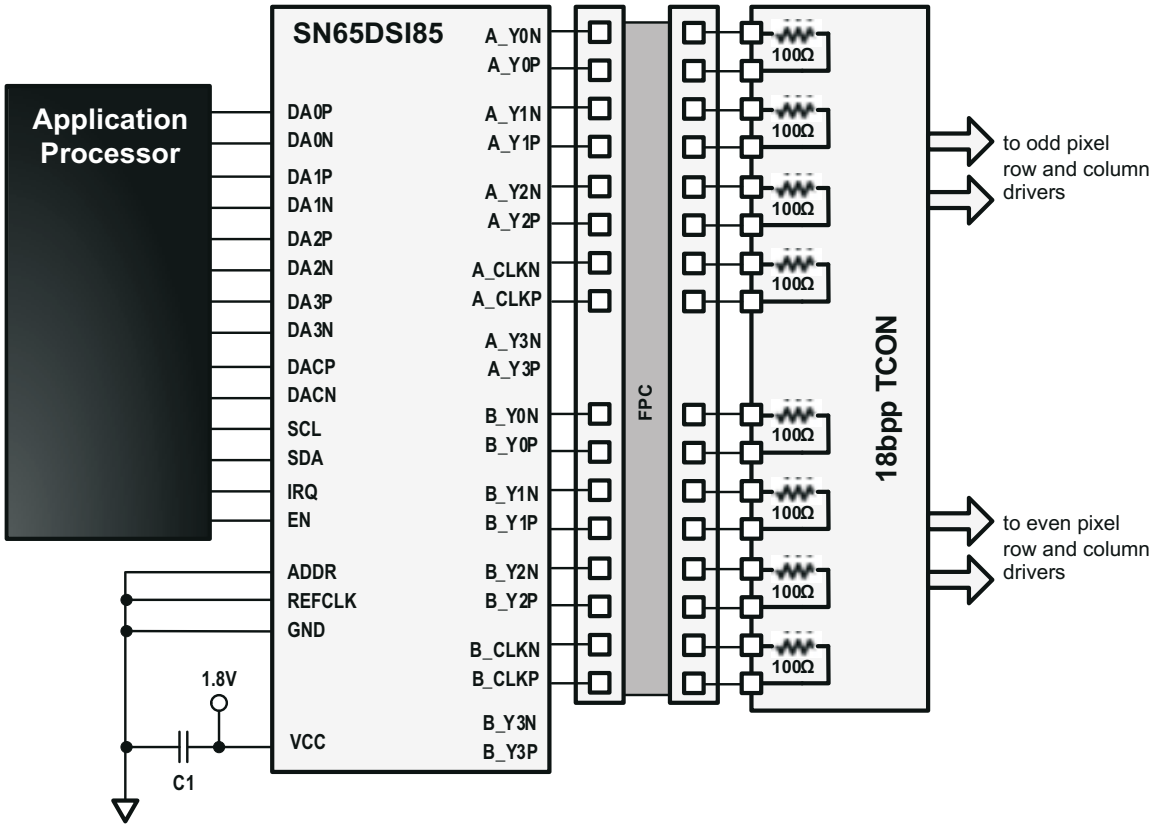

Figure 8-1. Typical WUXGA 18-bpp Panel Application

8.2.1.1 Design Requirements

Table 8-1 lists the design parameters for SN65DSI85.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC}	1.8 V (±5%)
CLOCK	DSIA_CLK
REFCKL Frequency	N/A
DSIA Clock Frequency	490 MHz
PANEL INFORMATION	
LVDS Output Clock Frequency	81 MHz
Resolution	1920 × 1200
Horizontal Active (pixels)	960
Horizontal Blanking (pixels)	144
Vertical Active (Lines)	1200
Vertical Blanking (lines)	20
Horizontal Sync Offset (pixels)	50
Horizontal Sync Pulse Width (pixels)	50
Vertical Sync Offset (lines)	1
Vertical Sync Pulse Width (lines)	5
Horizontal Sync Pulse Polarity	Negative
Vertical Sync Pulse Polarity	Negative
Color Bit Depth (6 bpc or 8 bpc)	6-bit

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Table 8-1. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Number of LVDS Lanes	2 × [3 Data lanes + 1 Clock lane]
DSI INFORMATION	
Number of DSI Lanes	1 × [4 Data Lanes + 1 Clock Lane]
DSI Input Clock Frequency	490 MHz
Dual DSI Configuration (Odd/Even or Left/Right)	N/A

8.2.1.2 Detailed Design Procedure

The video resolution parameters required by the panel need to be programmed into the SN65DSI84. For this example, the parameters programmed would be the following:

Horizontal active = 1920 or 0x780
CHA_ACTIVE_LINE_LENGTH_LOW = 0X80
CHA_ACTIVE_LINE_LENGTH_HIGH = 0x07

Horizontal pulse Width = 50 or 0x32
CHA_HSYNC_PULSE_WIDTH_LOW = 0x32
CHA_HSYNC_PULSE_WIDTH_HIGH= 0x00

Horizontal back porch = Horizontal blanking – (Horizontal sync offset + Horizontal sync pulse width)
Horizontal back porch = 144– (50 + 50)
Horizontal back porch = 44 or 0x2C
CHA_HORIZONTAL_BACK_PORCH = 0x2C

Vertical pulse width = 5
CHA_VSYNC_PULSE_WIDTH_LOW = 0x05
CHA_VSYNC_PULSE_WIDTH_HIGH= 0x00

The pattern generation feature can be enabled by setting the CHA_TEST_PATTERN bit at address 0x3C and configuring the following TEST PATTERN GENERATION PURPOSE ONLY registers.

Vertical active = 1200 or 0x4B0
CHA_VERTICAL_DISPLAY_SIZE_LOW = 0xB0
CHA_VERTICAL_DISPLAY_SIZE_HIGH = 0x04

Vertical back porch = Vertical blanking – (Vertical sync offset +Vertical sync pulse width)
Vertical back porch = 20 – (1 + 5)
Vertical back porch = 14 or 0x0E
CHA_VERTICAL_BACK_PORCH = 0x0E

Horizontal front porch = Horizontal sync offset
Horizontal front porch = 50 or 0x32
CHA_HORIZONTAL_FRONT_PORCH = 0x32

Vertical front porch = Vertical sync offset
Vertical front porch =1
CHA_VERTICAL_FRONT_PORCH = 0x01

In this example, the clock source for the SN65DSI84 is the DSI clock. When the MIPI D-PHY clock is used as the LVDS clock source, it is divided by the factor in DSI_CLK_DIVIDER (CSR 0x0B.7:3) to generate the FlatLink LVDS output clock. Additionally, LVDS_CLK_RANGE (CSR 0x0A.3:1) and CH_DSI_CLK_RANGE(CSR 0x12) must be set to the frequency range of the FlatLink LVDS output clock and DSI Channel A input clock respectively for the internal PLL to operate correctly. After these settings are programmed, PLL_EN (CSR 0x0D.0) should be set to enable the internal PLL.

LVDS_CLK)RANGE = 010b – 62.5 MHz ≤ LVDS_CLK < 87.5 MHz
HS_CLK_SRC = 1 – LVDS pixel clock derived from MIPI D-PHY channel A HS continuous clock
DSI_CLK_DIVIDER = 00101b – Divide by 6
CHA_DSI_LANES = 00 – Four lanes are enabled
CHA_DSI_CLK_RANGE = 0x62 – 490 MHz ≤ frequency < 495 MHz

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8.2.1.2.1 Example Script

```
<aardvark>
  <configure i2c="1" spi="1" gpio="0" tpower="1" pullups="1" />
  <i2c_bitrate khz="100" />
```

```
=====SOFTRESET=======
  <i2c_write addr="0x2D" count="1" radix="16">09 01</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 0D======= ======PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured======
  <i2c_write addr="0x2D" count="1" radix="16">0D 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 0A======= ======HS_CLK_SRC bit0=== ======LVDS_CLK_Range bit 3:1======
  <i2c_write addr="0x2D" count="1" radix="16">0A 05</i2c_write>
  <sleep ms="10" />
```

```
======ADDR  0B=======  ======DSI_CLK_DIVIDER  bit7:3=====  ======RefCLK  multiplier(bit1:0)======
======00 - LVDSclk=source clk, 01 - x2, 10 -x3, 11 - x4======
  <i2c_write addr="0x2D" count="1" radix="16">0B 28</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 10======= ======DSI Ch Confg Left_Right Pixels(bit7 - 0 for A ODD, B EVEN, 1 for the
other config)====== ======DSI Ch Mode(bit6:5) 00 - Dual, 01 - single, 10 - two single =======
======CHA_DSI_Lanes(bit4:3), CHB_DSI_Lanes(bit2:1), 00 - 4, 01 - 3, 10 - 2, 11 - 1
======SOT_ERR_TOL_DIS(bit0)=======
  <i2c_write addr="0x2D" count="1" radix="16">10 26</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 12=======
  <i2c_write addr="0x2D" count="1" radix="16">12 62</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 18======= ======bit7: DE_Pol, bit6:HS_Pol, bit5:VS_Pol, bit4: LVDS Link Cfg, bit3:CHA
24bpp, bit2: CHB 24bpp, bit1: CHA 24bpp fmt1, bit0: CHB 24bpp fmt1======
```

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```
  <i2c_write addr="0x2D" count="1" radix="16">18 63</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 19=======
  <i2c_write addr="0x2D" count="1" radix="16">19 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 1A=======
  <i2c_write addr="0x2D" count="1" radix="16">1A 03</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 20======= ======CHA_LINE_LENGTH_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">20 80</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 21======= ======CHA_LINE_LENGTH_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">21 07</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 22======= ======CHB_LINE_LENGTH_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">22 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 23======= ======CHB_LINE_LENGTH_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">23 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 24======= ======CHA_VERTICAL_DISPLAY_SIZE_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">24 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 25======= ======CHA_VERTICAL_DISPLAY_SIZE_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">25 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 26======= ======CHB_VERTICAL_DISPLAY_SIZE_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">26 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 27======= ======CHB_VERTICAL_DISPLAY_SIZE_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">27 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 28======= ======CHA_SYNC_DELAY_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">28 20</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 29======= ======CHA_SYNC_DELAY_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">29 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 2A======= ======CHB_SYNC_DELAY_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">2A 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 2B======= ======CHB_SYNC_DELAY_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">2B 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 2C======= ======CHA_HSYNC_PULSE_WIDTH_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">2C 32</i2c_write>
  <sleep ms="10" />
```

```
 ======ADDR 2D======= ======CHA_HSYNC_PULSE_WIDTH_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">2D 00</i2c_write>
  <sleep ms="10" />
```

```
 ======ADDR 2E======= ======CHB_HSYNC_PULSE_WIDTH_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">2E 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 2F======= ======CHB_HSYNC_PULSE_WIDTH_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">2F 00</i2c_write>
```


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```
  <sleep ms="10" />
```

```
======ADDR 30======= ======CHA_VSYNC_PULSE_WIDTH_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">30 05</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 31======= ======CHA_VSYNC_PULSE_WIDTH_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">31 00</i2c_write>
  <sleep ms="10" />
```

```
 ======ADDR 32======= ======CHB_VSYNC_PULSE_WIDTH_LOW========
  <i2c_write addr="0x2D" count="1" radix="16">32 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 33======= ======CHB_VSYNC_PULSE_WIDTH_HIGH========
  <i2c_write addr="0x2D" count="1" radix="16">33 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 34======= ======CHA_HOR_BACK_PORCH========
  <i2c_write addr="0x2D" count="1" radix="16">34 2C</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 35======= ======CHB_HOR_BACK_PORCH========
  <i2c_write addr="0x2D" count="1" radix="16">35 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 36======= ======CHA_VER_BACK_PORCH========
  <i2c_write addr="0x2D" count="1" radix="16">36 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 37======= ======CHB_VER_BACK_PORCH========
  <i2c_write addr="0x2D" count="1" radix="16">37 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 38======= ======CHA_HOR_FRONT_PORCH========
  <i2c_write addr="0x2D" count="1" radix="16">38 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 39======= ======CHB_HOR_FRONT_PORCH========
  <i2c_write addr="0x2D" count="1" radix="16">39 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 3A======= ======CHA_VER_FRONT_PORCH========
  <i2c_write addr="0x2D" count="1" radix="16">3A 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 3B======= ======CHB_VER_FRONT_PORCH========
  <i2c_write addr="0x2D" count="1" radix="16">3B 00</i2c_write>
  <sleep ms="10" />
```

```
======ADDR 3C======= ======CHA/CHB TEST PATTERN(bit4 CHA, bit0 CHB)========
  <i2c_write addr="0x2D" count="1" radix="16">3C 00</i2c_write>
  <sleep ms="10" />
```

```
=======ADDR 0D======= ======PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured======
  <i2c_write addr="0x2D" count="1" radix="16">0D 01</i2c_write>
  <sleep ms="10" />
```

```
 =====SOFTRESET=======
  <i2c_write addr="0x2D" count="1" radix="16">09 00</i2c_write>
  <sleep ms="10" />
```

```
======write======
  <i2c_write addr="0x2D" count="196" radix="16">00</i2c_write>
  <sleep ms="10" />
```

```
======Read======
  <i2c_read addr="0x2D" count="256" radix="16">00</i2c_read>
  <sleep ms="10" />
```

```
</aardvark
```

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8.2.1.3 Application Curve

SN65DSI85: SINGLE Channel DSI to DUAL Channel LVDS, 1440 x 1200

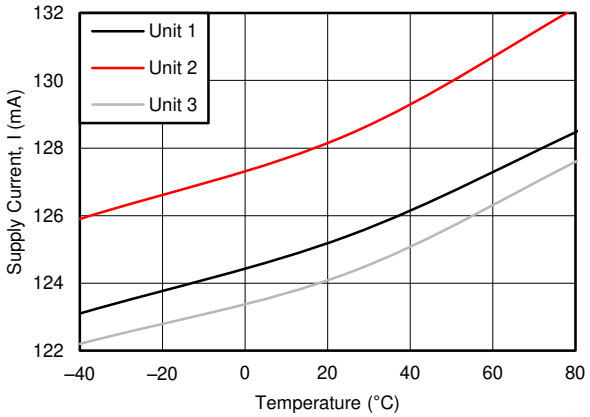

Figure 8-2. Supply Current vs Temperature

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8.2.2 Typical WQXGA 24-bpp Application

Figure 8-3 illustrates a typical application using the SN65DSI85 configured for a dual-channel DSI receiver to interface a dual-channel DSI application processor to an LVDS Dual-Link 24 bit-per-pixel panel supporting 2560x1600 WQXGA resolutions at 60 frames per second.

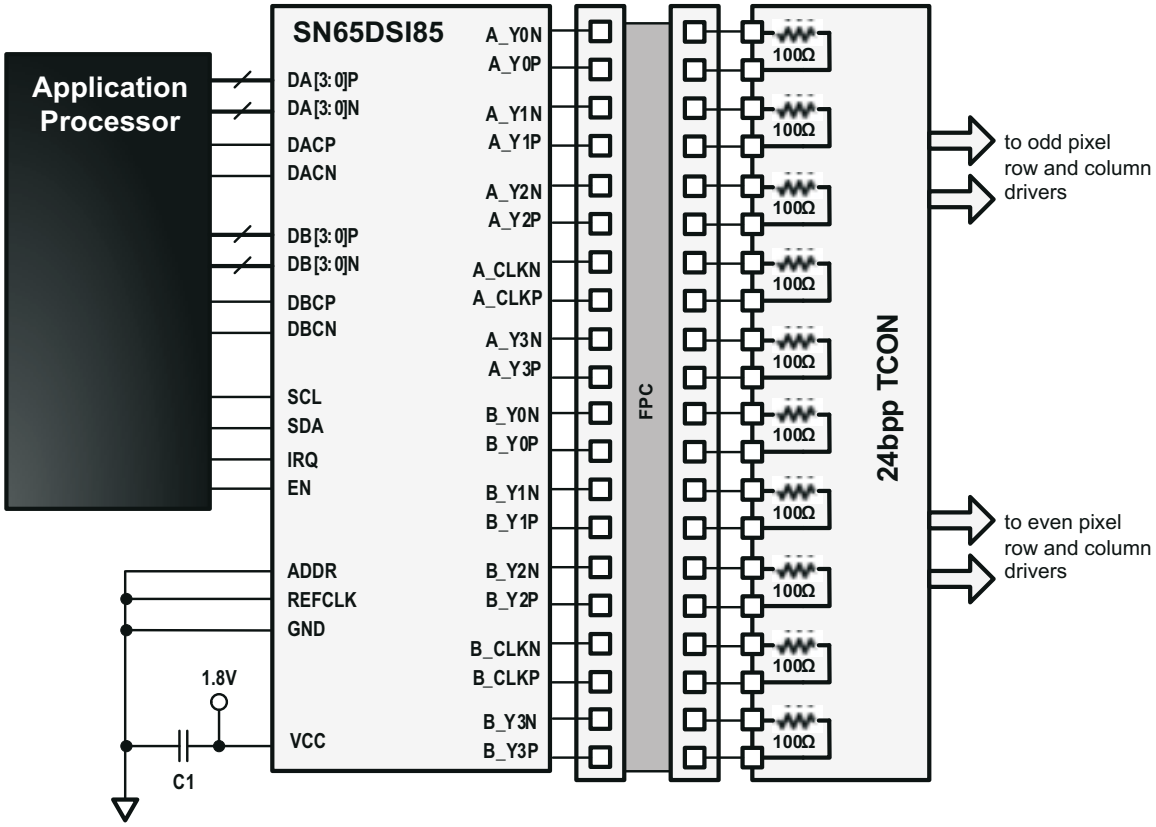

Figure 8-3. Typical WQXGA 24-bpp Panel Application

8.2.2.1 Design Requirements

Table 8-2 lists the design parameters for SN65DSI85.

Table 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC}	1.8 V (±5%)
PANEL INFORMATION	
LVDS Output Clock Frequency	154 MHz
Resolution	2560 x 1600
Color Bit Depth (6 bpc or 8 bpc)	8-bit
Number of LVDS Lanes	2 × [4 Data lanes + 1 Clock lane]
DSI INFORMATION	
Number of DSI Lanes	2 × [4 Data Lanes + 1 Clock Lane]
DSI Input Clock Frequency	500 MHz

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9 Power Supply Recommendations

9.1 V_{CC} Power Supply

Each VCC power supply pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI85 device. It is recommended to have one bulk capacitor (1 µF to 10 µF) on it. It is also recommended to have the pins connected to a solid power plane.

9.2 VCORE Power Supply

This pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI85 device. It is recommended to have one bulk capacitor (1 µF to 10 µF) on it. It is also recommended to have the pins connected to a solid power plane.

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10 Layout

10.1 Layout Guidelines

10.1.1 Package Specific

For the ZXH package, to minimize the power supply noise floor, provide good decoupling near the SN65DSI85 device power pins. The use of four ceramic capacitors (2 × 0.1 µF and 2 × 0.01 µF) provides good performance. At the least, TI recommends to install one 0.1-µF and one 0.01-µF capacitor near the SN65DSI85 device. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized. Placing the capacitor underneath the SN65DSI85 device on the bottom of the PCB is often a good choice.

10.1.2 Differential pairs

- Differential pairs must be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
- Keep away from other high speed signals.
- Keep lengths to within 5 mils of each other.
- Length matching must be near the location of mismatch.
- Each pair must be separated at least by 3 times the signal trace width.
- The use of bends in differential traces must be kept to a minimum. When bends are used, the number of left and right bends must be as equal as possible and the angle of the bend must be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of vias must be kept to a minimum. It is recommended to keep the via count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do NOT route differential pairs over any plane split.
- Adding Test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they must be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

10.1.3 Ground

TI recommends that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the SN65DSI85 must be connected to this plane with vias.

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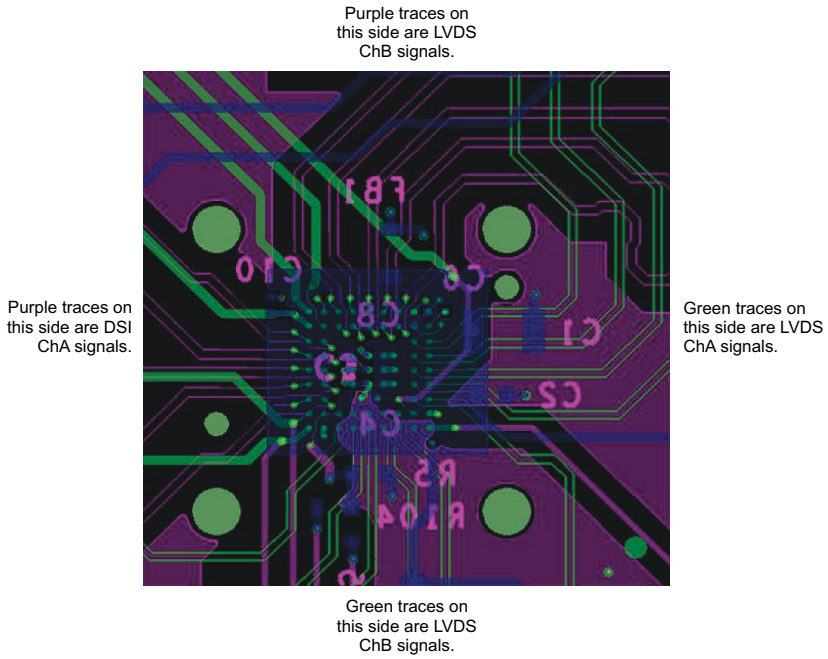
10.2 Layout Example



Green - Top Layer, Purple - Layer 3, Blue - Bottom Layer

Figure 10-1. SN65DSI85 Layout Example

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

11.3 Trademarks

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65DSI85ZXHR	Active	Production	NFBGA (ZXH) | 64	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DSI85
SN65DSI85ZXHR.A	Active	Production	NFBGA (ZXH) | 64	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DSI85

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65DSI85 :

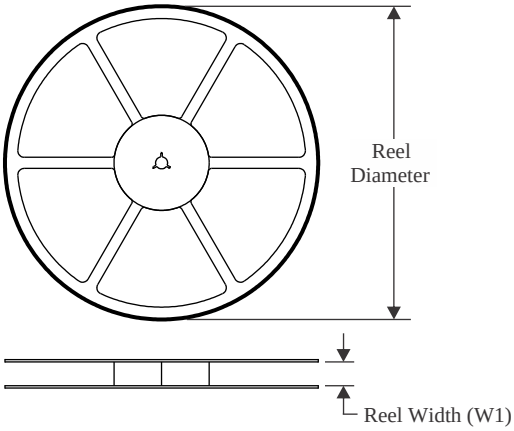
- Automotive : SN65DSI85-Q1

NOTE: Qualified Version Definitions:

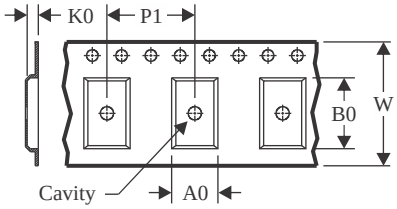
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

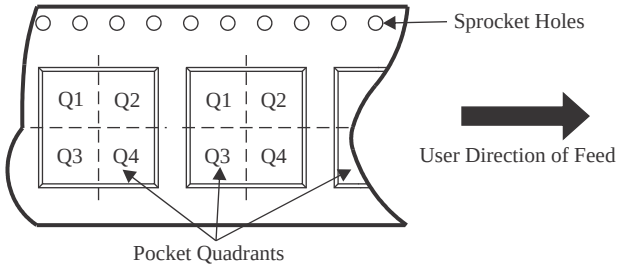


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

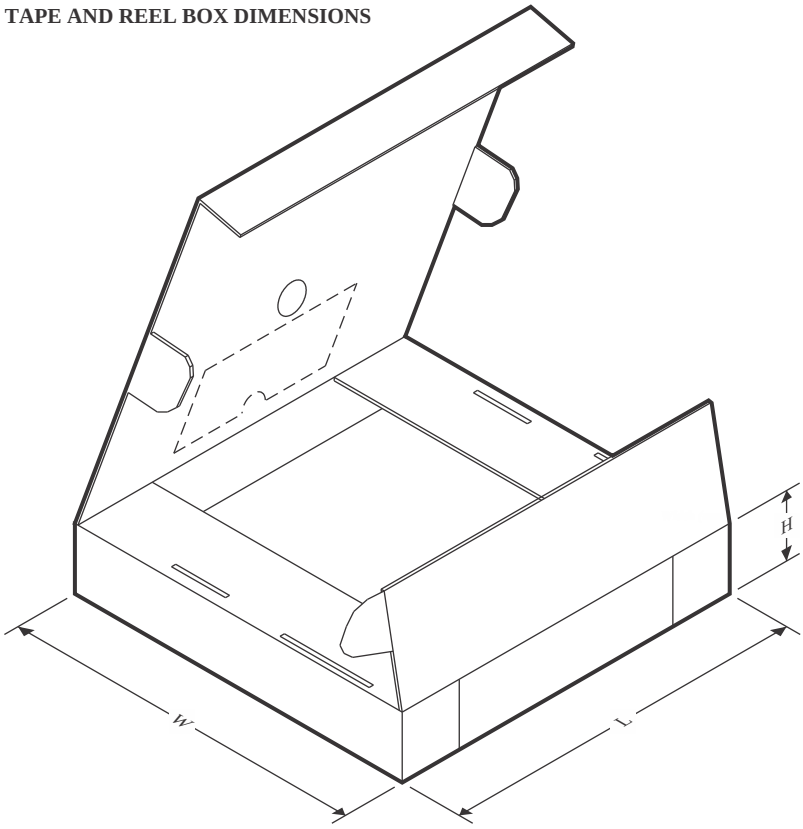
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65DSI85ZXHR	NFBGA	ZXH	64	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

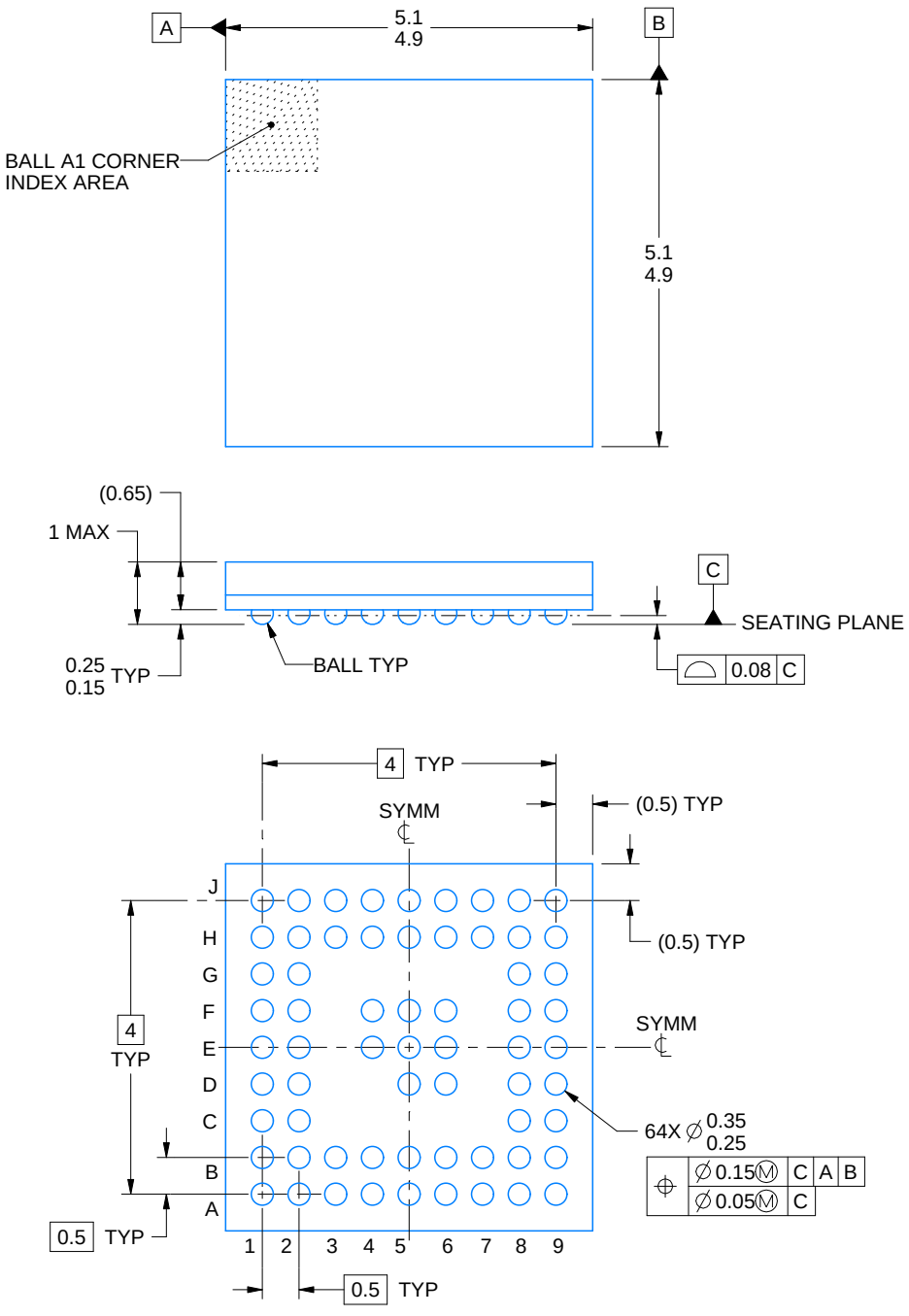
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65DSI85ZXHR	NFBGA	ZXH	64	2500	336.6	336.6	31.8

PACKAGE OUTLINE

ZXH0064A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



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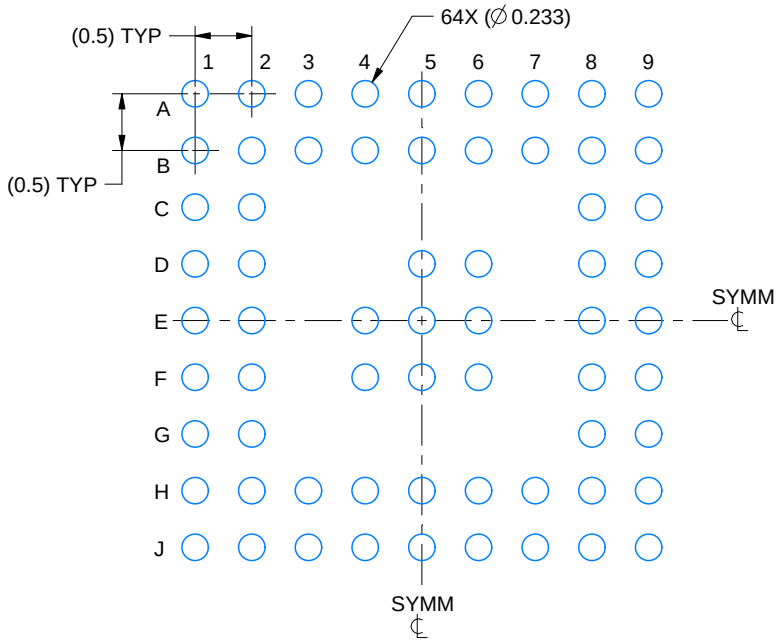
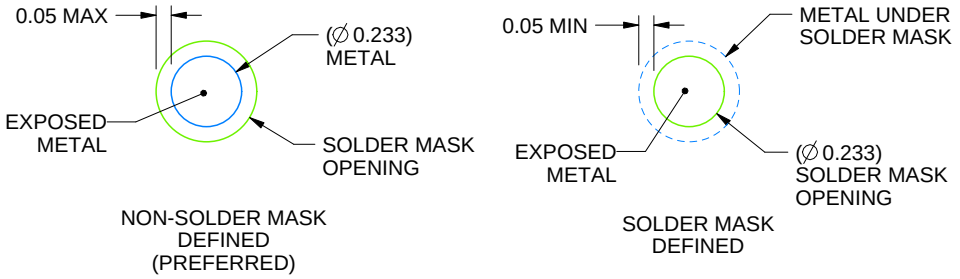
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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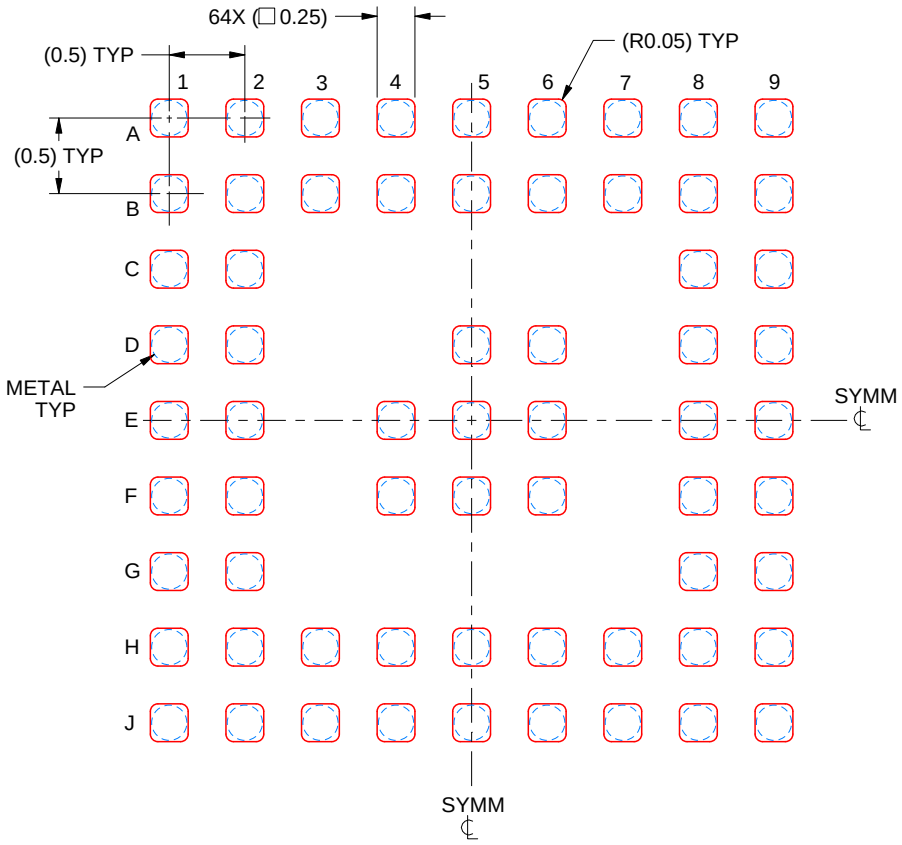
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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