LVDS Application and Data Handbook

High-Performance Linear Products Technical Staff

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Contents

List of Illustrations

List of Tables

INTRODUCTION

High-speed transmission of binary data has converged to a general class of low-voltage differential signaling (LVDS) that presents unique challenges to the designer. This handbook is a compilation of application notes for data transmission above 30 Mbps using an LVDS electrical layer.

What is LVDS? Where should it be used? What are its benefits? What are its limitations? Answers to these and other questions are the subject of this document. This guide examines the details of low-voltage differential signaling (LVDS) and provides applications information to help designers use these devices. This document looks at TI's broad selection of discrete LVDS devices ranging from single-channel drivers and receivers to serialization devices that significantly reduce the cabling, connector, and component costs required for today's interface solutions. However, before exploring the details of LVDS, step back first and look at data transmission in general, and see where LVDS fits in.

Transmitting data from one location to another, whether it takes place between integrated circuits on a printed-circuit board, or between networked computers located halfway around the world, has resulted in the development of numerous transmission technologies. These include electrical, optical, and wireless interfacing solutions. Over the past three decades, Texas Instruments has combined its expertise in high-speed digital and analog technologies to provide leading-edge solutions to meet the demands of today's data transmission needs. TI is constantly pushing the capabilities and extending the performance parameters of practically every electrical data-transmission standard.

Chapter 1 presents the basics of data transmission. Chapter 2 provides a mapping of system-level requirements to line-circuit features and characteristics; this becomes a basis for product selection in Chapter 4. To stimulate some design ideas, some application examples are provided in Chapter 3. Chapter 4 presents the product selection. Specifications are provided in Chapter 5 and Chapter 6 offer design guidelines and tools for obtaining optimum performance with the chosen line circuit. Finally, Chapter 7 presents common testing techniques used to verify or troubleshoot the design.

Chapter 1
Data Transmission Basics

Data transmission, as the name suggests, is a means of moving data from one location to another. Choosing the best transmission standard to accomplish this requires evaluation of many system parameters. The first two considerations encountered are *How fast?* and *How far? How fast?* refers to the signaling rate or number of bits transmitted per second. *How far?* is concerned with the physical distance between the transmitter and receiver of the data. Consideration of these two primary system parameters usually results in a significant narrowing of the possible solutions. Figure 1–1 shows the speed and distance coverage of some familiar data transmission choices.

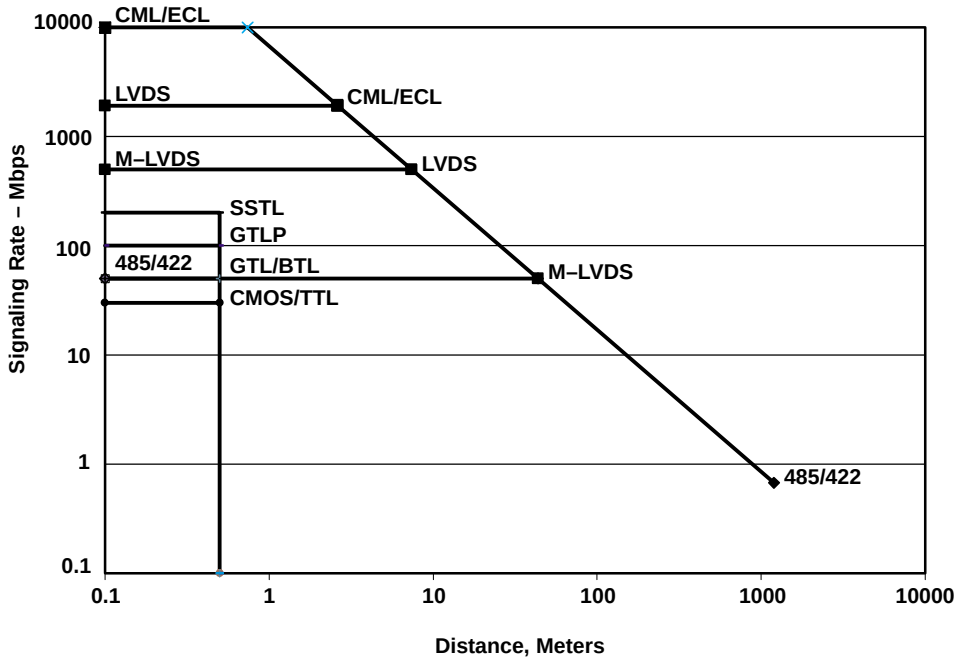


Figure 1–1. Approximate Signaling Rate vs Transmission Distance for Various Interfaces

As can be seen in Figure 1–1, signaling rate eventually decreases as transmission distance increases. While steady-state losses may become a factor at the longest transmission distances, the major factors limiting signaling rate, as the distance is increased, are time varying. Cable bandwidth limitations, which degrade the signal transition time and introduce intersymbol interference (ISI), are primary factors reducing the achievable signaling rate when transmission distance is increased.

Figure 1–1 also shows that general-purpose, single-ended logic, including backplane transceiver logic (BTL: IEEE 1194.1), gunning transceiver logic (GTL), and gunning transceiver logic plus (GTLP) provide satisfactory interface solutions when the transmission distance is short (< 0.5 m) and the signaling rate is moderate. When transmission distance is increased, standards with higher voltage swings or differential signaling often move the data.

If data transmission over about 30 m and less than 50 Mbps is required, differential signaling standards TIA/EIA-422 and TIA/EIA-485 should be considered. High differential outputs, sensitive receivers, and the capability to operate with up to 7 V of ground noise make these interfaces ideal for long direct connections between equipment. TIA/EIA-422 and TIA/EIA-485 use similar voltage levels but differ in the bus topologies they can support. TIA/EIA-422 is used for multidrop (one driver and many receivers) operation, while TIA/EIA-485 allows for multipoint signaling (many drivers and receivers).

For signaling greater than 50 Mbps or in low-power applications, low-voltage-differential signaling (LVDS) or multipoint-low-voltage-differential signaling (M-LVDS) provides an attractive solution. Introduced in 1996, LVDS, specified in TIA/EIA-644 offers high signaling rates and low power consumption for point-to-point or multidrop buses. M-LVDS, specified in TIA/EIA-899, was introduced in 2002 and offers similar benefits for the multipoint application. The benefits, features, and application of LVDS and M-LVDS are the subject of this handbook.

When the signaling rate requirements exceed the capabilities of LVDS, current-mode logic (CML) circuits are used, principally the emitter-coupled logic (ECL) and positive ECL (PECL) families. Signaling at 10 Gbps is possible with ECL/PECL devices. The high speeds are achieved at the cost of high power consumption.

Transmission Lines and Characteristics

An LVDS output voltage can switch from one logic state to the opposite in 260 ps and, in most applications, the interface must be modeled as a distributed-parameter circuit. This is not a model that most users relish analyzing. Fortunately, in most applications users can apply a transmission line model to the interconnect. Many others have solved transmission line characteristics and equations and only a summary is presented here.

Applying a transmission line model to the interconnection between LVDS circuits requires that two conditions be met.

1. The physical dimension of the interconnect circuit must be long compared to the shortest wavelength (highest frequency) of the signal. The highest frequency component of a binary signal is determined by the voltage (or current) transitions between logic states. This makes key parameters of the driver output voltage rise and fall times, since the fastest signal changes take place at this point in the circuit. If the delay time of the interconnect circuit is more than three times the 10%-to-90% transition time of the signal, the circuit is generally long enough to be modeled as a transmission line.
2. The dimensions of the conductors, the distance between the signal and return conductors, and the dielectric around them must be constant. The transmission line solution is based upon the model of each small segment along the transmission path being electrically the same and taking the segment length to zero. A discontinuity in the physical characteristics along the transmission path forces either a multiple transmission line model or a distributed parameter solution.

With the above conditions, the interconnect can be modeled as an ideal transmission line whose characteristics are determined by its distributed (per unit length) capacitance, C, and inductance, L. A good approximation results in the following characteristics:

- An ideal transmission line has a *characteristic impedance,* and both voltage and current at any point on the line are related by Z_0= v/i. The characteristic impedance is real (resistance) and $R_0 = \sqrt{L/C}\ \Omega$.
- The time delay per unit length of an ideal transmission line is a constant with a value of $\nu_0 = \sqrt{LC}\ \Omega$ seconds/length.
- The ideal transmission line is lossless, and there is no attenuation of the input signal along the transmission path.

When a line driver changes output states, an initial voltage wave is launched into the transmission line. The driver output characteristics and the characteristic impedance of the transmission line determine the voltage and current of the wave (see Figure 1–2).

See reference 4 for one solution.

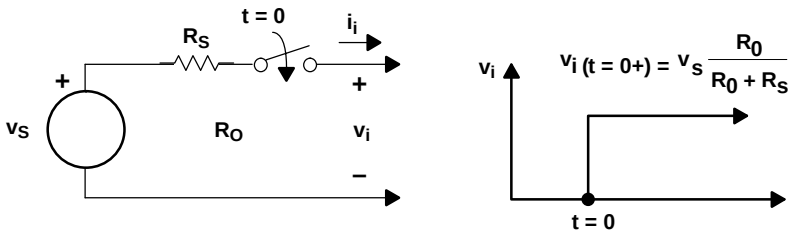


Figure 1–2. Initial-Wave Circuit Model

In the ideal transmission line model, the initial wave would continue to propagate to infinity. Since real circuits have an end to them, the wave encounters a load resistance, R_L (see Figure 1–3). At that point, the total signal power available is what was input some time ago as $P_i = v_i^2/R_O$. Since the power in the load is $P_L = v_L^2/R_O$ and energy must be conserved, one might suppose that $v_i^2/R_O = v_i^2/R_L$. However, if R_O were greater than R_L and the incoming voltage and the voltage across the load were the same, there would be more power on the load than was input to the line. From the conservation of energy principal, this cannot be and means there is a missing term from the power equality and $v_i^2/R_O = v_L^2/R_L + v_r^2/R_O$ where the term v_r^2/R_O is the power not absorbed by the load and reflected back into the transmission line.

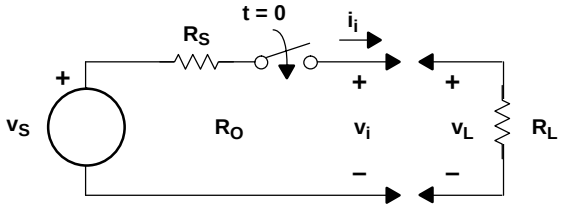


Figure 1–3. The Line-Load Boundary

A bit of algebraic manipulation shows that the ratio of v_r to v_i needed to maintain energy equilibrium is $\frac{v_r}{v_i} = \frac{R_L - R_O}{R_L + R_O}$. This is defined as the voltage reflection coefficient of the load and is often designated as ρ_{vL}.

Example: Figure 1–4 gives an example of a 2-V source with a 100-Ω source resistance driving one meter of cable terminated with 150 Ω. At t = 0, an initial voltage wave of 1 V is generated at the source and is determined by division of 2 V by the 100-Ω source and characteristic impedance of the transmission line. The wave propagates down the cable at 5 ns/m where it reaches the 150-Ω load resistor. At that instant, a reflection is generated of $v_r = v_i \times \rho_{vL} = 0.2$ V. The reflected voltage adds to v_i and the voltage across R_L goes to $v_i + v_r = v_i (1+\rho_{vL}) = 1.2$ V. The reflected wave travels back towards the source where the 100-Ω source resistance absorbs all of the signal power as indicated by the reflection coefficient of zero at the source.

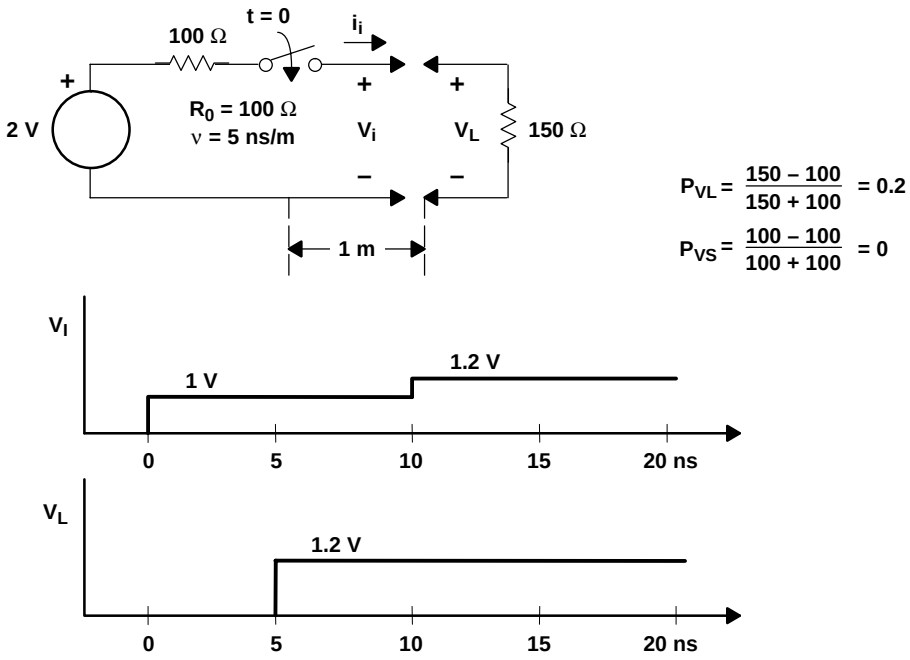


Figure 1–4. Reflected-Wave Example

If transmission lines were ideal and lossless, there would be no limit on how long a cable could be and still be able to recover the input signal. As seen in Figure 1–1, the maximum signaling rate decreases as the cable length increases. This is due to the second-order effects not included in the ideal transmission line model. Skin, proximity, dielectric loss, and radiation loss effects all act to influence the primary line parameters and degrade the signal. Estimation of these effects is best made empirically and the application chapters of this document offer guidelines.

Single-Ended vs Differential

We referred earlier to single-ended data transmission (as employed in BTL, GTL, GTLP, TIA/EIA–232, etc.) and differential transmission (as used with TIA/EIA-422, TIA/EIA-485, TIA/EIA–644 (LVDS), etc.). Each method of transmission has benefits and disadvantages.

Single-Ended Transmission

Single-ended transmission is performed by using one signal line for each information channel and a common ground return path shared among numerous information channels. Figure 1–5 shows the electrical schematic diagram of a single-ended transmission system. Single-ended receivers interpret the logical state at their inputs based upon the voltage at the single input line with respect to ground.

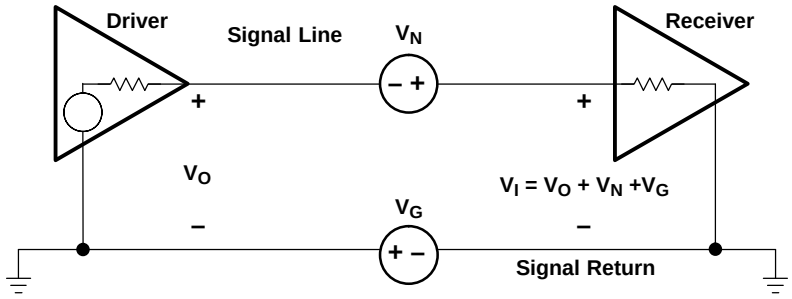


Figure 1–5. Single-Ending Interface Circuit Schematic Diagram

The advantages of single-ended transmission are simplicity and low cost of implementation. A single-ended system requires only one line per signal. It is therefore ideal when cabling and connector costs are more important than the signaling rate or transmission distance. You will find this tradeoff in low-speed PC applications such as a parallel printer port or serial communication with many handshaking lines.

The main disadvantage of the single-ended solution is its relatively poor noise performance at high signaling rates or long distances. Because the noise coupled to the circuit adds to the signal voltage, it is susceptible to data errors. The signal line of a single-ended circuit acts as an antenna to radiate and receive electric fields while the area formed around the circuit path is an antenna for magnetic fields. The voltage source V_N, as shown in Figure 1–5, represents this high-frequency electromagnetic coupling. Since single-ended interface circuits generally share the return path with other circuits, there is also a component of conducted susceptibility as changes in the ground current create the ground noise voltage represented by V_G. This noise is generally low in frequency (i.e., 60 Hz from main power).

Differential Transmission

Differential transmission addresses many of the shortcomings of single-ended solutions by using a pair of signal lines for each information channel. Figure 1–6 shows an electrical schematic diagram of a differential transmission system. The differential driver uses a pair of complementary outputs to indicate the state transmitted. The differential receiver detects the voltage difference between the signal pair, rather than relative to ground, to determine its output state.

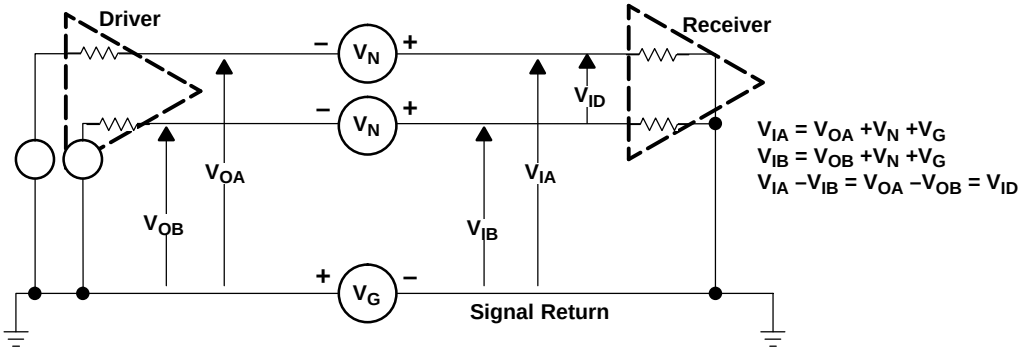


Figure 1–6. Differential Interface Circuit Schematic Diagram

This mode of transmission has several important advantages over single ended. You can see the fundamental advantage in the derivation of the differential input voltage, V_{ID}, in Figure 1–6. The noise sources V_N and V_G add to the input signals V_{IA} and V_{IB}, just as with the single-ended circuit, but by taking the difference between the two input voltages, the common noise terms are cancelled from the desired signal. The differential receiver accomplishes this and, with small differential input voltage thresholds, maintains high signal-to-noise ratios.

There is a presumption that the V_N coupled to each signal line are equal or nearly so. Differential signal pairs that are close together are generally exposed to the same noise sources. Twisting the signal wires together adds to this advantage. This ensures similar exposure to electric fields and cancels differential emf from magnetic field coupling by reversing the polarity in adjacent loops created by the twist.

In addition to noise immunity, differential circuits radiate substantially less noise to the environment than single-ended circuits. This is primarily due to the complementary current in each line of the signal pair canceling each other's generated fields. Conducted noise is also lower because there is little common-mode current to circulate through the signal return path.

Differential signaling adds cost and complexity in silicon and interconnecting hardware where it is roughly double that for a single-ended interface. As signaling rate or the number of circuits increase, this becomes less of a disadvantage as you add ground wires to make the single-ended signaling work. Indeed, you can find few data interfaces above 10 Mbps or longer than a half meter or so that are not differential.

Point-to-Point, Multidrop, and Multipoint Buses

Each electrical interface design is different, but interface problems can be categorized into certain common topologies or architectures. The number of drivers and receivers physically interconnected via a common media determines the architecture, limits the possible interface solutions, and drives the requirements on line circuits.

Point-to-Point

A point-to-point interface consists of only two connections to the transmission media. This can be a single driver and a single receiver in a simplex connection (unidirectional transmission) or a transceiver at each end operating in half duplex (bidirectional transmission). The point-to-point connection provides the optimum configuration from a performance viewpoint. A point-to-point connection avoids mainline stubs and other discontinuities, and provides the highest possible signaling rate. Figure 1–7 shows a differential point-to-point simplex and half-duplex connection.

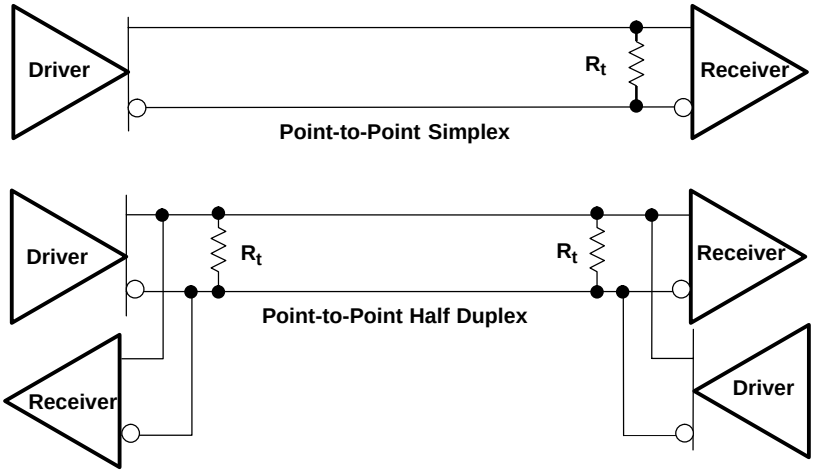


Figure 1–7. A Point-to-Point Data Interchange Circuit

Multidrop

A multidrop or distributed simplex distribution bus is the second common interconnection approach. A multidrop bus consists of a single driver with multiple receivers connected to the main transmission line. The line termination is most often located at the far end of the line. Like point-to-point, a multidrop connection provides unidirectional transmission. Multidrop communication is common when a single master needs to broadcast the same information to multiple slaves. Figure 1–8 shows a differential multidrop interconnection.

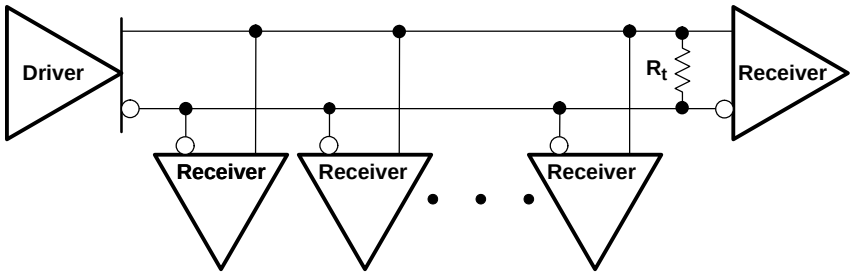


Figure 1–8. A Multidrop Data Interchange Circuit

Multipoint

The final architecture is multipoint, also called multiplex, communication. A multipoint bus is three or more stations or nodes connected to a common transmission line where any two nodes can establish communication. Electrical requirements for the line circuits are the same as for the point-to-point half-duplex connection but are flexible in the number of listen-only, talk-only, or talk-and-listen stations. Figure 1–9 shows a multipoint interconnection.

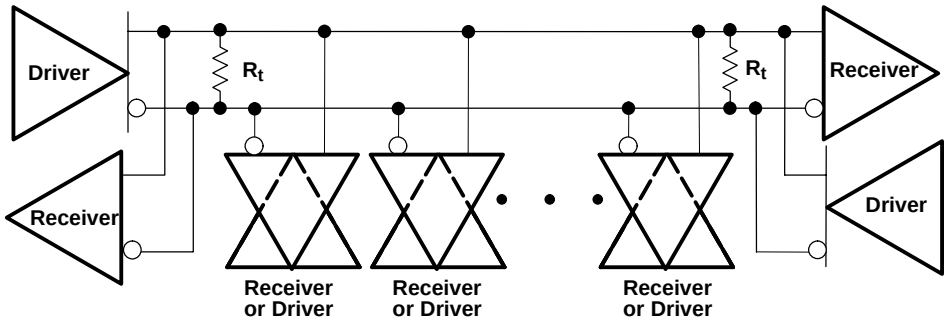


Figure 1–9. A Multipoint Data Interchange Circuit

Physical location of stations may require other system topologies. However, once you adopt the transmission-line model, it must be constructed using these basic interconnections and linked through repeaters or concentrators to maintain a clean electrical path between stations connected to a single transmission-line segment. Data-flow management of these hybrid configurations is complex and beyond the scope of this handbook.

Benefits of Standardization

Data transmission, as the name suggests, is a means of moving data from one location to another. To accomplish this, the sender and receiver must have agreed upon the nominal rate of transmission, the information-to-bit mapping pattern, the communication protocol, and the electrical states and pulse codes used to represent logical states on the bus. These (and other) agreements are often made in either formal or informal interface standards and can specify the requirements to varying depths or layers. This handbook addresses only the lowest (electrical) layer of the interface.

Standardization allows for interoperability of equipment or parts from different suppliers, and independence from sole-source suppliers. It also encourages competition between multiple producers. When multiple vendors compete for the same standardized business, design innovations and production efficiency become key competitive factors. The benefits are higher quality and more readily available mass-produced goods at lower prices.

Without standards, common items such as screws and nuts, light bulbs, tires, and computer parts would be significantly more expensive, and it would be much harder to find replacements for them. A simple example of how a lack of standardization raises costs and makes replacements harder to find is valve stems for faucets. The local building centers or plumbing-supply houses have a variety of choices; getting exactly the right one is costly and quite often a gamble.

More to the point of this document is the world of electrical interfaces, where standardization permits interoperation of systems produced by different vendors. The worlds of computers and telecommunications are based on standards. You can trace the explosive growth of the IBM-compatible personal computers in the consumer market directly to the availability of a large number of publicly available electrical and mechanical interface standards. Numerous other personal-sized computer systems have failed commercially because either their makers kept the interfaces secret, or they were incompatible with already established and popular standards.

644 vs 644a vs LVDM vs M-LVDS

Standardization bodies conceived LVDS (as specified in TIA/EIA-644) to provide a general-purpose electrical-layer specification for drivers and receivers connected in a point-to-point simplex interface. The standard requires receivers to have input leakage currents below 20 μA, which drive the receiver input impedance requirements. Figure 1–10 shows the driver test circuit.

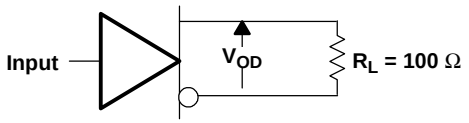


Figure 1–10. TIA/EIA-644 Driver Output Test Circuit

Although 644 compliant devices have seen rapid and broad acceptance in point-to-point communications, the 644 standard does not quantify the driver characteristics required for multidrop operation. (As discussed previously, a multidrop application has one driver communicating with multiple receivers.) The 644 receiver leakage requirement of 20 μA has a small effect on the driver output voltage when only one receiver is connected, but this effect becomes more pronounced as the driver is loaded with additional receivers. An update to LVDS, designated TIA/EIA–644–A, standardizes the driver requirements for LVDS devices being used in a multidrop configuration. The full-load test required for the driver output identifies 644-A compliant devices. Figure 1–11 shows the 644-A test circuit, which ensures connection of 32 receivers in a multidrop configuration.

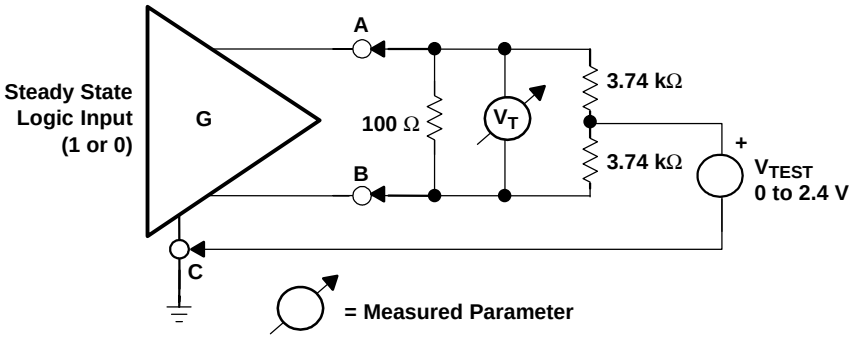


Figure 1–11. TIA/EIA-644-A Driver Output Test Circuit

A distinct difference for the driver in a half-duplex point-to-point or multipoint bus versus a point-to-point simplex or multidrop bus is the load presented to the driver as the output switches. When transmitting from the end of the line, the driver load is a transmission line with characteristic impedance of R_0 in parallel with the termination resistor used to prevent reflections from other driver(s). If properly terminated, the termination value is R_0 and the equivalent load becomes $R_0/2$. The load presented to a driver located midbus is two transmission lines in parallel and presents a time-varying load to the driver of $R_0/2$. Since reflection prevention requires termination resistors equal to R_0 at both ends of the line, the steady-state load is also $R_0/2$.

The need for multipoint LVDS-like drivers quickly emerged and TI and National Semiconductor offered proprietary solutions. TI offers an LVDM family of drivers, which are compliant with the 644 LVDS standard, with the exception of a doubling of the output current. These LVDM drivers are also useful for additional noise margin in a multidrop or a point-to-point connection.

The proprietary solutions were not necessarily interchangeable or did not address all of the requirements for a robust multipoint interface circuit. In response, the technical committees of TIA developed TIA/EIA-899 to standardize and provide the benefits of LVDS in a multipoint environment. Familiarly known as multipoint-LVDS or M-LVDS, TIA/EIA ratified and published this standard in early 2002. TI participated in the development of this standard, and has developed components that are in full compliance.

TIA/EIA-644-A LVDS and TIA/EIA-899 are both ANSI-accredited international standards and higher-level standards reference them for the electrical layer of data interfaces. Higher-level standards address mechanical and protocol requirements.

LVDS/M-LVDS Summary

The most attractive features of LVDS include its high signaling rate, low power consumption, and electromagnetic compatibility. The following sections summarize each of these benefits and Chapter 2, *LVDS and M-LVDS Line Circuit Characteristics and Features*, offers a more detailed explanation.

Signaling Rate

We define the number of state changes per unit time as the signaling rate for the interface. Knowing the unit interval time, t_{UI}, between state changes, you can derive the signaling rate as the inverse of the unit interval.

TIA/EIA-644-A and TIA/EIA-899 require that driver output transition times be less than 30% of the unit interval, with a lower limit of 260 ps and 1 ns, respectively. The standards also recommend that the transition time at the receiver input be less than 50% of the unit interval. The difference between driver output rise time and receiver input rise time allows for signal degradation through the interconnect media.

Combining the driver transition times required by the standard, and receiver input rise time recommendations, LVDS supports a theoretical maximum signaling rate of 1.923 Gbps and M-LVDS 500 Mbps. Longer transition times, leading to lower signaling rates, are also allowed by the standards. You should note that the standards define the characteristics at the interface to the bus and not the line circuit. Line circuits may support signal transitions faster than 260 ps and even higher signaling rates if standard compliance is not required.

When estimating the minimum signaling rate for a particular line circuit, designers should use the maximum output transition time. For example, in the SN65LVDS31, the maximum specified 20%-to-80% differential output transition time is 600 ps. Using the 30% relationship between rise time and unit interval, we see that this driver can support standard unit interval of 600 ps/0.3 = 2000 ps or a signaling rate of 500 Mbps. The 30% rule is conservative and users can obtain higher signaling rates with appropriate timing budgets.

Power

As the name implies, LVDS is a low-voltage signaling standard. An LVDS output driver provides 350 mV, nominal, into a 100-Ω load. This results in ≈1.2 mW of power delivered to the load. Figure 1–12 compares the load power of LVDS and other differential signaling techniques and shows LVDS to be 1.5% to 50% of the presented signaling approaches. In general, a lower load power correlates closely with lower overall power for the interface.

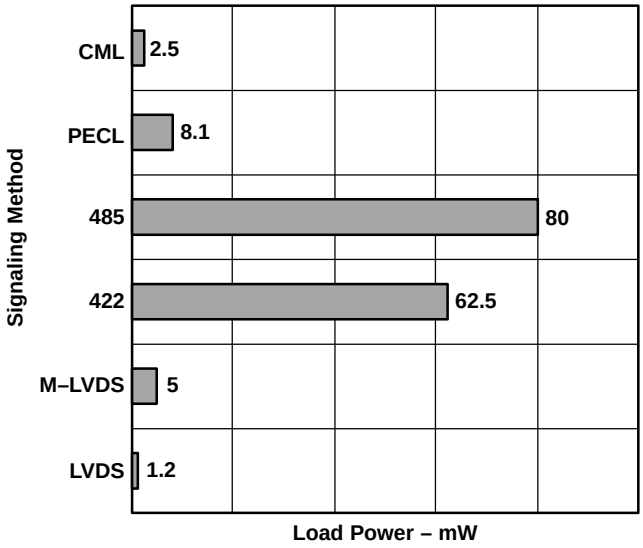


Figure 1–12. Load Power Comparison of Differential Signals

Electromagnetic Compatibility

Differential signaling allows LVDS to operate in the presence of electromagnetic noise, while at the same time minimizes its own radiated emissions. Differential signaling also rejects externally coupled noise common-mode when within the input range of the differential receiver. Figure 1–13 shows the voltage range for different TIA/EIA standardized interfaces. It is interesting to note that an attempt to include ECL, CML, or other informal standards is difficult or impossible due to the lack of a single specification but rather a family of similar device data sheets.

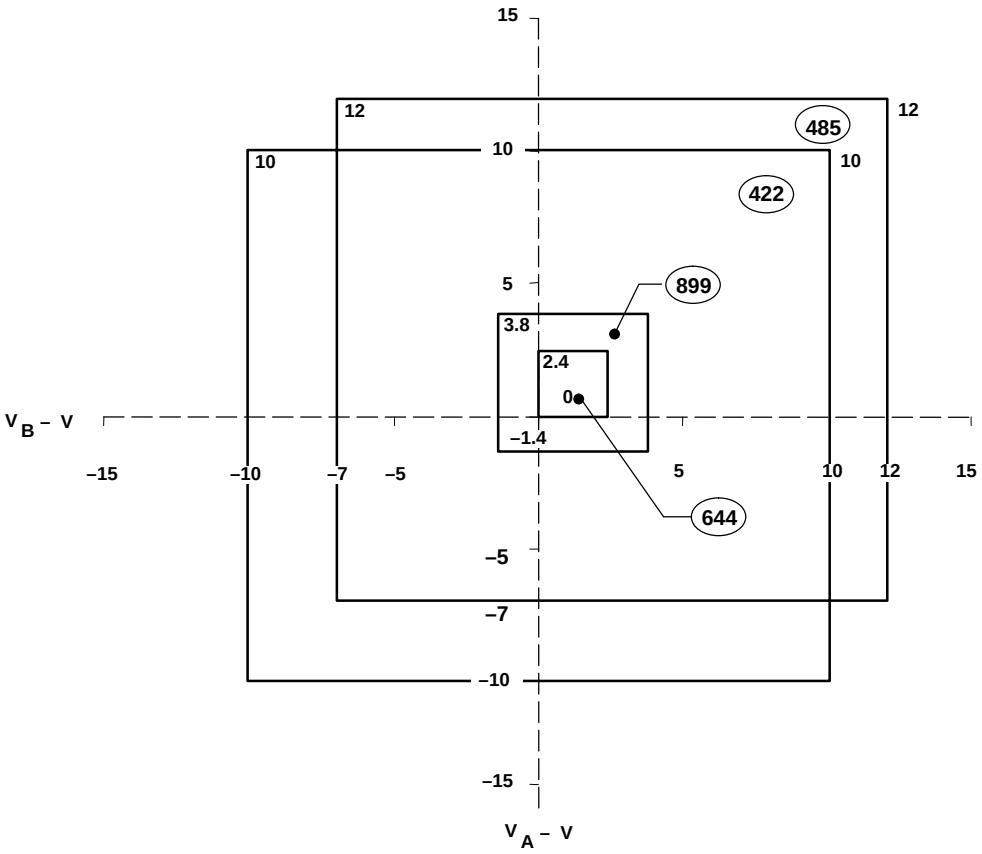


Figure 1–13. TIA/EIA Standard Voltage Ranges

References

1. TIA/EIA-644: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits in 1996
2. TIA/EIA-899: Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M-LVDS)
3. Hayt, William H., *Engineering Electromagnetics*, McGraw Hill, Inc., 1974: 407–424

Chapter 2
LVDS And M-LVDS Line Circuit Characteristics and Features

This chapter builds on the introductory material presented in Chapter 1 by attempting to provide the reader with some insight into the line circuit features and their impact on system performance. The chapter presents specific requirements of the TIA-644-A and -899 standards along with nonstandard characteristics that affect overall performance.

Driver Output Voltage

The driver's primary function is to launch an electromagnetic wave into one or two transmission lines. As explained earlier, this is equivalent to generating a voltage across a resistor, albeit a low-valued resistor. Most device specifications designate the differential output voltage as V_{OD} and referenced to the inverting output. Both the minimum and maximum output voltages are significant parameters, as the minimum sets the minimum noise margin for the interface and the maximum establishes the input voltage range of circuits connected to the bus.

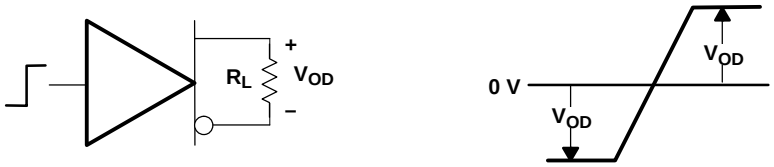


Figure 2–1. V_{OD} Definition

TIA/EIA-644-A drivers must generate a V_{OD} of 247 mV to 454 mV across 100 Ω, while 899 drivers require more voltage, 480 mV to 650 mV, across the smaller load of 50 Ω. The reasons for the difference fall back to the extra noise contributors in the multipoint environment versus point-to-point discussed earlier.

Beyond the basic function, the symmetry of the complementary outputs becomes an important characteristic for noise emissions from the line. Ideally the current in each conductor of the signal pair is equal and opposite; as usual, the ideal is too expensive to achieve. This means that there is always some inequality in the two currents called imbalance. Imbalance can result from differences in the electrical characteristics of the complementary driver output circuitry or the loads, or from time delay between switching outputs. This is particularly critical, as the common-mode components created during switching imbalance are high in frequency and radiate readily.

The differential driver parameter of significance in this regard is the common-mode output voltage, V_{OC} (sometimes designated a V_{OS}), and is the arithmetic mean of the two complementary output voltages. You measure this driver characteristic directly by monitoring the output voltage at the node between two identical resistors connected across the line as shown in Figure 2–2. The common-mode output can be broken down to the steady-state and peak-to-peak parameters $V_{OC(SS)}$ and $V_{OC(PP)}$ with emitted noise frequency fundamentals of $0.5/t_{UI}$ Hz with $V_{OC(SS)}$ and out to $3/t_{UI}$ Hz and beyond with $V_{OC(PP)}$.

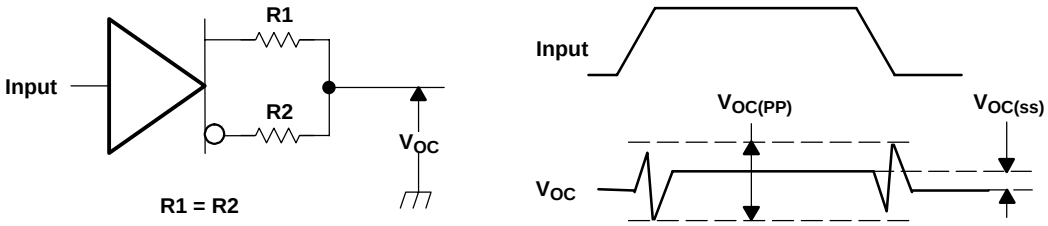


Figure 2–2. Circuit Used to Measure the Driver Common-Mode Output Voltage

The smaller the $V_{OC(PP)}$ parameters are, the better the noise emission performance of the interface. Both TIA/EIA-644 and -899 require their drivers to create no more than 150 mV of $V_{OC(PP)}$. When comparing the radiation potential of a data line, $V_{OC(PP)}$ is directly comparable to the voltage swing of a single-ended signal, and the advantage of differential over single-ended signaling in this regard becomes obvious.

Differential Input Voltage Threshold

The input signal to the transmission line is the driver output voltage; the differential receiver must detect what comes out. The first parameter to consider for a receiver is the differential input voltage threshold, V_{IT}, as it defines the voltage needed to change the receiver output state. The specified maximum and minimum V_{IT} establish the limits for V_{IT}, and difference voltages above or below them assure that the receiver indicates a valid logic state at its output.

The EIA/TIA-644-A standard specifies a maximum V_{IT} of 100 mV and a minimum of –100 mV under all operating conditions and over the input common-mode voltage range. With a minimum driver differential output voltage of 247 mV, this provides a worst-case differential noise margin of 147 mV. Although this may seem like a small value, interference in a well-balanced differential transmission system introduces virtually no differential noise.

In addition to a higher minimum output voltage for TIA/EIA-899 drivers, compliant receivers must exhibit a maximum V_{IT} of 50 mV and a minimum of –50 mV for Type-1 receivers, for a minimum 400 mV differential noise margin. TIA/EIA-899 also specifies Type-2 receivers with a maximum V_{IT} of 150 mV and a minimum of 50 mV. The offset V_{IT} of a Type-2 receiver allows a 0-V difference to be a valid bus state and is useful for wired-logic signaling or failsafe provisions. Figure 2–3 shows a graphical summary of the input voltage thresholds.

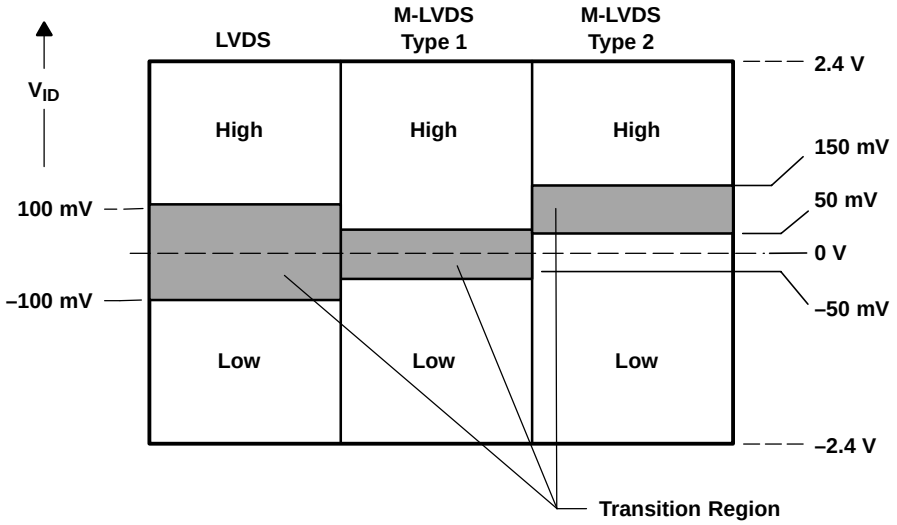


Figure 2–3. LVDS and M-LVDS Differential Input Voltage Thresholds

A differential input voltage between the maximum and minimum thresholds lies in the transition region and results in an indeterminate output state. The output may be high, low, or on its way between states. The time-varying behavior of the output during transition depends upon the bandwidth of the receiver and the time variation of the input voltage.

Consider an LVDS line receiver as a differential amplifier with a gain of about 100,000. V_{IT} is the input voltage where the output would be one-half of the way between high and low and, with no feedback for hysteresis, it takes only a few 10s of microvolts above or below the threshold for the output to switch to a high or low state. The system is likely to have this much differential noise and, if near the threshold, could cause oscillation of the output[2].

[2]See *Fault Tolerance and Failsafe Receivers section* later in this chapter for handling this condition.

Fortunately, the gain at high frequencies goes down to a point where the circuit does not respond to noise riding on the input signal. A rule of thumb is to transverse the input transition region ($V_{IT(MAX)} - V_{IT(MIN)}$) in less than 10 x t_T, where t_T is the 20%-to-80% output transition time of the receiver. For example, for a receiver with an output transition time of 1 ns, you would want the input signal to go through the transition region in under 10 ns. If the design cannot assure the input transition times, we recommend a receiver with some internal feedback to provide input voltage hysteresis. TI has LVDS and M-LVDS receivers that provide 25 mV of hysteresis.

Common-Mode Voltage Range

Referring back to Figure 1–6 in Chapter 1 and related discussion, differential signaling works well because noise is common to both signal lines and is rejected. As with all circuits, there is a limit to the noise voltage magnitude and frequency that a differential receiver can reject. This leads to the need to specify a receiver's input common-mode voltage range, commonly designated as V_{ICR}. The common-mode voltage range required for an interface circuit represents a compromise that takes into account numerous factors including the available semiconductor technologies, signaling rates, cable impedances, distance goals, and other relevant environmental factors.

The impact of EMI on a perfectly balanced differential transmission line is to induce a purely common-mode voltage which is identical on each of the two conductors. The magnitude of the induced common-mode voltage is a function of several factors: The strength, orientation, and proximity of the disturbing source; the effects of any shielding that may be present; and the common-mode impedance characteristics of the transmission system. Predicting the exact nature of EMI-induced common-mode voltage is difficult at best, but the reader should assume there is always some amount present.

Ground potential differences are another major source of common-mode noise voltage[3]. They may be induced by EMI, by the power distribution system, or by ground-return currents in the local power supplies. Predicting the magnitude of ground shift induced common-mode voltage is also very difficult, and designers need to examine each installation and use good design and layout techniques to reduce or eliminate these problems.

Common-mode rejection is an inherent feature of true differential receivers, just as it is with other differential-input circuits such as operational amplifiers. The degree to which a differential amplifier or receiver can reject common-mode voltages is a function of several factors. Careful electrical and mechanical design of the receiver components and interconnections is required to ensure that the matching is as close to ideal as possible. Designers can use an input attenuator to reduce the common-mode voltage seen by the circuit, typically with a proportional loss in the differential signal. The attenuator can employ active feedback circuits to sense and partially compensate for the received common-mode voltage such that they attenuate more of the common-mode than the differential signal. They have finite response times and so are of decreasing value as the frequencies increase.

Passive filtering termination circuits can also attenuate the common-mode noise seen at the receiver terminals more than the differential signals. Common-mode chokes, or baluns, along with split termination resistors with capacitors to ground from the center point, are frequently used filter implementations.

The receiver common-mode input voltage is the mean value of the voltages at the inputs, V_{IA} and V_{IB}. Summing the defining equation for these two voltages from Figure 1–6 in Chapter 1 and dividing by two gives the expression for the common-mode voltage below.

$$V_{IC} = \frac{V_{IA} + V_{IB}}{2} = \frac{V_{OA} + V_N + V_{OB} + V_N + V_G}{2}$$

[3]Some additional information related to common-mode noise and LVDS is available in several TI application reports. *A Statistical Survey of Common-Mode Noise* (SLLA057); *LVDS in Harsh Environments with the Next Generation Receivers* (SLLA061), and *Solving Noise Problems with LVDS* (SLLA073).

Combining and rearranging the terms gives, $V_{IC} = \frac{V_{OA} + V_{OB}}{2} + V_N + V_G$, and recognizing that $\frac{V_{OA} + V_{OB}}{2} = V_{OC}$ gives $V_{IC} = V_{OC} + V_N + V_G$. This means that the receiver input common-mode voltage range includes the driver V_{OC} as well as the noise terms and must accommodate both. It is also important to recognize that V_{IC} contains steady-state as well as time-varying components.

TI measures common-mode rejection versus frequency for a differential line receiver as a go/no-go test since it has only two output states. Parameters such as common-mode rejection ratio (CMRR) applied to differential amplifiers have meaning only at nodes internal to the differential line receiver circuit. Instead, we evaluate the common-mode rejection of a differential line receiver by applying a steady-state maximum and minimum V_{IT} (100 mV and –100 mV in the case of LVDS) and a common-mode test pulse to the inputs as shown in Figure 2–4. The common-mode pulse transverses the V_{ICR} and we verify that the receiver's output does not change state. This test determines the common-mode frequency response by the high-order harmonics generated in the edges of the pulse and usually specifies a transition time of less than 20% of the intended minimum unit interval for the circuit. For example, a 500-ps transition time applies high-frequency harmonics out to the gigahertz range.

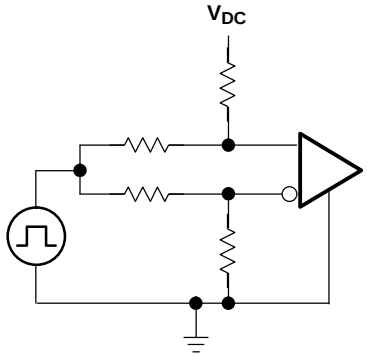


Figure 2–4. Common-Mode Rejection Test of a Differential Line Receiver

Table 2–1 shows the tolerance of the various differential signaling standards to common-mode noise voltage and introduces the SN65LVDS33 LVDS receiver with extended V_{ICR}. Texas Instruments' family of LVDS products includes several receivers with common-mode ranges that extend beyond the minimum specified in TIA/EIA-644-A. Wider V_{ICR} allows LVDS signaling in environments that would otherwise be too hostile for standard LVDS. Many of these devices are pin-compatible replacements for other popular receivers.

Table 2–1. Noise Voltage Tolerance of Differential Signaling Standards

STANDARD	MAXIMUM RECEIVER INPUT VOLTAGE	MINIMUM RECEIVER INPUT VOLTAGE	RECEIVER COMMON-MODE INPUT VOLTAGE RANGE	MAXIMUM DRIVER COMMON-MODE OUTPUT VOLTAGE	MINIMUM DRIVER COMMON-MODE OUTPUT VOLTAGE	MAXIMUM COMMON-MODE NOISE VOLTAGE
Generic	$V_{I(MAX)}$	$V_{I(MIN)}$	V_{ICR}= $V_{I(MAX)}$–$V_{I(MIN)}$	$V_{OC(MAX)}$	$V_{OC(MIN)}$	$V_N + V_G$= MIN($V_{I(MAX)} - V_{OC(MAX)}$, $V_{OC(MIN)} - V_{I(MIN)}$)
ECL[4]	–0.88	–1.81	0.93	–1.25	–1.417	0.37
PECL	4.12	3.19	0.93	3.75	3.583	0.37
LVPECL[5]	2.42	1.355	1.065	2.005	1.73	0.375
TIA/EIA-644-A	2.4	0	2.4	1.375	1.125	1.025
TIA/EIA-899	3.8	–1.4	5.2	2.1	0.3	1.7
SN65LVDS33 with M-LVDS Driver	5	–4	9	2.1	0.3	2.9
SN65LVDS33 with LVDS Driver	5	–4	9	1.375	1.125	3.625
TIA/EIA-485-A	12	–7	19	3	–1	6
TIA/EIA-422-B	10	–10	20	3	–3	7

Signaling Rate

The basic function of a line driver or receiver is the recreation of a logic state change over a distance. The signaling rate or data signaling rate is simply the number of state changes made per unit of time. It does not distinguish between data, clock, or handshaking signals, nor depends upon the bus architecture or protocol. It simply describes the transmission or reception rate of a single bit. Hence, the unit bits per second (bps) is used (this has replaced the term baud in binary transmission systems).

Signaling rate is an important parameter when determining the bandwidth requirements of a data interchange circuit of a line driver, interconnecting media, and line receiver. The transmission of two successive state changes forms the beginning and end of a voltage and current pulse down the circuit. As one expects, there is a limit to how short the pulse duration can be to allow successful reception at the other end of the signal chain.

There must be signal quality criteria to specify or describe the minimum pulse duration or maximum signaling rate of a circuit. Many specifications describe the quality of a binary data pulse by the amount of time spent in transition between states relative to the duration of the pulse. TIA/EIA-644 and TIA/EIA-899 and other specifications define this criteria. These standards define the pulse duration as the unit interval or t_{UI} and the maximum transition times as a fraction of t_{UI}. Figure 2–5 shows the signal quality criteria from TIA/EIA-644-A.

[4]100E series, High Performance ECL Data, Motorola, DL140/D, 1995

[5]MC100EP16 Data Sheet, On Semiconductor, April 2001

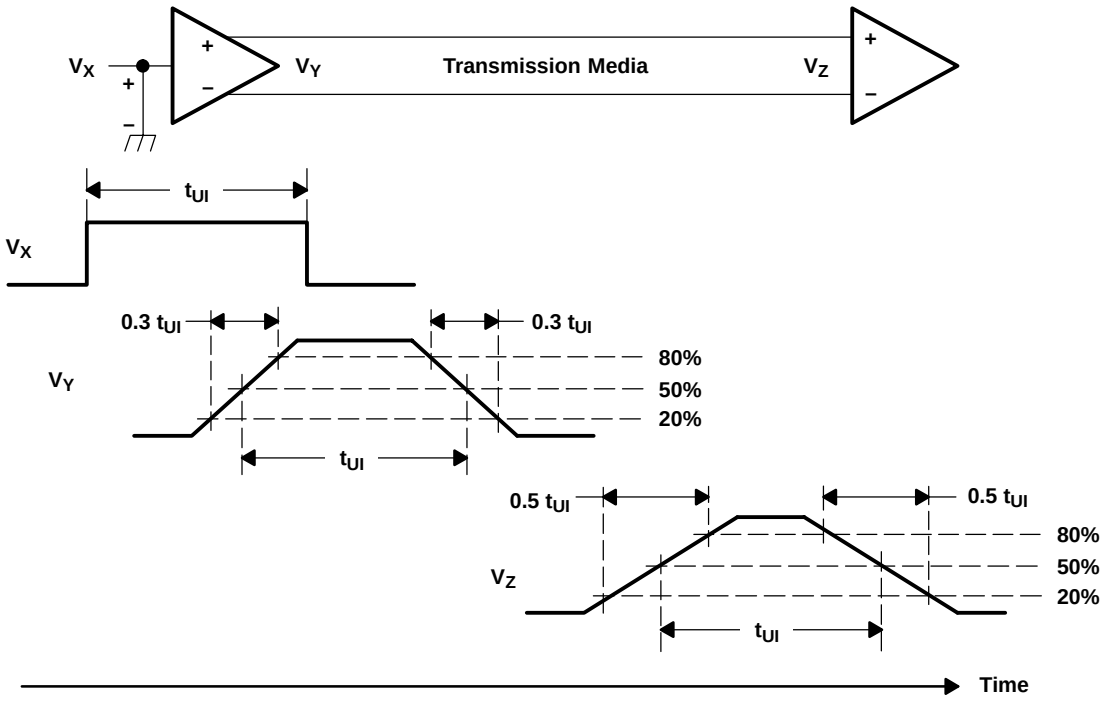


Figure 2–5. TIAS/EIA-644-A Signal Quality Recommendations

When the signal transition time reaches 0.5 t_{UI} at the end of the transmission line, we have achieved the minimum pulse duration and maximum signaling rate for a single interface circuit. When evaluating the signaling rate capability of the line circuits however, most assume a lossless line and apply the 0.3 t_{UI} limits to both the driver and receiver. (This is because the degradation of the transition time to 0.5 t_{UI} allows for losses in the transmission media and not the line circuits.) This implies that the signaling-rate capability of the line circuits can be determined by their output rise and fall times and, on first order, is a good approximation.

NOTE:

Figure 2–5 shows that the transition time is measured from the entire signal swing and not from the receiver threshold. For example, 0.5 t_{UI} transitions still allow the minimum duration pulse to attain a steady-state level.

Basing the signaling rate upon the real-time shape of the data pulse ignores when the bus state becomes valid relative to the sampling instant. Assuming that the sampling time is stable and repeats, any variation in time of the bus state change adds or subtracts from the set-up or hold time required for sampling. We generically call this variation jitter and it comes from several sources in the line circuits.

Ideally, a line driver or receiver reproduces a state change at the output some fixed time after it occurs at the input. In reality, the propagation delay time varies with temperature, supply voltage, manufacturing process, the preceding bit sequence, and noise. All of these factors affect when the state is valid for sampling and further processing. The interface designer must allocate a budget for each within the communication system's timing budget. There are few standard methods used to characterize and specify these variables, but we can make some general observations and conclusions.

The highest speed interface circuits normally transmit timing information along with the data, encoded either in the data or in a separate parallel circuit. The method of transmitting timing information (clock) determines which type of line-circuit jitter must be budgeted. In general, only high-frequency jitter components are a concern in clock-encoded data and all jitter components are budgeted in the parallel-clocking approach.

Propagation delay time variation with temperature or manufacturing process is very low in frequency and specified in the propagation delay time limiting values of device data sheets. Since most parallel circuits operate at the same temperature and supply voltage, data sheets specify an additional parameter called part-to-part skew or $t_{SK(PP)}$ to characterize manufacturing process variability only. This parameter is the propagation delay time of separately packaged line circuits when operated at the same supply voltage and temperature in the recommended operating range. A related parameter is output skew or $t_{SK(O)}$ and is the propagation delay time difference between two parallel circuits residing in the same integrated line circuit. In a monolithic device, the two circuits were subjected to the same manufacturing process and the delays are closely matched.

The state changes or bits that have occurred before a transition affect the initial operating points in the line circuit and the propagation delay time. Data sheets often specify two parameters for this effect. Pulse skew, or $t_{SK(P)}$, is simply the difference in the propagation delay of a high-to-low and a low-to-high transition from a steady-state input condition and represents the maximum pattern-dependent delay time variation. A subset of $t_{SK(P)}$ is the deterministic jitter or $t_{j(d)}$. This is a measurement of the delay time variation with a pseudo-random bit sequence and includes intermediate operating points for a statistical description of this jitter component. This jitter contribution is high in frequency (at or above the signaling rate).

Finally, the jitter contribution from noise is difficult to characterize and specify for line circuits and is best evaluated in the actual interface and environment. Data sheets may indicate noise-induced jitter in the typical characteristic sections of device data sheets that break out a random jitter parameter, show peak-to-peak jitter comparisons of multichannel line circuits under various operating combinations, graph propagation delay time versus common-mode or differential input voltage, or others.

Power Consumption

High signaling rates and low power are often mutually exclusive features of a data line interface. As the signal frequency increases, circuit impedances tend to decrease requiring more current to generate a voltage. Since power is the product of voltage and current, maintaining or reducing power levels requires a reduction in operating voltage. This is the impetus behind the development of LVDS and M-LVDS line circuits.

While the advantage of reducing supply and signal voltages is apparent, the authors designed both the LVDS and M-LVDS standards to minimize the amount of common-mode power by using a purely differential line termination with no low-impedance path to ground. This is most apparent when comparing LVDS to ECL circuits. The graph in Figure 2–6 shows a comparison between the power vs signaling rate characteristics of a 10-output ECL repeater and a 16-output LVDS repeater[6]. Even though the LVDS has 1.6 times the number of outputs, you can see that the LVDS device has roughly half the power dissipation. In fairness, you should note that most ECL/PECL devices run at higher maximum speeds than presently available LVDS devices, so there are some situations where the additional power of ECL/PECL is justified.

[6]SLLA103 *LVPECL and LVDS Power Comparison*, Texas Instruments Incorporated, 2001

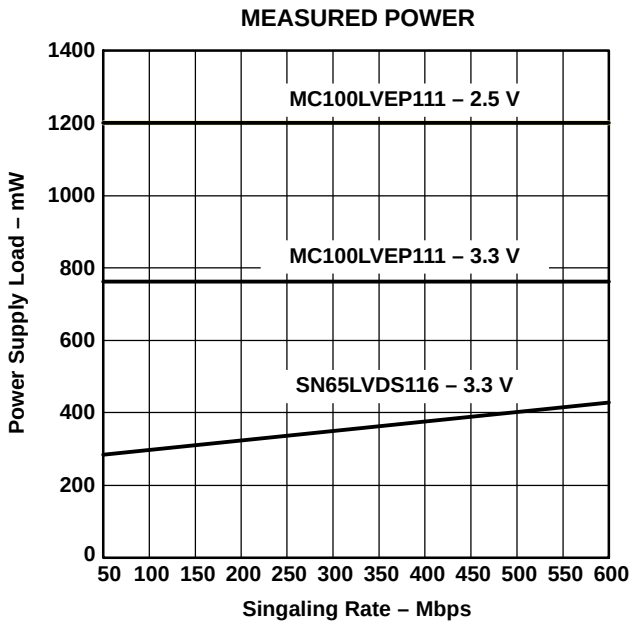


Figure 2–6. MC100LVEP111 and SN65LVDS116 Power Comparison

LVDS and M-LVDS drivers further reduce this wasted power by the common use of high impedance (relative to the load) outputs. Referring to Figure 2–7, as the source resistance (R_S) increases, I_O becomes less sensitive to changes in load resistance. This includes variation in R_L and, more importantly, the momentary internal shorts from R_S to ground that occur when transistors replace the ideal switches.

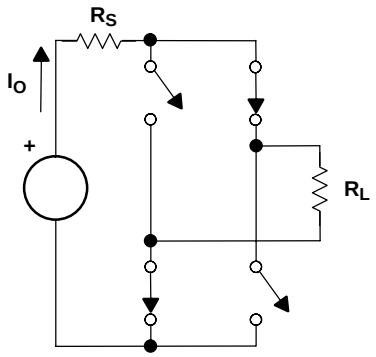


Figure 2–7. Differential Driver Circuit Model

When compared to drivers with relatively lower output impedance (such as most RS-422 and -485 drivers), high-impedance outputs result in more stable power consumption with increasing signaling rate. To illustrate, Figure 2–8 shows the normalized power consumption of the MAX3485 3.3-V RS-485 and SN65MLVD200 M-LVDS driver[7]. It is important to note that MAX3485 consumes 142 mW while the SN65MLVD200 only consumes 54 mW in the steady state and the signaling rate extends to 200 Mbps for the SN65MLVD200.

[7]SLLA106 *TIA/EIA-485 and M-LVDS, Power and Speed Comparison*, Texas Instruments Incorporated, 2001

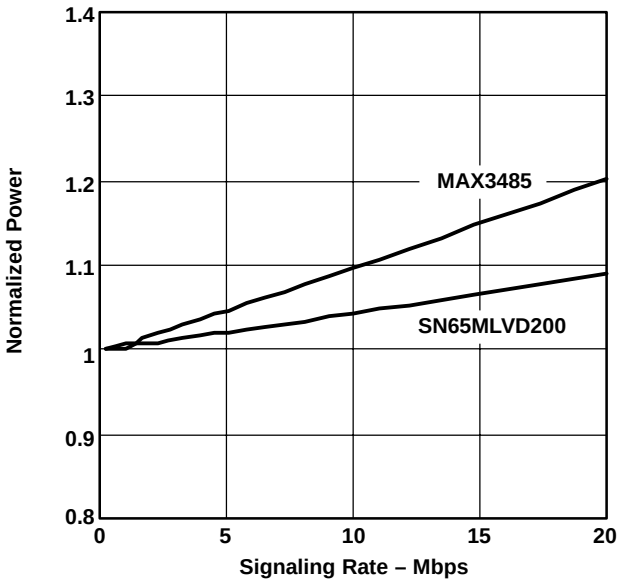


Figure 2–8. Normalized Power vs Speed Comparison of Voltage-Mode and Current-Mode Driver

Supply Voltage

The LVDS and M-LVDS standard levels were designed around a 3.3-V supply system but do not specify the supply voltage for interface circuits. Provided the designer meets the interface specifications, LVDS or M-LVDS integrated circuits can operate from any voltage. There are 5-V LVDS circuits and some that operate down to 2.5-V, such as the SN65LVDS1050.

Reliability

When operated within recommended operating conditions, interface circuits are as reliable as any other silicon-based circuit. However, exposure to transient noise coupled to long transmission lines or to static discharges through connector pins can damage interface circuits.

Although designers must treat noise in general application of interface circuits as random, manufacturers model certain recurring types of noise sources and specify the tolerances at the integrated-circuit level. Following is a brief overview of some of the more common models[8].

Human-Body Model (HBM)—The HBM simulates the action of a human body discharging accumulated static charge through a device to ground, and employs a series RC network consisting of a 100-pF capacitor and a 1500-Ω resistor.

Machine Model (MM)—The MM simulates a machine discharging accumulated static charge through a device to ground. It comprises a series RC network of a 200-pF capacitor, and nominal series resistance of less than 1 Ω. The output waveform usually is described in terms of peak current and oscillating frequency for a given discharge voltage.

Charged-Device Model (CDM)—The CDM simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occur when there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube and hitting a metal surface. The CDM addresses the possibility that a charge may reside on a lead frame or package (e.g., from shipping) and discharge through a pin that subsequently is grounded, causing damage to sensitive devices in the path. The parasitic impedance and capacitance of the device limit the discharge current. CDM testing consists of charging a package to a specified voltage, then discharging this voltage through the relevant package leads. TI conducts CDM testing using a field-induced CDM (FCDM) simulator.

[8]SSY010 *Electrostatic Discharge (ESD)*, Texas Instruments Incorporated, 2000

High specifications with any of the above noise models are an indication of how a device tolerates noise transients when installed in a printed-circuit card and an enclosure. Data sheets sometime specify the ESD tolerance separately for the bus pins (those connected to the transmission line) with respect to the supply pins, since these are the most susceptible after installation. Unfortunately, the installation has much to do with the ultimate performance in this regard and any claims of compliance with system-level specifications must come with complete specification of test conditions.

Texas Instruments offers LVDS devices with 15 kV of HBM ESD protection on the bus pins. This superior ESD performance is a direct result of the advanced analog silicon processes[9] used at TI, and is unavailable from most other vendors.

Integrated Terminations

Proper termination of a transmission line is necessary to reduce reflected signals. Reflected signals may lead to an increase in data errors, and so transmission system standards are very careful to define termination requirements. EIA/TIA-644-A defines a *terminating receiver* load in terms of a combination of line-termination impedance plus a receiver. The standard also defines the characteristics of receivers without line-termination impedances. The differential input impedance of a terminating receiver is to be between 90 Ω and 132 Ω, or approximately 111 Ω ±19%.

Although the standard does not state specifically how the line-termination impedance is to be physically located as a part of the terminating receiver, it does have several cautionary notices about not introducing stubs and reflections. The ideal location of the line termination is as close to the receiver as possible, which then has a near-zero stub length. Texas Instruments has integrated termination resistors into several LVDS receivers. This gives the ideal zero-length stub, in addition to saving end users the need for purchasing and installing external components.

Integrating the termination resistors with the receiver circuit is essentially impossible with standard digital silicon processes, as used in ASICs. The reason is that the majority of those processes are incapable of providing resistive components that can meet the tolerance requirements of the standard. The advanced analog processes used to fabricate TI's terminated receivers include proprietary additions that provide the needed stable resistive components.

The cost savings potential provided by using TI's internally terminated LVDS receivers includes the purchase and stocking costs; the fabrication, QC, and R&M costs; and the additional PC board area. The board space savings can be particularly significant in situations where multiple parallel signal paths are involved. Texas Instruments has available a family of 8- and 16-channel LVDS receivers, both with and without internal terminations. In addition to saving the 8 or 16 termination circuits for each of these devices, they ease the layout of PC-board traces and eliminate stubs for maintaining signal quality.

[9]See SLLA065 *A Comparison of LinBiCMOS and CMOS Processes Technologies for LVDS,* Texas Instruments Incorporated, 2000

Fault Tolerance and Failsafe Receivers

One area of performance that is described, but not always specified, in the standards is the area of fault conditions. These may include conditions where the driver power is off, the receiver is not connected, and the transmission line is open or short circuited. All of these conditions may cause the differential input voltage to fall within the transition region[10] of the receiver and cause an indeterminate output state. *Failsafe* defines the behavior of the receiving circuit under these fault conditions. The consequences of not including failsafe provisions are the detection of random noise as valid data or receiver oscillation; depending on the application, this could cause serious system response problems.

Experienced designers use a number of receiver design techniques to provide a predictable response from a receiver under these different fault conditions. With a differential input voltage within the transition regions, a small amount of positive feedback from the output stage of a receiver can cause the positive-going input threshold to be greater than the negative-going threshold creating hysteresis in the response. This feature prevents oscillation of the receiver output from differential noise below the hysteresis value. This failsafe feature does not force the output to a predetermined state but keeps in the last one before entering the transition region. Due to the sensitive thresholds and high signaling rates of LVDS and M-LVDS receivers, large amounts of hysteresis voltage is neither possible nor desirable. The data sheet for a receiver generally specifies the input hysteresis voltage in the electrical tables.

If the fault condition results in a high resistance or open circuit between the receiver inputs (such as a disconnected cable), most differential receivers from TI offer an open-circuit failsafe feature. This technique connects high-value internal resistors to pull the receiver inputs to a valid input voltage when the inputs are not connected to anything else. Data sheets specify open-circuit failsafe in the feature bullets, function tables, or equivalent input schematics of the data sheet.

The Type-2 receivers specified in the TIA/EIA-899 M-LVDS standard provide another means of failsafe response. The standard requires the Type-2 receiver to have a differential input voltage threshold offset from zero such that even shorted lines (0 V differential) provide a valid bus and receiver output state. Offset of the threshold does subtract from the noise margin and adds pulse distortion (jitter) over Type-1 receivers with thresholds near zero volts. Designers can use Type-2 receivers in parallel with Type-1 receivers to detect loss of input signal and gate the Type-1 receiver output.

TI introduced a more sophisticated fault detection and failsafe technique with the SN65LVDS33 family of receivers. This design employs additional circuitry to monitor the differential input voltage. If the differential input voltage remains in the transition region for more than 600 nanoseconds, the failsafe circuitry forces the outputs to a high state. This system detects the loss of signal conditions that can occur if the driver is off or disconnected, or if the transmission line is short-circuited[11].

Live Insertion (Hot Plugging)

Live insertion, hot plugging, and hot swap all describe adding or removing devices to or from a common data bus without removing power from the entire bus. Depending on the source, each term may take on a different significance in relation to a level of performance or isolation. Here, the term live insertion is used in a general sense meaning both insertion and removal of connections to a bus and power cycling of connected devices. The scope of live insertion design encompasses power-management as well as integrated circuit design, influencing all levels of design from system architecture to component selection.

At the electrical layer, two primary concerns with live insertion are part destruction and data corruption. Damage can occur if there are large potential differences between the bus and line circuit at insertion. Most equipment designed for live insertion assures that grounds are connected before the signal pins to equalize potentials. Even so, high-impedance circuits can retain charges and users must rely on the device ESD structures to discharge them. Here, high ESD ratings are beneficial. Contention with other drivers on the bus does not damage LVDS or M-LVDS circuits as the standards require output current limiting.

[10] See *Differential Input Voltage Threshold* section in this chapter.

[11] More on the active failsafe feature of the SN65LVDS33 can be found in SLLA082A.

In order not to disturb the bus signals during power cycling of a connected node, the line driver and receiver must appear as high impedance to the bus. Look for a receiver specification of the input current with the supply voltage at zero volts and a power-up/down glitch-free feature on the line driver. A power-up/down glitch-free driver is designed to keep the outputs off and high impedance below a certain supply voltage threshold regardless of input conditions. This allows stabilization of the driver inputs with either lower operating voltage logic or power sequencing. Often, the only indication of this feature is as a bullet on the front of the data sheet. If specified, it may show up as a test condition of the driver output current.

The left scope graph in Figure 2–9 shows the power-up and -down glitches seen on a driver output without this feature. The picture on the right is the SN65LVDS050 showing monotonic transitions during power cycling.

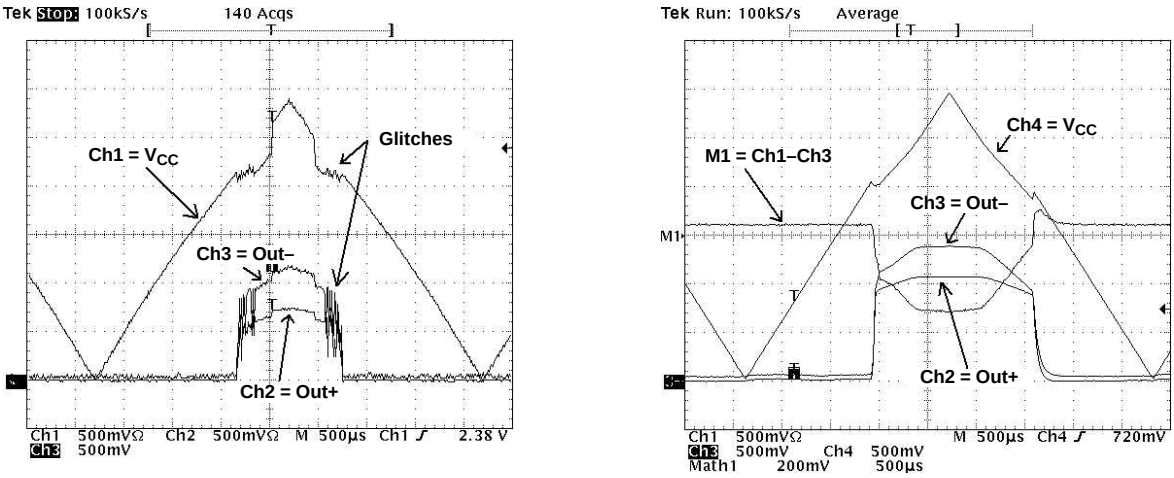


Figure 2–9. Power-Up/Down Waveforms

Chapter 3
Application Examples

Receiving Single-Ended Logic Levels

One of the problems in data interchange is the large number of electrical layers used for data transmission and the need to translate them to another level. LVDS and M-LVDS receivers possess the switching speeds and sensitivity to allow receipt of many of the common single-ended signals including 5-V TTL, LVTTL, 5-V CMOS, 3.3-V CMOS, 2.5-V CMOS, BTL, GTL, GTL+, and numerous others. All of these use binary signaling and indicate the logic state by a voltage level being above or below a certain threshold with respect to circuit ground.

Since LVDS and M-LVDS receivers are high-speed comparators with differential input voltage thresholds better than 100 mV, they can receive many single-ended logic signals with more noise margin than with standard input circuits. If the designer can accurately set the switching threshold in the middle of the input signal swing, the circuit is less susceptible to data errors due to noise. This technique also provides means to translate a variety of input signals to a common level for further level shifting or direct processing. The complementary inputs also offer a simple means of providing inverted and noninverted signals.

Figure 3–1 represents the input logic state by the output voltage V_O, which is attenuated or input directly to one input of the differential receiver. The receiver then compares the input voltage, V_I, to the threshold voltage, V_T, established at the other input by a reference circuit. When V_I is sufficiently above or below V_T, the receiver reproduces or inverts the logic state at the output of the receiver.

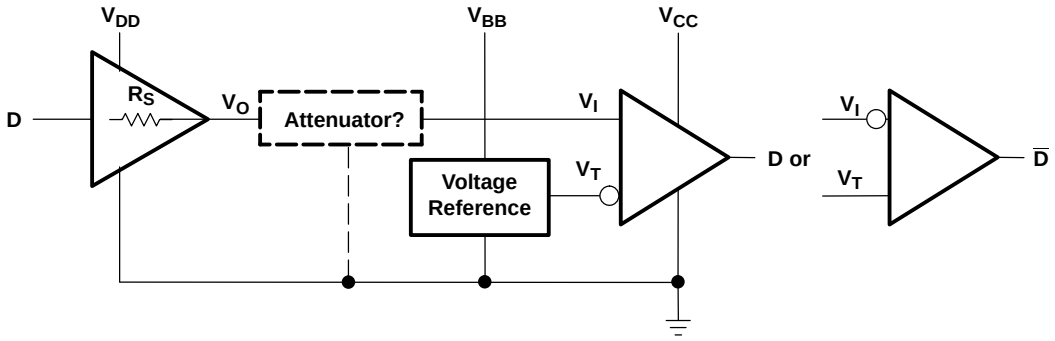


Figure 3–1. Circuit Blocks for Receiving Single-Ended Logic Signals

The characteristics of the driver and receiver circuits determine the requirement and design for the attenuator circuit block. It is only necessary when V_O goes beyond the input voltage range of the receiver. The input voltage range for TIA-EIA-644-A receivers is 0 V to 2.4 V and for TIA/EIA-899 receivers is –1.4 V to 3.8 V and can eliminate the need for attenuation of signals within those ranges. TI also offers the SN65LVDS33 and related LVDS receivers with an input voltage range of –4 V to 5 V that can eliminate the need for attenuation with wider driver supply ranges[12].

Should attenuation of V_O be necessary, the simple resistor divider in Figure 3–2 brings the highest output voltage within the receiver's range. The supply voltage of the upstream driver, V_{DD} bounds the highest voltage and sets the maximum gain (minimum attenuation) as $A = \frac{V_I}{V_O} \leq \frac{V_{DD(MAX)}}{V_{I(MAX)}}$ where $V_{I(MAX)}$ is the receiver's maximum input voltage specification. To prevent significant loading of the driver, the sum of R_1 and R_2 should be about 20 times the source resistance. To prevent the receiver input from loading down the attenuator, the current through R_1 and R_2 should be 20 times the input current of the receiver (20 x 20 μA for standard-compliant receivers).

[12]If the signaling rate allows, TIA/EIA-422 or -485 receivers have –7 V to 12 V input ranges that can eliminate any need to consider attenuation.

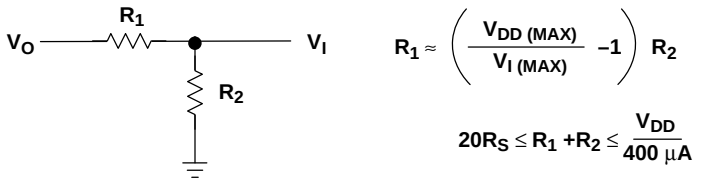
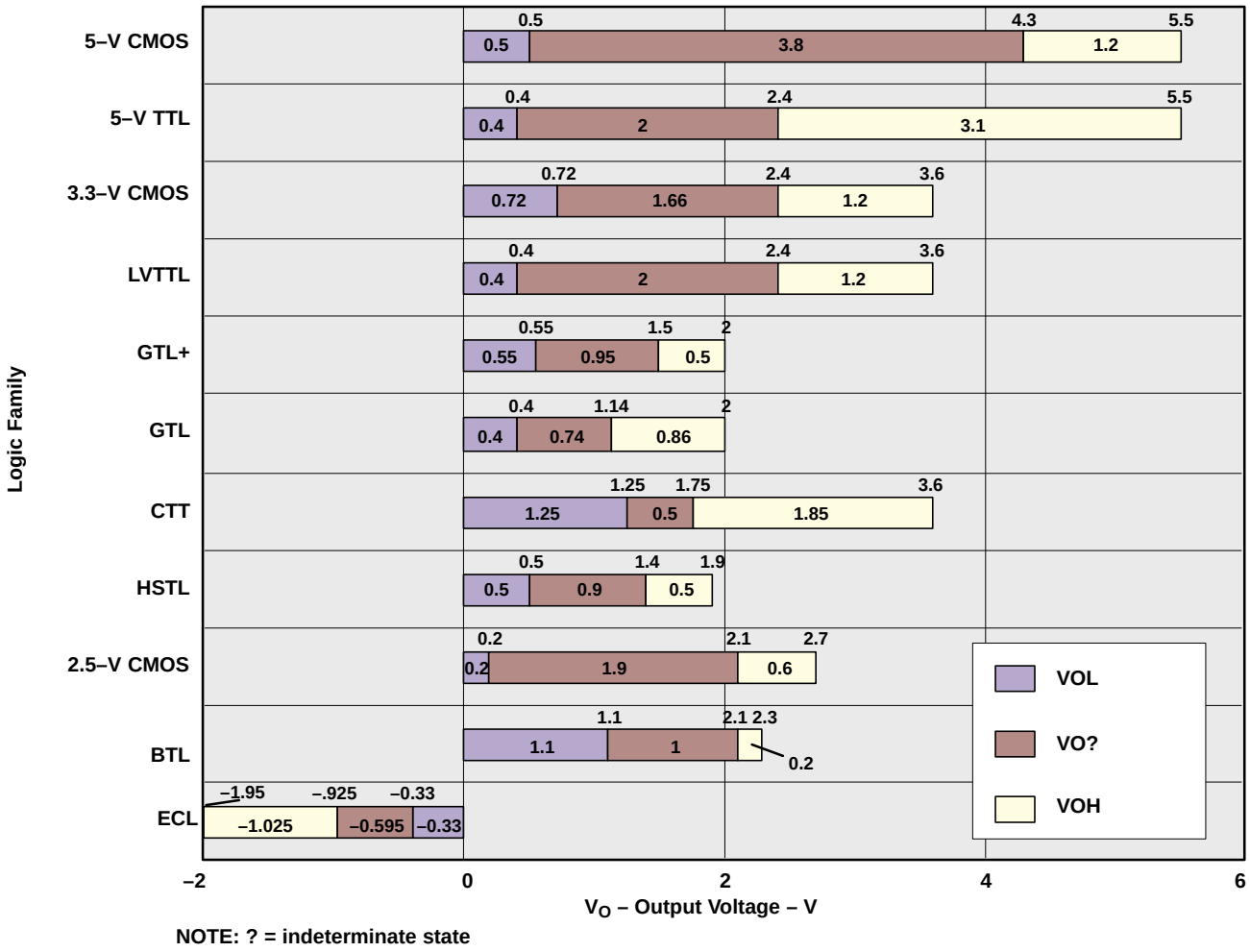


Figure 3–2. Simple Input Attenuator

Using a 5-V supplied driver with a maximum V_{OH} of 4 V at a supply of 5 V and an I_{OH} of –16 mA, gives $R_S = \frac{V_{DD}-V_{OH}}{-I_{OH}} = \frac{5-4}{0.016} = 62.5\ \Omega$ and, from Figure 3–2, $R_1 \approx \left(\frac{5.5}{2.4}-1\right)R_2 = 1.3R_2$ and $20 \times 62.5 \le R_1 + R_2 \le \frac{5}{400\ \mu A}$ or $1250\ \Omega \le R_1 + R_2 \le 12500\ \Omega$. R_1 and R_2 solutions are left to the reader.

The voltage reference circuit, setting the threshold for detecting a logic state change, is required; however, designers may use one reference circuit for other receiver circuits in the same interface. A switching threshold set to the average of the high-level and low-level output voltages attains the maximum noise margin. However, designers must use the worst-case voltages to specify V_T. Figure 3–3 shows the minimum high-level and maximum low-level output voltages for some of the more common logic families. From these, we derive the desired nominal V_T for each family using $V_T = \frac{V_{OH} + V_{OL}}{2}$.



NOTE: ? = indeterminate state

Figure 3–3. Single-Ended Logic Levels

Variation from the optimum V_T reduces the noise margin; designers must allocate a budget to the various noise contributors to determine the design tolerance for V_T. The budget greatly depends upon the specific application and reason for using this approach to receive the single-ended signal. If the reason for using a differential receiver is to improve noise margin and noise immunity, the switching threshold range must be smaller than that available with *standard* single-ended logic receivers. If the goal is level shifting or logical inversion, matching the standard input thresholds may be sufficient.

Figure 3–4 shows a likely portion of the voltage reference circuit along with the defining equations for component values. One-percent resistors are recommended (but not required) to make variation of V_{BB} the largest error contributor to V_T. If a supply line is used, ±5% variation can be expected on V_T. For CMOS switching levels, it is desirable to use the driver supply, V_{DD}, for V_{BB} as the optimum V_T is one-half of V_{DD}. If better control of V_{BB} is necessary, you can use an active voltage regulator circuit to achieve a tolerance of ±1%.

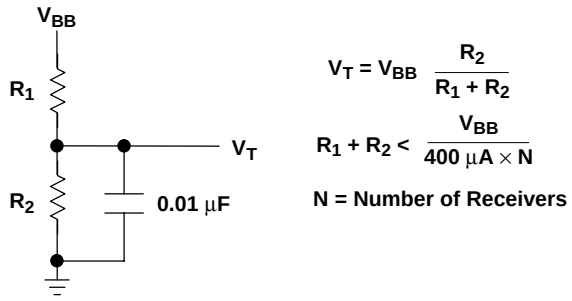


Figure 3–4. Voltage Divider Reference Circuit

In addition to the variation of V_T, the error budget should include the tolerance on the differential receiver's input voltage threshold. This is 100 mV for TIA/EIA-644-A receivers, 50 mV for TIA/EIA-899 receivers, or that specified for the chosen receiver.

Interface designers can use LVDS and M-LVDS receivers to receive a wide variety of single-ended logic levels, often with more noise margin (better noise immunity). These receivers also provide a convenient means to translate between different signaling levels or invert the logic of the signal. Output options for receivers currently include 3.3-V CMOS, LVDS, and LVPECL.

Receiving Other Differential Signals

You can create a differential interface circuit by simply employing two complementary single-ended signal lines using any of the signaling levels described in the previous section. In this case, replace the reference circuit of Figure 3–1 with the complementary signal under the same constraints and solution as the other line. However, there is an increasing number of purely differential and hybrid signaling standards that LVDS or M-LVDS receivers can receive.

IEEE-1394 (Firewire), LVD-SCSI, USB, Ethernet, Fibrechannel, and other interface standards use a form of low-voltage differential signaling compatible with the speeds and voltage levels of LVDS or M-LVDS receivers. On occasion, a designer may want to reproduce the bus signals at other logic levels. Figure 3–5 shows one such example where the electrical interface of a 100-Mbps IEEE-1394 is accomplished using an LVDS driver and receivers.

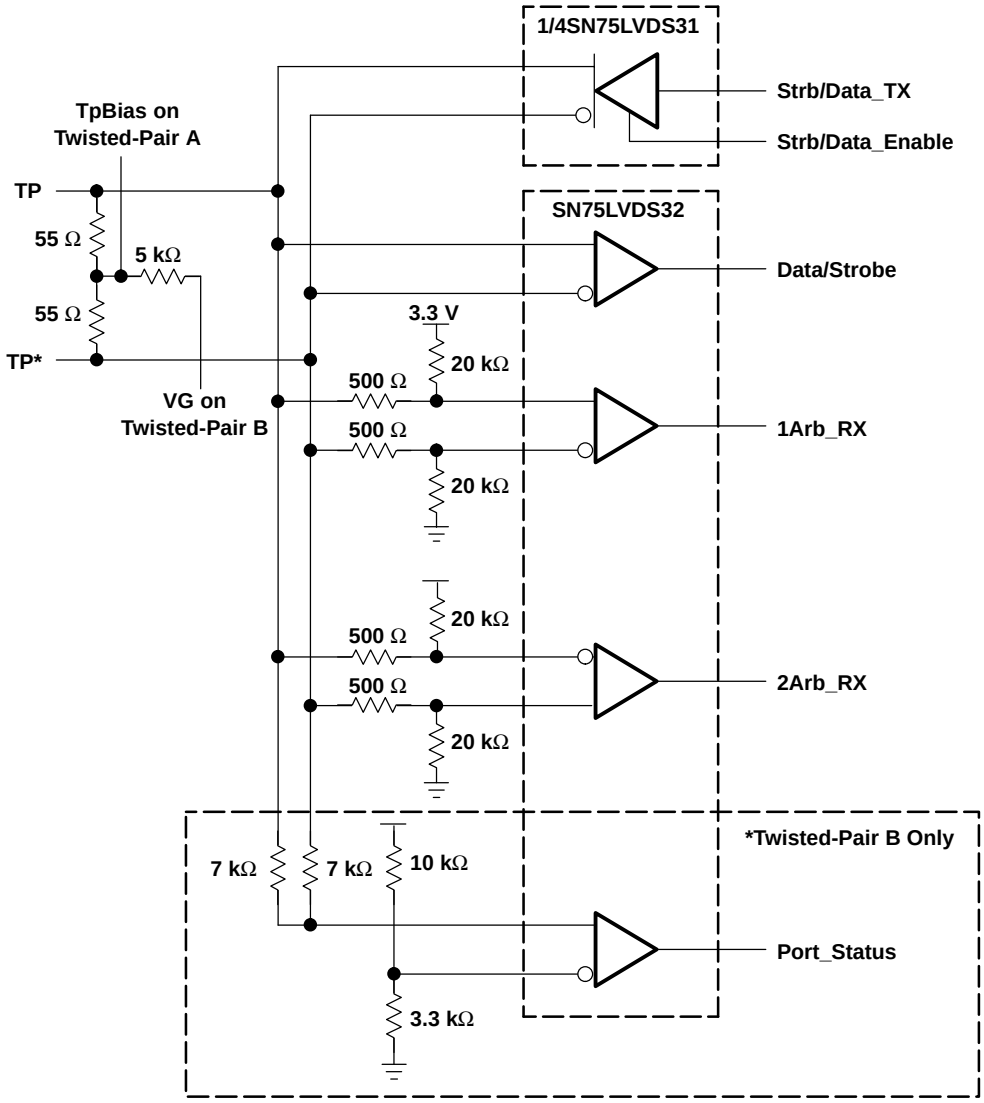


Figure 3–5. 100-Mbps IEEE-1394 Transceiver With LVDS

For non-LVDS-like signals, the –4 V to 5 V common-mode input voltage range of the SN65LVDS348 can be used advantageously to receive higher-voltage differential signals such as ECL, 5-V CML, TIA/EIA-422 (RS-422), or TIA/EIA-485 (RS-485). ECL driver outputs; including negative ECL (NECL), positive ECL (PECL), and low-voltage ECL (LVPECL), are typically loaded with 50 Ω biased to a dc termination voltage at least 2 V below the high-side supply voltage (due to the emitter-follower output structure). This results in the minimum and maximum levels for LVPECL, PECL, and NECL outputs given in Table 3–1.

Table 3–1. ECL Output Voltage Levels

	LVPECL	PECL	ECL
V_{OH} (Max)	2.42 V	4.120 V	–0.880 V
V_{OH} (Min)	2.275 V	3.975 V	–1.025 V
V_{OL} (Max)	1.68 V	3.380 V	–1.620 V
V_{OL} (Min)	1.49 V	3.190 V	–1.810 V

As can be seen, all of the ECL voltage levels lie within the common-mode voltage range of the SN65LVDS348 and the only external circuitry required is the ECL load of 50 Ω terminated to 2 V below the high-side source supply line. You can implement this as shown in Figure 3–6, where the Thevenin equivalent of the resistor divider provides the required ECL terminations.

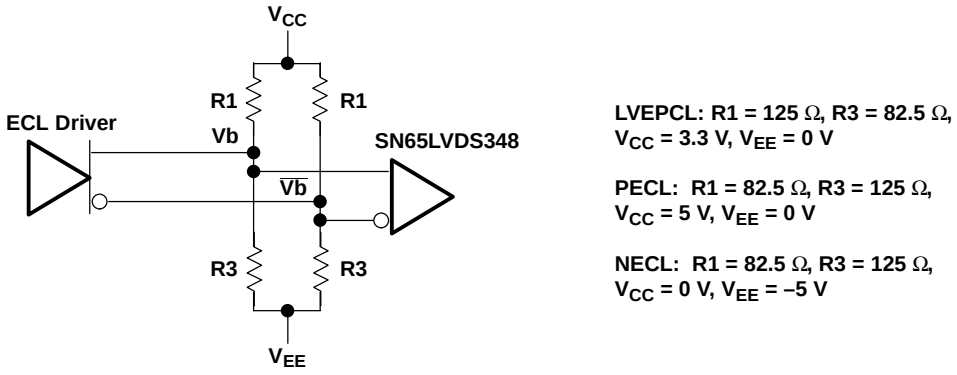


Figure 3–6. ECL-to-CMOS Conversion With the SN65LVDS348

At 400 mV, the differential voltage swing of CML (current-mode logic) is well within the TIA/EIA-644-A specification. Unfortunately, the common-mode voltage levels of 5-V CML are beyond the 2.4-V VICR specified in the standard. Since the voltage swing is relatively small and voltage division can create a differential voltage below the 100-mV minimum input differential voltage, the standard-compliant alternative is ac coupling. However, a wide common-mode device, such as the SN65LVDS348, can avoid the coupling capacitors and a voltage divider reducing the CML-to-CMOS translation circuit to that shown in Figure 3–7.

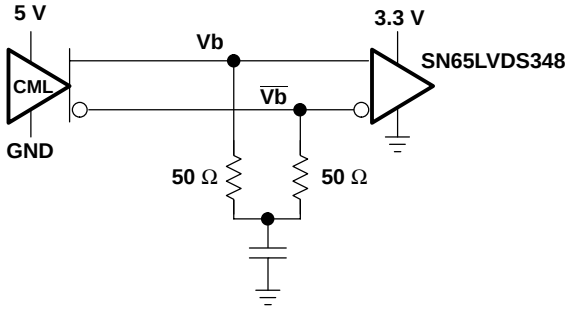


Figure 3–7. CML-to-CMOS Translation With the SN65LVDS348

RS-485 receiver requirements encompass those of the RS-422 receiver with an input voltage range of –7 V to 12 V and a minimum V_{IT} of –200 mV and maximum of 200 mV. The SN65LVDS348 receiver can implement fully compliant RS-485 or RS-422 receiver using the circuit shown in Figure 3–8.

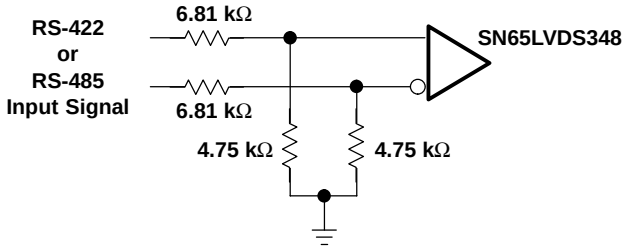


Figure 3–8. RS-422/485-to-CMOS Translator With the SN65LVS348

The significance of the wide common-mode device is great. The wide common-mode device satisfies the output extremes of NECL, PECL, CML, and 422, without excessive component addition. This gives designers flexibility to replace a legacy receiver with a wide common-mode LVDS part and still maintain operation. In the

single-ended case, this can result in an increase in noise margin. In the differential case, the replacement provides for the future upgrade to an LVDS driver, allowing future circuits to benefit from the low power, EMI, and crosstalk of LVDS.

Adjusting LVDS Output Levels

There may be cases where the standard differential output levels of LVDS may not provide sufficient noise margin. This noise could come from a low characteristic impedance transmission media from loading, impedance mismatches from connectors or stub lines, a lossy cable, a long haul, or any combination of these factors. Most, but not all, LVDS and M-LVDS drivers are fixed-current outputs such that the output voltage levels (and differential noise margin) can be increased linearly by connecting driver outputs in parallel.

Figure 3–9 shows the differential output current versus differential output voltage of the SN65LVDS31 quadruple LVDS driver. In the differential output voltage range of 0.1 V to 1 V, the steady-state output closely resembles an ideal 4.2-mA current source in parallel with 890 Ω as shown in Figure 3–10.

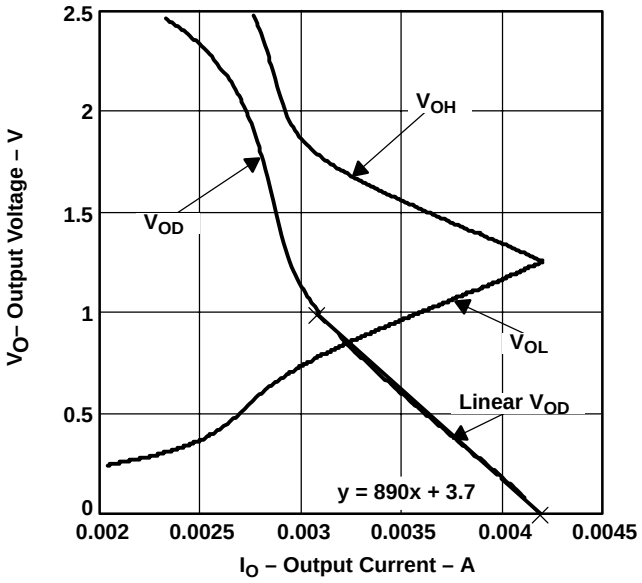


Figure 3–9. SN65LVDS31 Output Current vs Voltage

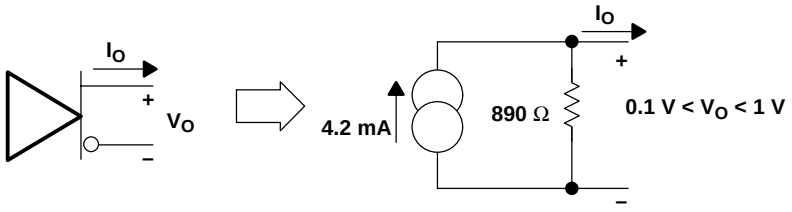


Figure 3–10. Equivalent Circuit of SN65LVDS31 Steady-State Differential Output

If users want to increase the signal into a 100-Ω transmission line by connecting *n* drivers in parallel, our model predicts a differential output of 377 mV for n=1, 685 mV for n=2, 942 mV for n=3. Indeed, the eye patterns for parallel-connected drivers shown in Figure 3–11 reveal outputs very near these predicted values and verify our typical model. Notice that the eye patterns show no noticeable increase in the zero-crossing jitter with additional drivers.

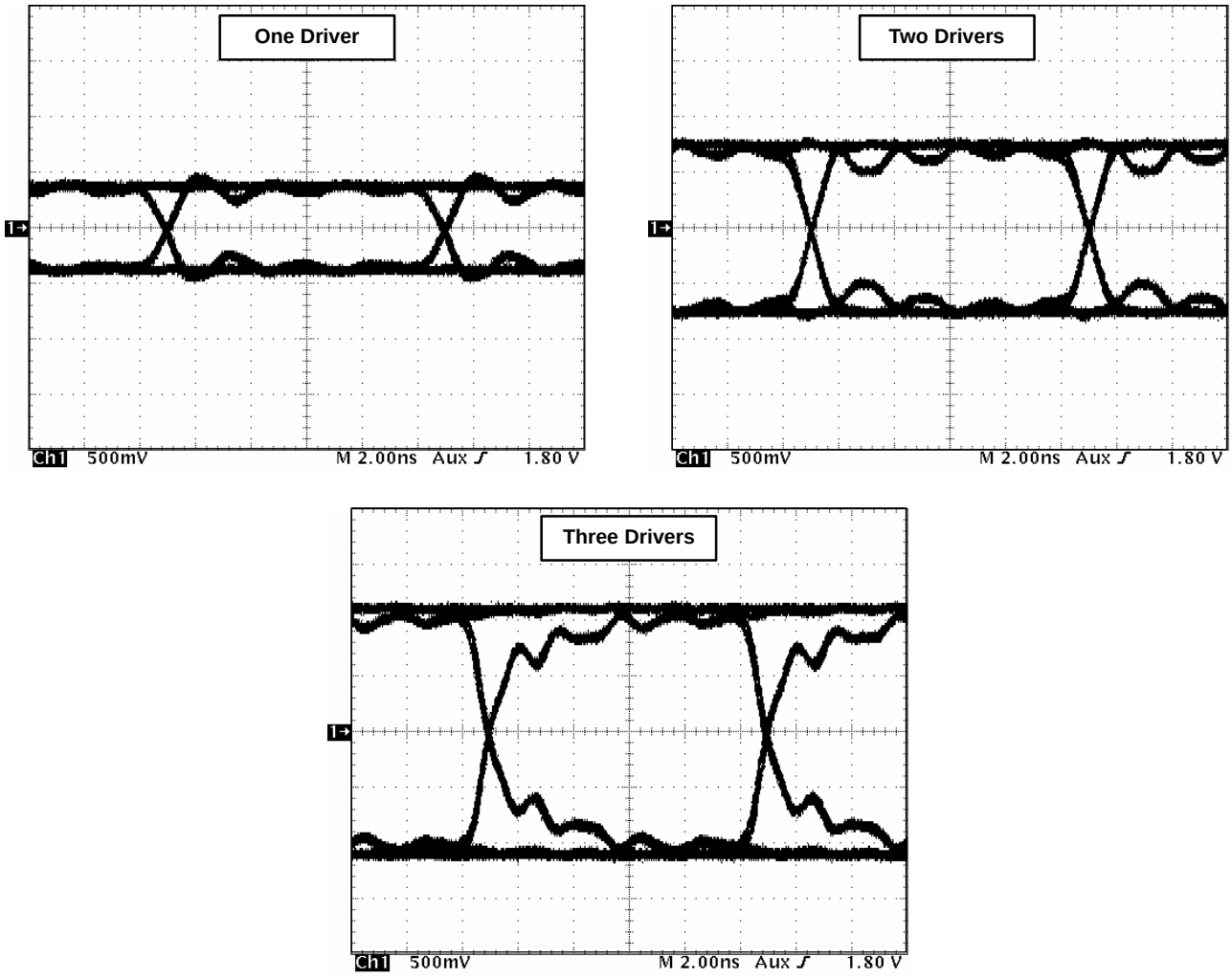


Figure 3–11. Eye Patterns for Multiple Drivers and 100-Ω Loads

If the load is decreased to 27 Ω, our driver model indicates four drivers in parallel should return the signal level to 404 mV and standard LVDS. Figure 3–12 shows this to be the case with a steady-state differential output of 400 mV. Some overshoot of the signal is observed and can be attributed to the less than ideal connection to the load imposed by the test fixture used. It is also interesting that the zero-crossing jitter does not increase noticeably over that with a single driver.

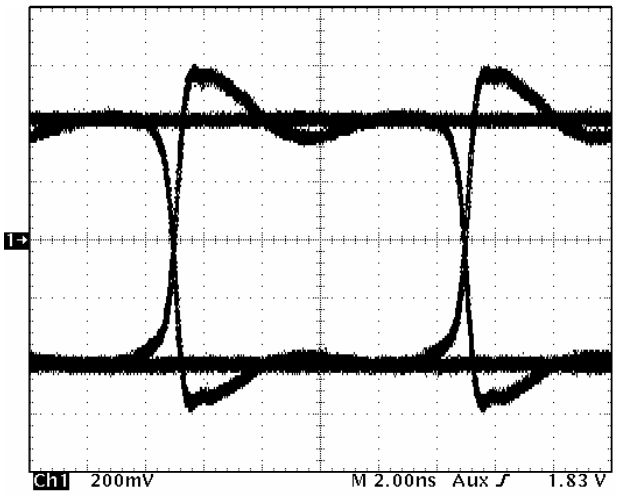


Figure 3–12. Eye Patterns With Four Parallel Drivers Into a 27-Ω Load

Increasing steady-state margin is not the only reason that parallel connection of current-mode drivers may be beneficial. In long or very lossy transmission lines, we know that the high-frequency components of a signal suffer higher attenuation. What if we could increase only the high-frequency signals at the driver to account for this larger attenuation? The circuit shown in Figure 3–13 accomplishes this by adding a high-pass filter to the output of one of a pair of drivers.

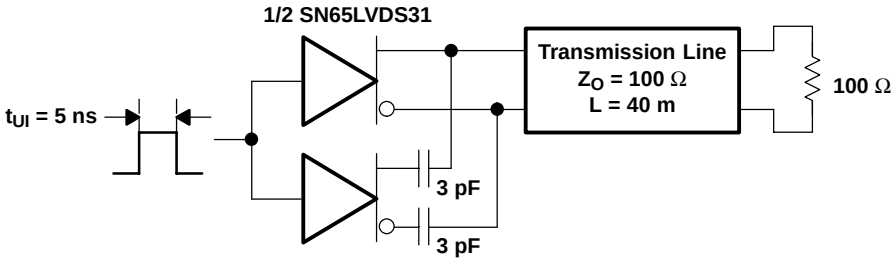


Figure 3–13. Precompensation Circuits With Two Drivers

Figure 3–14 shows the resultant eye patterns at the output of the driver (lower trace) and at the end of the cable (upper trace) for a 200-Mbps PRBS with and without the precompensation driver. Precompensation opens the eye by approximately 40% allowing lower bit-error rates or longer cables. The amount of high-frequency boost can be increased by adding more filtered drivers in parallel. The series capacitors of Figure 3–13 were chosen from standard values and for a –3-dB frequency of 100 MHz (1/2 the signaling rate in Hertz) using $f_0 = 1/2\pi RC$, where R is the parallel combination of the source resistance of the two drivers (890/2) plus the characteristic impedance of the line (100 Ω), or 545 Ω.

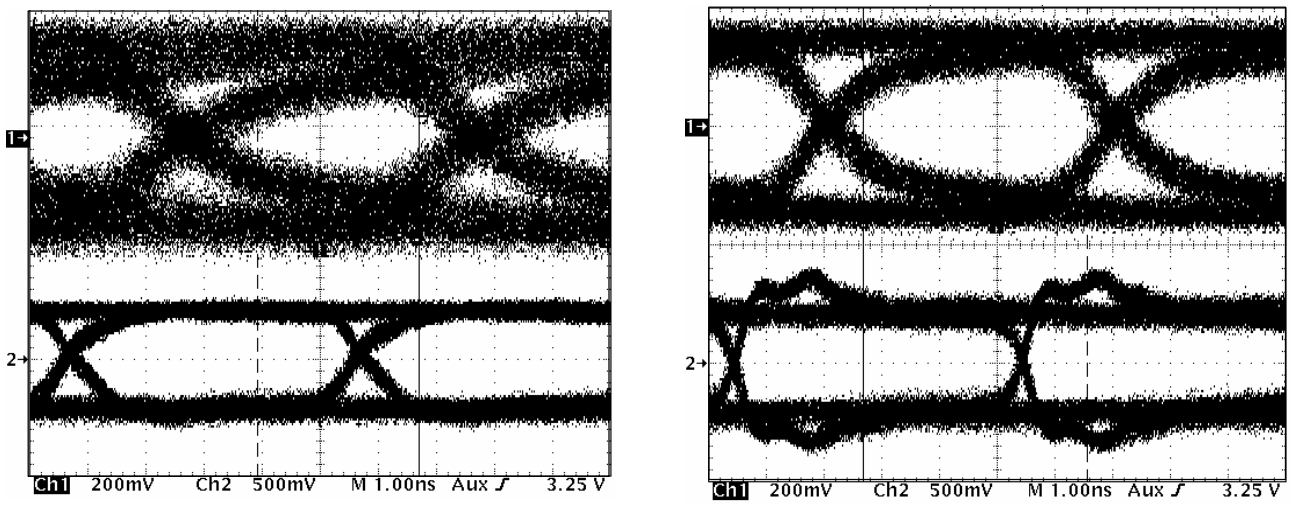


Figure 3–14. Eye-Patterns With and Without Precompensation

One advantage of the current-mode outputs of many LVDS drivers is the flexibility to add or subtract output current to the load as needed by nonstandard data transmission applications. Application of additional signal can increase steady-state noise margins, open eye patterns for lossy transmission lines, or increase cable length.

Chapter 4
Product Selection

Texas Instruments offers well over 160 part numbers in the LVDS line at the time of publication, with more in development. While this increases the options available to the designer, it does present a challenge in finding the best solution. This chapter provides the part numbering convention, definitions, and selection guides for general classes of circuit functions, and an industry cross reference.

Figure 4–1 illustrates the general part numbering convention for TI's LVDS products. The part number can often be used for initial product selection but readers are cautioned to always refer to the most recent version of the product specification before making any design decisions.

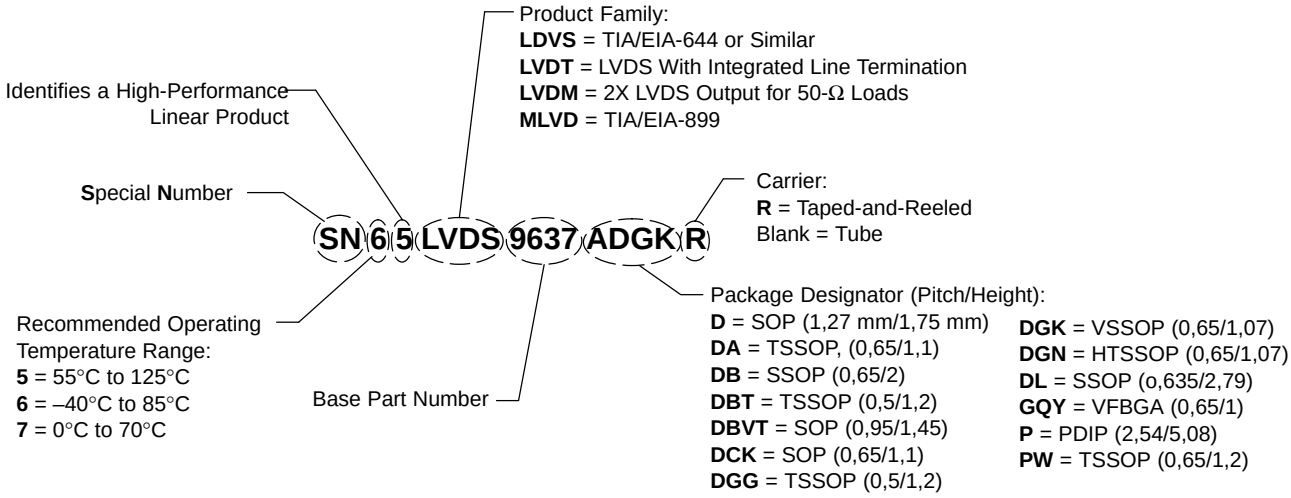


Figure 4–1. TI's LVDS Part Numbering Convention

Cross-Point Switches

The first selection guide contains the cross-point switches. A cross-point switch, also known as a crossbar or NxN switch, is a device that provides a fixed number of inputs and outputs to be able to keep a number of nodes communicating at full speed with other nodes. Users can program these devices to perform the function of an N-port repeater and N-input multiplexer as well as perform dynamic or static signal routing.

All of the cross-point switches listed in Table 4–1 use LVDS on the signal lines and operate from 3.3-V supplies.

Table 4–1. Cross-Point Switches

MATERIAL	INPUT/OUTPUTS	V_{IT} (mV)	V_{ICR} (V)	OPEN-CIRCUIT FAILSAFE?	SIGNALING RATE (Mbps)	R_L (Ω)	BUS-PIN ESD (kV)	PAGE
SN65LVDM22D	2x2	50	2.4	Yes	400	50	12	5–7
SN65LVDM22PW	2x2	50	2.4	Yes	400	50	12	5–7
SN65LVDS122D	2x2	50	4	Yes	1500	100	8	5–45
SN65LVDS122PW	2x2	50	4	Yes	1500	100	8	5–45
SN65LVDS125DBT	4x4	50	4	Yes	1500	100	8	5–75
SN65LVDS22D	2x2	100	2.4	Yes	400	100	12	5–7
SN65LVDS22PW	2x2	100	2.4	Yes	400	100	12	5–7
SN65LVDT122D	2x2	50	4	No	1500	100	8	5–45
SN65LVDT122PW	2x2	50	4	No	1500	100	8	5–45
SN65LVDT125DBT	4x4	50	4	No	1500	100	8	5–75

Serializers/Deserializers

A serializer takes parallel data, such as a 10-bit signal, and converts it into a serial stream for transmission on a serial link. At the other end, a deserializer converts the serial data back to parallel. This is done to reduce the cost and size of the interconnect. All of the serializer and deserializer circuits listed in Table 4–2 operate from a 3.3-V supply.

Table 4–2. Serializers and Deserializers

MATERIAL	FUNCTION	INPUTS	OUTPUTS	CLOCK LINE?	CLOCK FREQUENCY RANGE (MHz)	BUS-PIN ESD (kV)	PAGE
SN65LVDS150PW	Clock generator	1 LVDS	1 LVDS	Yes	5 to 50	12	5–47
SN65LVDS151DA	Serializer	10 LVTTL	1 LVDS	Yes	5 to 50	12	5–49
SN65LVDS152DA	Deserializer	1 LVDS	10 LVTTL	Yes	5 to 50	12	5–51
SN65LVDS93DGG	Serializer	28 LVTTL	5 LVDS	Yes	20 to 65	6	5–23
SN65LVDS95DGG	Serializer	21 LVTTL	4 LVDS	Yes	20 to 65	6	5–31
SN65LVDS96DGG	Deserializer	4 LVDS	21 LVTTL	Yes	20 to 65	4	5–33
SN65LV1021DB	Serializer	10 LVTTL	1 LVDS	No	10 to 40	NA	5–67
SN65LV1023DB	Serializer	10 LVTTL	1 LVDS	No	30 to 66	NA	5–69
SN65LV1212DB	Deserializer	1 LVDS	10 LVCMOS	No	10 to 40	NA	5–67
SN65LV1224DB	Deserializer	1 LVDS	10 LVCMOS	No	30 to 66	NA	5–69

Line Driver and Receivers

The devices listed in Table 4–3 contain a combination of stand-alone LVDS, LVDM, or M-LVDS line drivers and receivers. All operate from a 3.3-V supply, have LVCMOS receiver outputs, and LVTTL driver inputs.

Table 4–3. Driver and Receiver Combinations Devices

MATERIAL	RECEIVERS	V_{IT} (mV)	V_{ICR} (V)	OPEN-CIRCUIT FAILSAFE?	IDLE-LINE FAILSAFE?	DRIVERS	R_L (Ω)	BUS-PIN ESD (kV)	PAGE
SN65LVDM179BD	1	50	2.4	Yes	No	1	50	12	5–25
SN65LVDM179D	1	50	2.4	Yes	No	1	50	12	5–25
SN65LVDM179DGK	1	50	2.4	Yes	No	1	50	12	5–25
SN65LVDM180BD	1	50	2.4	Yes	No	1	50	12	5–25
SN65LVDM180D	1	50	2.4	Yes	No	1	50	12	5–25
SN65LVDM180PW	1	50	2.4	Yes	No	1	50	12	5–25
SN65LVDS179D	1	100	2.4	Yes	No	1	100	12	5–23
SN65LVDS179DGK	1	100	2.4	Yes	No	1	100	12	5–23
SN65LVDS180D	1	100	2.4	Yes	No	1	100	12	5–23
SN65LVDS180PW	1	100	2.4	Yes	No	1	100	12	5–23
SN65MLVD202D	1	50	5.2	No	No	1	30	3	5–55
SN65MLVD203D	1	50	5.2	No	No	1	30	3	5–55
SN65MLVD205D	1	50	5.2	Yes	Yes	1	30	3	5–55
SN75LVDS179D	1	100	2.4	Yes	No	1	100	12	5–23
SN75LVDS179DGK	1	100	2.4	Yes	No	1	100	12	5–23
SN75LVDS180D	1	100	2.4	Yes	No	1	100	12	5–23
SN75LVDS180PW	1	100	2.4	Yes	No	1	100	12	5–23
SN65LVDT41PW	1	100	2.4	Yes	No	4	100	16	5–5
SN65LVDM050BD	2	50	2.4	Yes	No	2	50	12	5–25
SN65LVDM050D	2	50	2.4	Yes	No	2	50	12	5–25
SN65LVDM050PW	2	50	2.4	Yes	No	2	50	12	5–25
SN65LVDM051BD	2	50	2.4	Yes	No	2	50	12	5–25
SN65LVDM051D	2	50	2.4	Yes	No	2	50	12	5–25
SN65LVDM051PW	2	50	2.4	Yes	No	2	50	12	5–25
SN65LVDS050D	2	100	2.4	Yes	No	2	100	12	5–23
SN65LVDS050PW	2	100	2.4	Yes	No	2	100	12	5–23
SN65LVDS051D	2	100	2.4	Yes	No	2	100	12	5–23
SN65LVDS051PW	2	100	2.4	Yes	No	2	100	12	5–23
SN65LVDS1050PW	2	100	2.4	Yes	No	2	100	12	5–71
SN75LVDS050D	2	100	2.4	Yes	No	2	100	12	5–77
SN75LVDS050PW	2	100	2.4	Yes	No	2	100	12	5–77
SN75LVDS051D	2	100	2.4	Yes	No	2	100	12	5–77
SN75LVDS051PW	2	100	2.4	Yes	No	2	100	12	5–77
SN75LVDS9638D	2	100	2.4	Yes	No	2	100	8	5–79
SN75LVDS9638DGK	2	100	2.4	Yes	No	2	100	8	5–79
SN75LVDS9638DGN	2	100	2.4	Yes	No	2	100	8	5–79
SN65LVDT14PW	4	100	2.4	Yes	No	1	100	16	5–5

Line Transceivers

Line transceivers have bidirectional IOs to or from the bus line for half-duplex or multipoint interconnections.

Table 4–4. LVDM and M-LVDS Transceivers

MATERIAL	TRANS-CEIVERS	V_{IT} (mV)	V_{ICR} (V)	OPEN-CIRCUIT FAILSAFE?	IDLE-LINE FAILSAFE?	OUTPUT	R_L (Ω)	BUS-PIN ESD (kV)	V_{CC} (V)	PAGE
SN65LVDM176BD	1	50	2.4	Yes	No	LVDM	50	15	3.3	5–53
SN65LVDM176D	1	50	2.4	Yes	No	LVDM	50	15	3.3	5–53
SN65LVDM176DGK	1	50	2.4	Yes	No	LVDM	50	15	3.3	5–53
SN65MLVD200D	1	50	5.2	No	No	899	30	3	3.3	5–55
SN65MLVD201D	1	50	5.2	No	No	899	30	3	3.3	5–55
SN65MLVD204D	1	50	5.2	Yes	Yes	899	30	3	3.3	5–55
SN65LVDM320DGG	8	50	2.4	Yes	No	LVDM	50	12	3.3	5–57
SN75LVDM976DGG	9	30	2.4	No	No	LVD–SCSI	30	N/A	5	5–65
SN75LVDM976DL	9	30	2.4	No	No	LVD–SCSI	30	N/A	5	5–65
SN75LVDM977DGG	9	30	2.4	No	No	LVD–SCSI	30	N/A	5	5–65
SN75LVDM977DL	9	30	2.4	No	No	LVD–SCSI	30	N/A	5	5–65
SN65LVDM1676DGG	16	50	2.4	Yes	No	LVDM	50	12	3.3	5–73
SN65LVDM1677DGG	16	50	2.4	Yes	No	LVDM	50	12	3.3	5–73

Line Receivers

All of the receivers listed in Table 4–5 operate from a 3.3-V supply and have CMOS outputs.

Table 4–5. LVDS Receivers

MATERIAL	RECEIVERS	V_{IT} (mV)	V_{ICR} (V)	R_T (Ω)	OPEN-CIRCUIT FAILSAFE?	IDLE-LINE FAILSAFE?	BUS-PIN ESD (kV)	PAGE
SN65LVDS2D	1	100	2.4	No	Yes	No	12	5–3
SN65LVDS2DBVT	1	100	2.4	No	Yes	No	12	5–3
SN65LVDS2GQY	1	100	2.4	No	Yes	No	12	5–3
SN65LVDT2D	1	100	2.4	110	Yes	No	12	5–3
SN65LVDT2DBVT	1	100	2.4	110	Yes	No	12	5–3
SN65LVDS9637BD	2	50	2.4	No	Yes	Yes	15	5–15
SN65LVDS9637D	2	100	2.4	No	Yes	No	8	5–13
SN65LVDS9637DGK	2	100	2.4	No	Yes	No	8	5–13
SN65LVDS9637DGN	2	100	2.4	No	Yes	No	8	5–13
SN75LVDS9637D	2	100	2.4	No	Yes	No	8	5–81
SN75LVDS9637DGK	2	100	2.4	No	Yes	No	8	5–81
SN75LVDS9637DGN	2	100	2.4	No	Yes	No	8	5–81
SN65LVDS34D	2	50	9	No	Yes	No	15	5–17
SN65LVDT34D	2	50	9	110	Yes	Yes	15	5–17
SN65LVDT9637BD	2	100	9	110	Yes	Yes	15	5–15
SN65LVDS048AD	4	100	2.4	No	Yes	No	10	5–21
SN65LVDS048APW	4	100	2.4	No	Yes	No	10	5–21
SN65LVDS32D	4	100	2.4	No	Yes	No	8	5–13
SN65LVDS32PW	4	100	2.4	No	Yes	No	8	5–13
SN65LVDS3486D	4	100	2.4	No	Yes	No	8	5–13
SN65LVDS3486PW	4	100	2.4	No	Yes	No	8	5–13
SN65LVDS390D	4	100	2.4	No	Yes	No	15	5–61

Table 4–5. LVDS Receivers (Continued)

MATERIAL	RECEIVERS	V_{IT} (mV)	V_{ICR} (V)	R_T (Ω)	OPEN-CIRCUIT FAILSAFE?	IDLE-LINE FAILSAFE?	BUS-PIN ESD (kV)	PAGE
SN65LVDS390PW	4	100	2.4	No	Yes	No	15	5–61
SN75LVDS32D	4	100	2.4	No	Yes	No	8	5–81
SN75LVDS32PW	4	100	2.4	No	Yes	No	8	5–81
SN75LVDS390D	4	100	2.4	No	Yes	No	15	5–61
SN75LVDS390PW	4	100	2.4	No	Yes	No	15	5–61
SN75LVDT390D	4	100	2.4	No	Yes	No	15	5–61
SN75LVDT390PW	4	100	2.4	No	Yes	No	15	5–61
SN65LVDT390D	4	100	2.4	110	Yes	No	15	5–61
SN65LVDT390PW	4	100	2.4	110	Yes	No	15	5–61
SN65LVDS32BD	4	50	9	No	Yes	Yes	15	5–15
SN65LVDS33D	4	50	9	No	Yes	Yes	15	5–17
SN65LVDS33PW	4	50	9	No	Yes	Yes	15	5–17
SN65LVDS3486BD	4	50	9	No	Yes	Yes	15	5–15
SN65LVDS348D	4	50	9	No	Yes	No	15	5–59
SN65LVDS348PW	4	50	9	No	Yes	No	15	5–59
SN65LVDS352PW	4	50	9	No	Yes	Yes	15	5–59
SN65LVDT32BD	4	50	9	110	Yes	Yes	15	5–15
SN65LVDT33D	4	50	9	110	Yes	Yes	15	5–17
SN65LVDT33PW	4	50	9	110	Yes	Yes	15	5–17
SN65LVDT3486BD	4	50	9	110	Yes	Yes	15	5–15
SN65LVDT348D	4	50	9	110	Yes	Yes	15	5–59
SN65LVDT348PW	4	50	9	110	Yes	Yes	15	5–59
SN65LVDT352PW	4	50	9	110	Yes	Yes	15	5–59
SN65LVDS388ADBT	8	100	2.4	No	Yes	No	15	5–61
SN65LVDS388DBT	8	100	2.4	No	Yes	No	15	5–61
SN75LVDS388ADBT	8	100	2.4	No	Yes	No	15	5–61
SN75LVDS388DBT	8	100	2.4	No	Yes	No	15	5–61
SN75LVDT388ADBT	8	100	2.4	No	Yes	No	15	5–61
SN75LVDT388DBT	8	100	2.4	No	Yes	No	15	5–61
SN65LVDT388ADBT	8	100	2.4	110	Yes	No	15	5–61
SN65LVDT388DBT	8	100	2.4	110	Yes	No	15	5–61
SN65LVDS386DGG	16	100	2.4	No	Yes	No	15	5–61
SN75LVDS386DGG	16	100	2.4	No	Yes	No	15	5–61
SN75LVDT386DGG	16	100	2.4	No	Yes	No	15	5–61
SN65LVDT386DGG	16	100	2.4	110	Yes	No	15	5–61

Line Drivers

All of the line drivers listed in Table 4–6 operate from a 3.3-V supply and have LVTTL inputs.

Table 4–6. Line Drivers

MATERIAL	DRIVERS	R_L (Ω)	BUS-PIN ESD (kV)	PAGE
SN65LVDS1D	1	100	15	5–3
SN65LVDS1DBVT	1	100	15	5–3
SN65LVDS9638D	2	100	8	5–9
SN65LVDS9638DGK	2	100	8	5–9
SN65LVDS9638DGN	2	100	8	5–9
SN65LVDS047D	4	100	10	5–19
SN65LVDS047PW	4	100	10	5–19
SN65LVDS31D	4	100	8	5–9
SN65LVDS31PW	4	100	8	5–9
SN65LVDM31D	4	50	12	5–9
SN65LVDS3487D	4	100	8	5–9
SN65LVDS3487PW	4	100	8	5–9
SN65LVDS391D	4	100	15	5–63
SN65LVDS391PW	4	100	15	5–63
SN75LVDS31D	4	100	8	5–79
SN75LVDS31PW	4	100	8	5–79
SN75LVDS391D	4	100	15	5–63
SN75LVDS391PW	4	100	15	5–63
SN65LVDS389DBT	8	100	15	5–63
SN75LVDS389DBT	8	100	15	5–63
SN65LVDS387DGG	16	100	15	5–63
SN75LVDS387DGG	16	100	15	5–63

Repeaters

A repeater amplifies or regenerates the signal in order to extend the distance or duplicate it to multiple transmission lines. Long distance transmission uses repeaters extensively. They are also used to bridge between two circuits using different signaling levels. All of the repeaters listed in Table 4–7 operate from a 3.3-V supply.

Table 4–7. Repeaters

MATERIAL	INPUTS: OUTPUTS	V_{IT} (mV)	V_{ICR} (mV)	R_T (Ω)	OPEN-CIRCUIT FAILSAFE?	SIGNALING RATE (Mbps)	OUTPUT	BUS-PIN ESD (kV)	PAGE
SN65LVDS100D	1:1	50	4	No	No	2000	644	8	5–35
SN65LVDS100DGK	1:1	50	4	No	No	2000	644	8	5–35
SN65LVDS101D	1:1	50	4	No	No	2000	LVPECL	8	5–35
SN65LVDS101DGK	1:1	50	4	No	No	2000	LVPECL	8	5–35
SN65LVDT100D	1:1	50	4	110	No	2000	644	8	5–35
SN65LVDT100DGK	1:1	50	4	110	No	2000	644	8	5–35
SN65LVDT101D	1:1	50	4	110	No	2000	LVPECL	8	5–35
SN65LVDT101DGK	1:1	50	4	110	No	2000	LVPECL	8	5–35
SN65LVDS116DGG	1:16	100	2.4	No	Yes	400	644	12	5–43
SN65LVDS104D	1:4	100	2.4	No	Yes	400	644	16	5–37
SN65LVDS104PW	1:4	100	2.4	No	Yes	400	644	16	5–37
SN65LVDS105D	1:4	LVTTL	N/A	No	Yes	400	644	16	5–37
SN65LVDS105PW	1:4	LVTTL	N/A	No	Yes	400	644	16	5–37
SN65LVDS109DBT	Dual 1:4	100	2.4	No	Yes	400	644	12	5–41
SN65LVDS108DBT	1:8	100	2.4	No	Yes	400	644	12	5–39
SN65LVDS117DGG	Dual 1:8	100	2.4	No	Yes	400	644	12	5–41

Cross Reference

COMPETITOR NAME	COMPETITOR PART NUMBER	TI GENERIC PART NUMBER	REPLACEMENT CODE†	PAGE
Fairchild Semiconductor	FIN1017	SN65LVDS1	P	5–3
Fairchild Semiconductor	FIN1018	SN65LVDS2	P	5–3
Fairchild Semiconductor	FIN1018	SN65LVDT2	P	5–3
Fairchild Semiconductor	FIN1022	SN65LVDM22	P	5–7
Fairchild Semiconductor	FIN1022	SN65LVDS22	P	5–7
Fairchild Semiconductor	FIN1027	SN65LVDS9638	P	5–9
Fairchild Semiconductor	FIN1028	SN65LVDS9637	P	5–13
Fairchild Semiconductor	FIN1031	SN65LVDS31	Q	5–9
Fairchild Semiconductor	FIN1032	SN65LVDS32	Q	5–13
Maxim	MAX9110	SN65LVDS1	P	5–3
Maxim	MAX9111	SN65LVDS2	P	5–3
Maxim	MAX9111	SN65LVDT2	P	5–3
Maxim	MAX9112	SN65LVDS9638	P	5–9
Maxim	MAX9152	SN65LVDM22	P	5–7
Maxim	MAX9152	SN65LVDS22	P	5–7
National Semiconductor (NSC)	DS90CP22	SN65LVDM22	P	5–7
National Semiconductor (NSC)	DS90CP22	SN65LVDS22	P	5–7
National Semiconductor (NSC)	DS90LV010	SN65LVDM176	P	5–53
National Semiconductor (NSC)	DS90LV011A	SN65LVDS1	Q	5–3
National Semiconductor (NSC)	DS90LV017	SN65LVDS1	P	5–3

COMPETITOR NAME	COMPETITOR PART NUMBER	TI GENERIC PART NUMBER	REPLACEMENT CODE†	PAGE
National Semiconductor (NSC)	DS90LV017A	SN65LVDS1	P	5–3
National Semiconductor (NSC)	DS90LV018A	SN65LVDT2	P	5–3
National Semiconductor (NSC)	DS90LV019	SN65LVDS180	P	5–23
National Semiconductor (NSC)	DS90LV027	SN65LVDS9638	P	5–9
National Semiconductor (NSC)	DS90LV027A	SN65LVDS9638	P	5–9
National Semiconductor (NSC)	DS90LV028A	SN65LVDS9637	P	5–13
National Semiconductor (NSC)	DS90LV031	SN65LVDM31	Q	5–11
National Semiconductor (NSC)	DS90LV031	SN65LVDS31	S	5–11
National Semiconductor (NSC)	DS90LV031A	SN65LVDM31	Q	5–11
National Semiconductor (NSC)	DS90LV031A	SN65LVDS31	S	5–11
National Semiconductor (NSC)	DS90LV031B	SN65LVDM31	Q	5–11
National Semiconductor (NSC)	DS90LV031B	SN65LVDS31	Q	5–11
National Semiconductor (NSC)	DS90LV032	SN65LVDS32	S	5–13
National Semiconductor (NSC)	DS90LV032A	SN65LVDS32	S	5–13
National Semiconductor (NSC)	DS90LV047	SN65LVDS047	S	5–19
National Semiconductor (NSC)	DS90LV047A	SN65LVDS047	S	5–19
National Semiconductor (NSC)	DS90LV048	SN65LVDS048A	S	5–21
National Semiconductor (NSC)	DS90LV048A	SN65LVDS048A	S	5–21
National Semiconductor (NSC)	DS92LV010	SN65LVDM176	P	5–53
National Semiconductor (NSC)	DS92LV010A	SN65LVDM176	P	5–53
National Semiconductor (NSC)	DS92LV090	SN75LVDM976	P	5–65
National Semiconductor (NSC)	DS92LV090	SN75LVDM977	P	5–65
National Semiconductor (NSC)	DS92LV090A	SN75LVDM976	P	5–65
National Semiconductor (NSC)	DS92LV090A	SN75LVDM977	P	5–65
National Semiconductor (NSC)	DS92LV1021	SN65LVDS1021	Q	5–67
National Semiconductor (NSC)	DS92LV1023	SN65LVDS1023	Q	5–69
National Semiconductor (NSC)	DS92LV1212	SN65LVDS1212	Q	5–67
National Semiconductor (NSC)	DS92LV1224	SN65LVDS1224	Q	5–69
National Semiconductor (NSC)	DS92LV222	SN65LVDM22	P	5–7
National Semiconductor (NSC)	DS92LV222	SN65LVDS22	P	5–7
National Semiconductor (NSC)	DS92LV222A	SN65LVDM22	P	5–7
National Semiconductor (NSC)	DS92LV222A	SN65LVDS22	P	5–7
Pericom Semiconductor	PI90LV017A	SN65LVDS1	P	5–3
Pericom Semiconductor	PI90LV018A	SN65LVDS2	P	5–3
Pericom Semiconductor	PI90LV018A	SN65LVDT2	P	5–3
Pericom Semiconductor	PI90LV022	SN65LVDS22	P	5–7
Pericom Semiconductor	PI90LV027A	SN65LVDS9638	P	5–9
Pericom Semiconductor	PI90LV028A	SN65LVDS9637	P	5–13
Pericom Semiconductor	PI90LV031A	SN65LVDS31	Q	5–9
Pericom Semiconductor	PI90LV032A	SN65LVDS32	Q	5–13
Pericom Semiconductor	PI90LVB022	SN65LVDM22	P	5–7

† F: The TI device has similar functionality but is not fully equivalent to the competitor's device.
P: The TI device has the same functionality as the competitor's device, but is not pin-for-pin equivalent and may not be parametrically equivalent.
Q: The TI device has the same functionality and pinout as the competitor's device, but is not an exact equivalent.
S: The functionality and parameters of this TI device are exact equivalents of the competitor's device.

Chapter 5
Product Specifications

General Information

This section contains the first two pages of data sheets to give the reader an overview of the product's features and function. The reader should obtain the most recent version of the data sheet from www.ti.com or by contacting their local sales representative before making product selection or design decisions.

The product status statement on a data sheet is based on JEDEC Publication 103, JEDEC Suggested Data Sheet Classifications, and disclaimers, which defines the following:

- The term *Product Preview* applies to products in the formative or design stage. Specifications may or may not be backed by engineering data.
- The term *Advance Information* applies to products in the sampling, preproduction, or first-production stages.
- The term *Production Data* applies, by TI convention, beyond product preview and advance information.

  PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

  ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

  PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

  For information prior to production, a side banner appears on each page indicating Product Preview or Advance Information.

  If electrical characteristics for devices in different statuses occur elsewhere in the data sheet, TI selects the statement that reflects the status of the most developed product and places one of the following on page 1.

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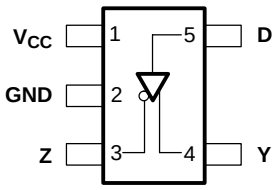
  UNLESS OTHERWISE NOTED this document contains ADVANCE INFORMATION on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

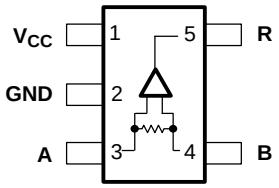
Table 5–1. Alphanumeric Listing

- **Meets or Exceeds the ANSI TIA/EIA-644A Standard**
- **Designed for Signaling Rates† up to:**
  - **630 Mbps Drivers**
  - **400 Mbps Receivers**
- **Operates From a 2.4-V to 3.6-V Supply**
- **Available in SOT–23 and SOIC Packages**
- **Bus-Terminal ESD Exceeds 15 kV**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV Into a 100-Ω Load**
- **Propagation Delay Times**
  - **1.7 ns Typical Driver**
  - **2.5 ns Typical Receiver**
- **Power Dissipation at 200 MHz**
  - **25 mW Typical Driver**
  - **60 mW Typical Receiver**
- **LVDT Receiver Includes Line Termination**
- **Low Voltage TTL (LVTTL) Level Driver Input Is 5-V Tolerant**
- **Driver Is Output High Impedance With V_{CC} < 1.5 V**
- **Receiver Output and Inputs Are High Impedance With V_{CC} < 1.5 V**
- **Receiver Open-Circuit Fail Safe**
- **Differential Input Voltage Threshold Less Than 100 mV**

SN65LVDS1
DBV Package
(TOP VIEW)

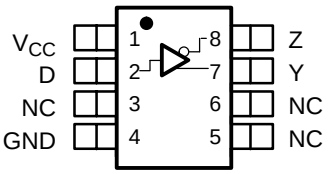


SN65LVDS2 and SN65LVDT2
DBV Package
(TOP VIEW)

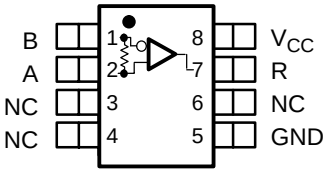


110-Ω Resistor for LVDT Only

SN65LVDS1
D Package
(TOP VIEW)



SN65LVDS2 and SN65LVDT2
D Package
(TOP VIEW)



110-Ω Resistor for LVDT Only

AVAILABLE OPTIONS

PART NUMBER	INTEGRATED TERMINATION	PACKAGE	PACKAGE MARKING
SN65LVDS1DBV		SOT23-5	SAAI
SN65LVDS1D		SOIC-8	LVDS1
SN65LVDS2DBV		SOT23-5	SABI
SN65LVDS2D		SOIC-8	LVDS2
SN65LVDT2DBV	√	SOT23-5	SACI
SN65LVDT2D	√	SOIC-8	LVDT2

description

The SN65LVDS1, SN65LVDS2, and SN65LVDT2 are single, low-voltage, differential line drivers and receivers in the small-outline transistor package. The outputs comply with the TIA/EIA-644A standard and provide a minimum differential output voltage magnitude of 247 mV into a 100-Ω load at signaling rates up to 630 Mbps for drivers and 400 Mbps for receivers.

When the SN65LVDS1 is used with an LVDS receiver (such as the SN65LVDT2) in a point-to-point connection, data or clocking signals can be transmitted over printed-circuit-board traces or cables at very high rates with very low electromagnetic emissions and power consumption. The packaging, low power, low EMI, high ESD tolerance, and wide supply voltage range make the device ideal for battery-powered applications.

The SN65LVDS1, SN65LVDS2, and SN65LVDT2 are characterized for operation from –40°C to 85°C.

†The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second)

Function Tables

DRIVER

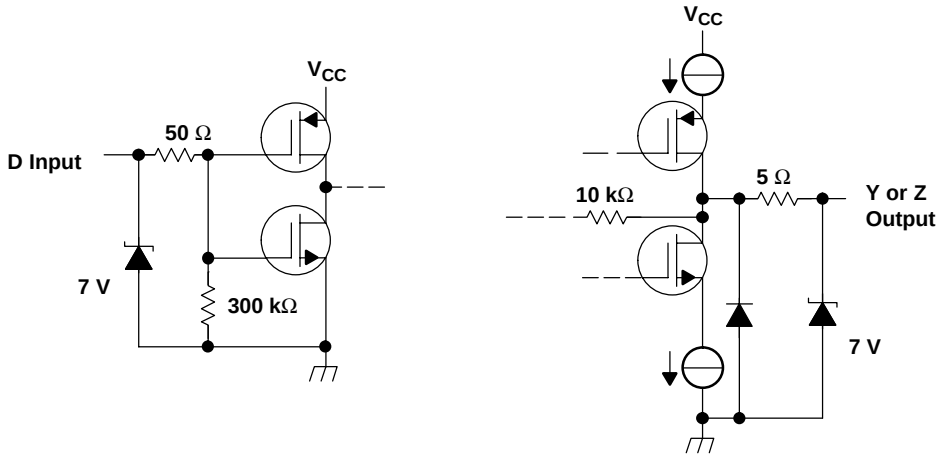
INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H
Open	L	H

RECEIVER

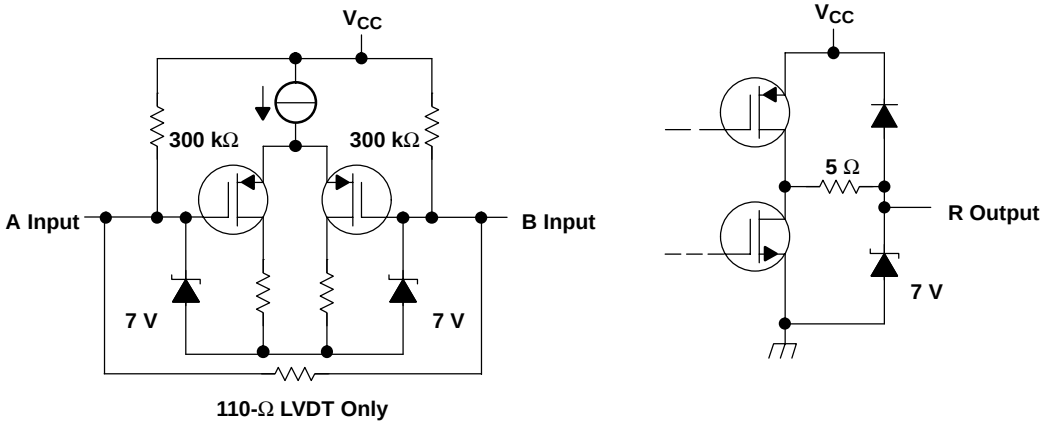
INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

H = high level, L = low level , ? = indeterminate

driver equivalent input and output schematic diagrams



receiver equivalent input and output schematic diagrams



MEMORY STICK™ INTERCONNECT EXTENDER CHIPSET WITH LVDS
SN65LVDT14—ONE DRIVER PLUS FOUR RECEIVERS
SN65LVDT41—FOUR DRIVERS PLUS ONE RECEIVER

FEATURES

- Integrated 110-Ω Nominal Receiver Line Termination Resistor
- Operates From a Single 3.3-V Supply
- Greater Than 125 Mbps Data Rate
- Flow-Through Pin-Out
- LVTTL Compatible Logic I/Os
- ESD Protection On Bus Pins Exceeds 16 kV
- Meets or Exceeds the Requirements of ANSI/TIA/EIA-644A Standard for LVDS
- 20-Pin PW Thin Shrink Small-Outline Package With 26-Mil Terminal Pitch

APPLICATIONS

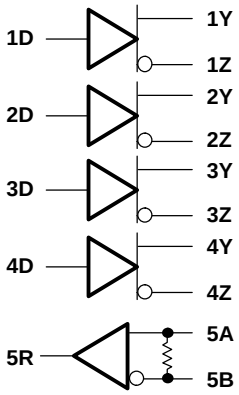
- Memory Stick Interface Extensions With Long Interconnects Between Host and Memory Stick™
- Serial Peripheral Interface™ (SPI) Interface Extension to Allow Long Interconnects Between Master and Slave
- MultiMediaCard™ Interface in SPI Mode
- General-Purpose Asymmetric Bidirectional Communication

DESCRIPTION

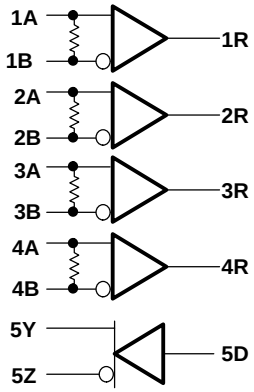
The SN65LVDT14 combines one LVDS line driver with four terminated LVDS line receivers in one package. It is designed to be used at the Memory Stick™ end of an LVDS based Memory Stick™ interface extension.

The SN65LVDT41 combines four LVDS line drivers with a single terminated LVDS line receiver in one package. It is designed to be used at the host end of an LVDS based Memory Stick™ interface extension.

SN65LVDT41 LOGIC DIAGRAM (POSITIVE LOGIC)



SN65LVDT14 LOGIC DIAGRAM (POSITIVE LOGIC)



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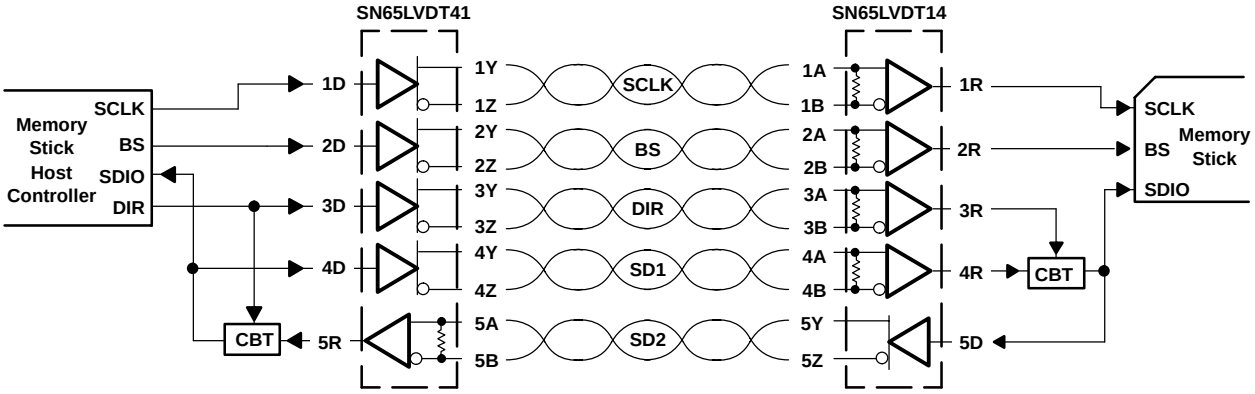
Memory Stick is a trademark of Sony.
Serial Peripheral Interface and SPI are trademarks of Motorola.
MultiMediaCard is a trademark of the MultiMediaCard Association.

TYPICAL MEMORY STICK INTERFACE EXTENSION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		SN65LVDT14, SN65LVDT41	UNIT
Supply voltage range(2)	V_{CC}	–0.5 to 4	V
Input voltage range	D or R	–0.5 to 6	V
	A, B, Y, or Z	–0.5 to 4	V
Electrostatic discharge	Human body model(3), A, B, Y, Z, and GND	±16	KV
	Human body model(3), all pins	±8	KV
	Charged device model(4), all pins	±500	V
Continuous total power dissipation		See Dissipation Rating Table	
Storage temperature range		–65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114–A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

PACKAGE DISSIPATION RATINGS

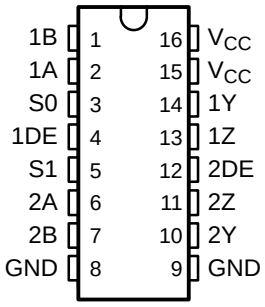
PACKAGE	T_A <25°C POWER RATING	OPERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
PW	774 mW	6.2 mW/°C	402 mW

RECOMMENDED OPERATING CONDITIONS

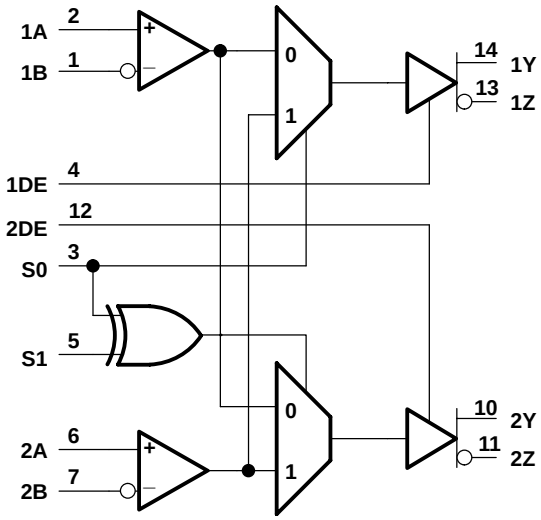
	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$	0.1		0.6	V
Common-mode input voltage, V_{IC} (See Figure 1)	$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
			$V_{CC} - 0.8$	V
Operating free-air temperature, T_A	–40		85	°C

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard**
- **Designed for Clock Rates up to 200 MHz (400 Mbps)**
- **Designed for Data Rates up to 250 Mbps**
- **Pin Compatible With SN65LVDS122 and SN65LVDT122, 1.5 Gbps 2x2 Crosspoint Switch From TI**
- **ESD Protection Exceeds 12 kV on Bus Pins**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Output Voltages of 350 mV Into:**
  - **100-Ω Load (SN65LVDS22)**
  - **50-Ω Load (SN65LVDM22)**
- **Propagation Delay Time; 4 ns Typ**
- **Power Dissipation at 400 Mbps of 150 mW**
- **Bus Pins Are High Impedance When Disabled or With V_{CC} Less Than 1.5 V**
- **LVTTL Levels Are 5 V Tolerant**
- **Open-Circuit Fail Safe Receiver**

SN65LVDS22D and SN65LVDS22PW (Marked as LVDS22)
SN65LVDM22D and SN65LVDM22PW (Marked as LVDM22)
(TOP VIEW)



logic diagram (positive logic)



description

The SN65LVDS22 and SN65LVDM22 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The receiver outputs can be switched to either or both drivers through the multiplexer control signals S0 and S1. This allows the flexibility to perform splitter or signal routing functions with a single device.

The TIA/EIA-644 standard compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 100 mV signals with up to 1 V of ground potential difference between a transmitter and receiver. The SN65LVDM22 doubles the output drive current to achieve LVDS levels with a 50-Ω load.

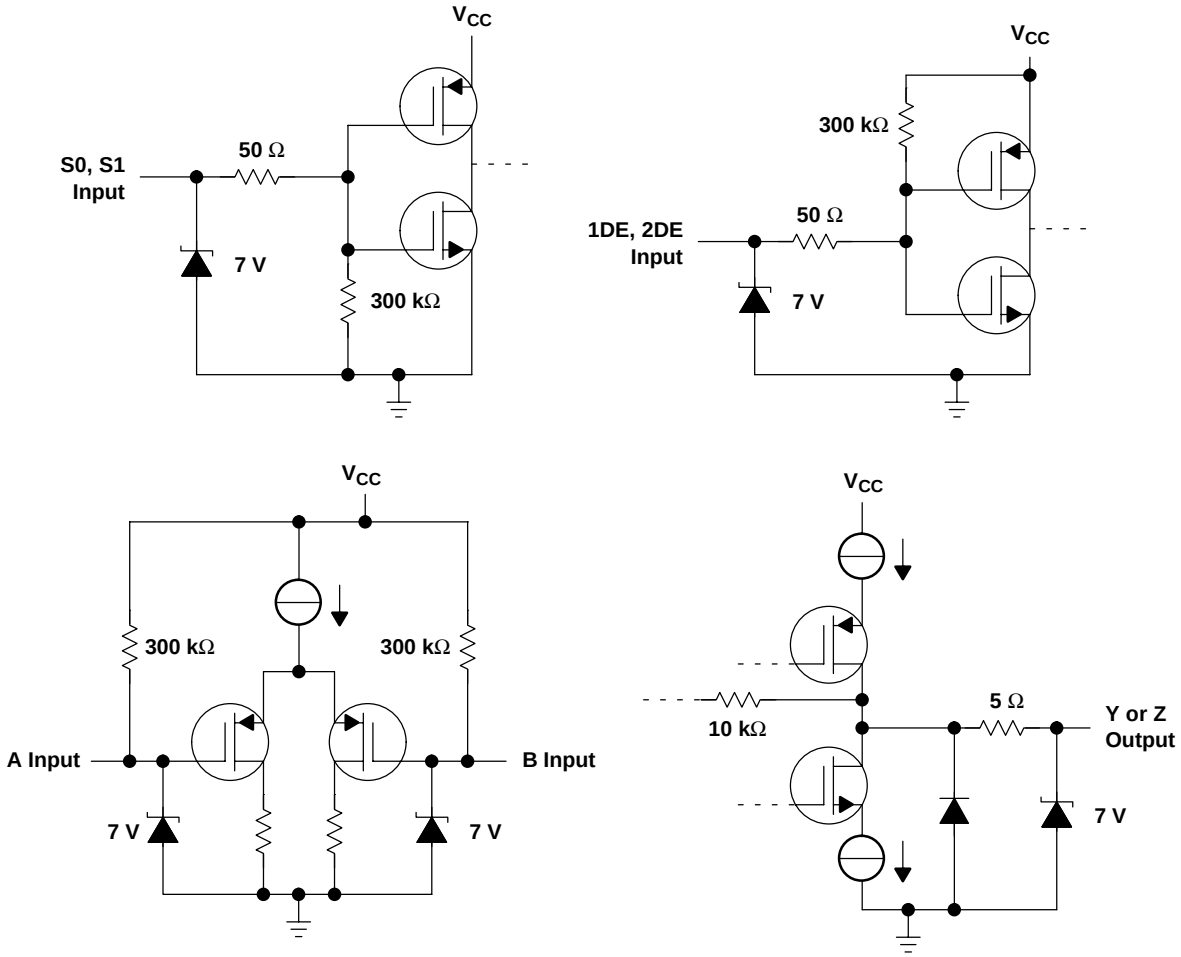
MUX TRUTH TABLE

INPUT		OUTPUT		FUNCTION
S1	S0	1Y/1Z	2Y/2Z	
0	0	1A/1B	1A/1B	Splitter
0	1	2A/2B	2A/2B	Splitter
1	0	1A/1B	2A/2B	Router
1	1	2A/2B	1A/1B	Router

The intended application of these devices and signaling technique is for both point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The SN65LVDS22 and SN65LVDM22 are characterized for operation from –40°C to 85°C.

equivalent input and output schematic diagrams



- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Typical Output Voltage Rise and Fall Times of 500 ps (400 Mbps)**
- **Typical Propagation Delay Times of 1.7 ns**
- **Operates From a Single 3.3-V Supply**
- **Power Dissipation 25 mW Typical per Driver at 200 MHz**
- **Driver at High Impedance When Disabled or With V_{CC} = 0**
- **Bus-Terminal ESD Protection Exceeds 8 kV**
- **Low-Voltage TTL (LVTTL) Logic Input Levels**
- **Pin-Compatible With the AM26LS31, MC3487, and μA9638**

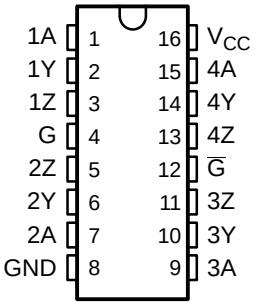
description

The SN55LVDS31, SN65LVDS31, SN65LVDS3487, and SN65LVDS9638 are differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5 V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

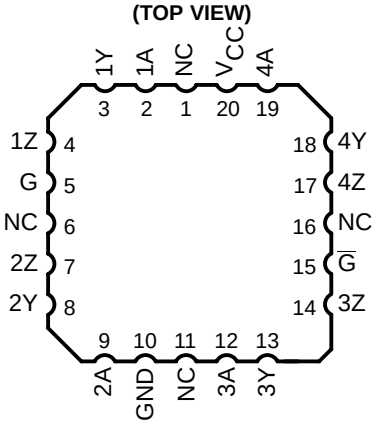
The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS31, SN65LVDS3487, and SN65LVDS9638 are characterized for operation from –40°C to 85°C. The SN55LVDS31 is characterized for operation from –55°C to 125°C.

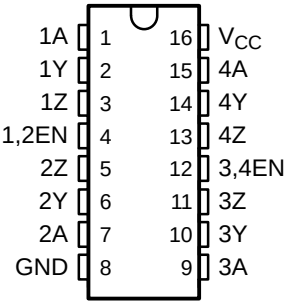
SN55LVDS31 . . . J OR W
SN65LVDS31 . . . D OR PW
(Marked as **LVDS31** or **65LVDS31**)
(TOP VIEW)



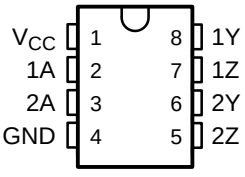
SN55LVDS31FK
(TOP VIEW)



SN65LVDS3487D
(Marked as **LVDS3487** or **65LVDS3487**)
(TOP VIEW)



SN65LVDS9638D (Marked as **DK638** or **LVDS38**)
SN65LVDS9638DGN (Marked as **L38**)
SN65LVDS9638DGK (Marked as **AXG**)
(TOP VIEW)



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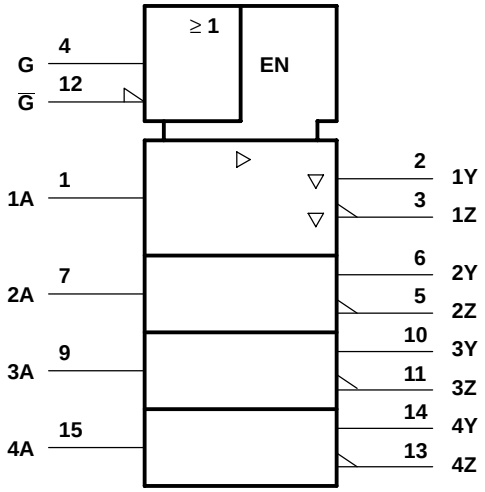
AVAILABLE OPTIONS

T_A	PACKAGE					
	SMALL OUTLINE		MSOP	CHIP CARRIER (FK)	CERAMIC DIP (J)	FLAT PACK (W)
	(D)	(PW)				
–40°C to 85°C	SN65LVDS31D	SN65LVDS31PW	—	—	—	—
	SN65LVDS3487D	—	—	—	—	—
	SN65LVDS9638D	—	SN65LVDS9638DGN	—	—	—
	—	—	SN65LVDS9638DGK	—	—	—
–55°C to 125°C	—	—	—	SN55LVDS31FK	SN55LVDS31J	SN55LVDS31W

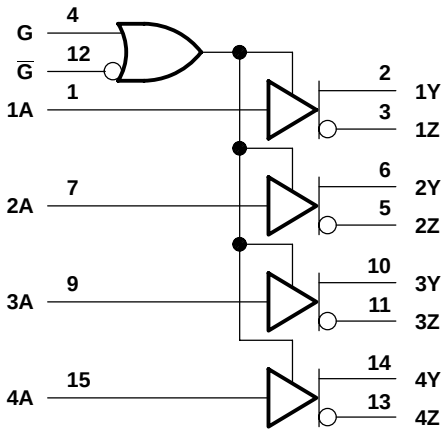
logic symbol†

SN55LVDS31, SN65LVDS31



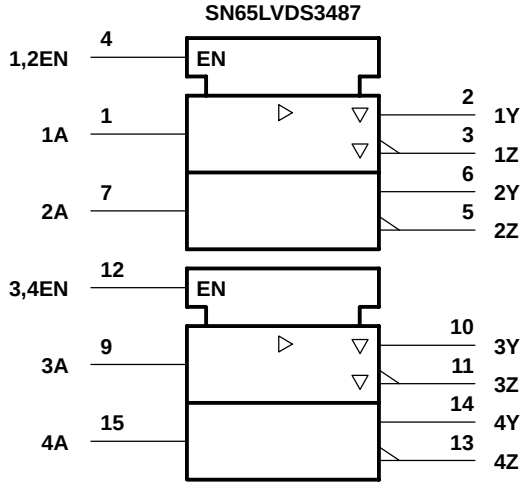
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'LVDS31 logic diagram (positive logic)



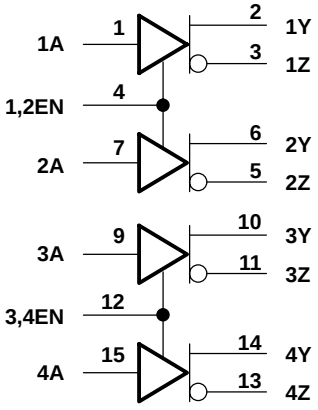
logic symbol†

SN65LVDS3487



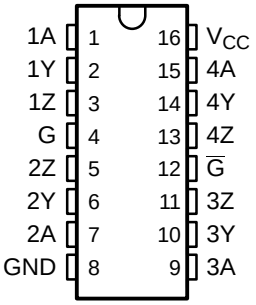
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'LVDS3487 logic diagram (positive logic)

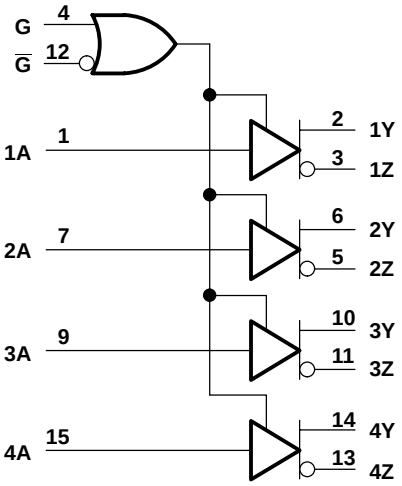


- **Designed for Signaling Rates† Up to 150 Mbps**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 700 mV and a 100-Ω Load**
- **Propagation Delay Time of 2.3 ns, Typical**
- **Single 3.3-V Supply Operation**
- **One Driver's Power Dissipation at 75 MHz, 50 mW, Typical**
- **High-Impedance Outputs When Disabled or With V_{CC} < 1.5 V**
- **Bus-Pin ESD Protection Exceeds 12 kV**
- **Low-Voltage CMOS (LVCMOS) Logic Input Levels Are 5-V Tolerant**

SN65LVDM31D (Marked as LVDM31)
(TOP VIEW)



functional block diagram



description

The SN65LVDM31 incorporates four differential line drivers that implement the electrical characteristics of low-voltage differential signaling. This product offers a low-power alternative to 5-V PECL drivers with similar signal levels. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 540 mV into a 100-Ω load when enabled by either an active-low or active-high enable input.

The intended application of this device and signaling technique is for both point-to-point and multiplexed baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDM31 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

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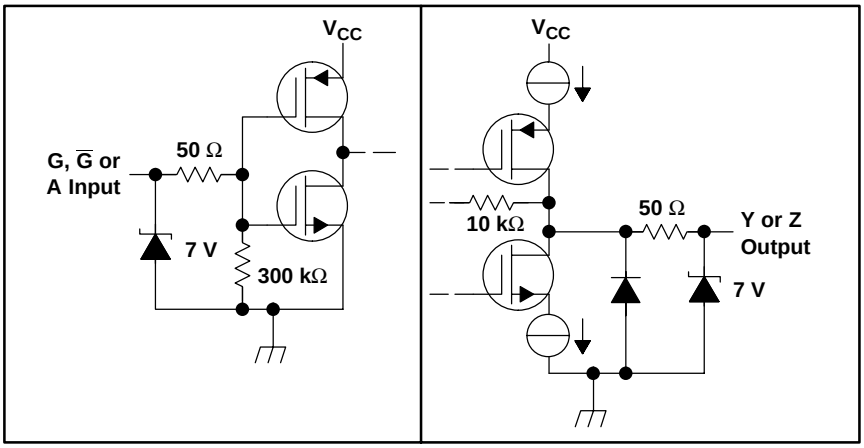
†The signaling rate is the number of voltage transitions that can be made per second.

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range (see Note 1) V_{CC} . . . . . –0.5 V to 4 V
Input voltage range, Inputs . . . . . –0.5 V to 6 V
Y or Z . . . . . –0.5 V to 4 V
Electrostatic discharge, (see Note 2): Y, Z, and GND . . . . . Class 3, A:12 kV, B:600 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2.0			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	–40		85	°C

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard**
- **Operates With a Single 3.3-V Supply**
- **Designed for Signaling Rate of up to 400 Mbps**
- **Differential Input Thresholds ±100 mV Max**
- **Typical Propagation Delay Time of 2.1 ns**
- **Power Dissipation 60 mW Typical per Receiver at 200 MHz**
- **Bus-Terminal ESD Protection Exceeds 8 kV**
- **Low-Voltage TTL (LVTTL) Logic Output Levels**
- **Pin-Compatible With the AM26LS32, MC3486, and μA9637**
- **Open-Circuit Fail Safe**

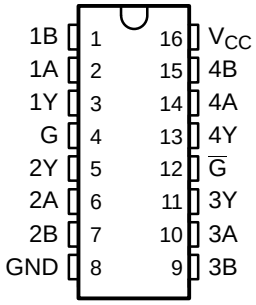
description

The SN55LVDS32, SN65LVDS32, SN65LVDS3486, and SN65LVDS9637 are differential line receivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four differential receivers provides a valid logical output state with a ±100 mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

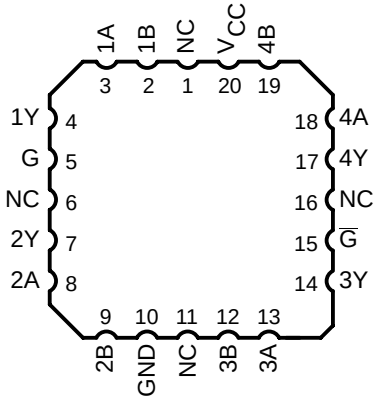
The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS32, SN65LVDS3486, and SN65LVDS9637 are characterized for operation from –40°C to 85°C. The SN55LVDS32 is characterized for operation from –55°C to 125°C.

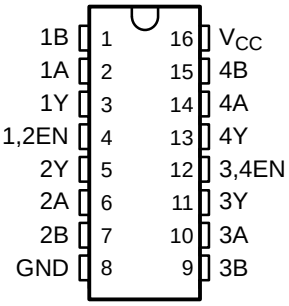
SN55LVDS32 . . . J OR W
SN65LVDS32 . . . D OR PW
(Marked as **LVDS32** or **65LVDS32**)
(TOP VIEW)



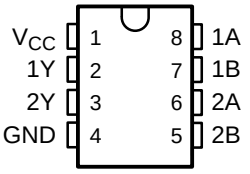
SN55LVDS32FK
(TOP VIEW)



SN65LVDS3486D (Marked as **LVDS3486**)
(TOP VIEW)



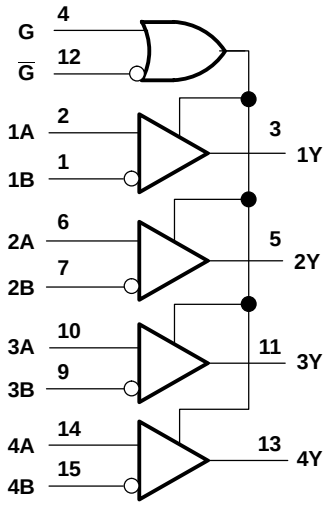
SN65LVDS9637D (Marked as **DK637** or **LVDS37**)
SN65LVDS9637DGN (Marked as **L37**)
SN65LVDS9637DGK (Marked as **AXF**)
(TOP VIEW)



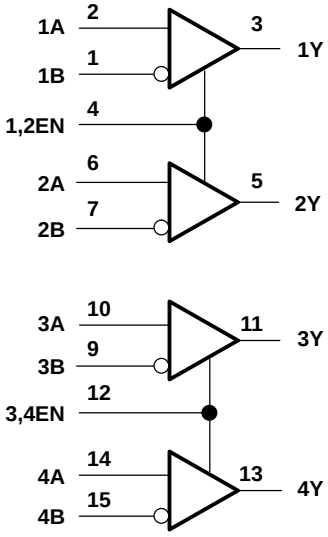
AVAILABLE OPTIONS

T_A	PACKAGE					
	SMALL OUTLINE		MSOP	CHIP CARRIER (FK)	CERAMIC DIP (J)	FLAT PACK (W)
	(D)	(PW)				
–40°C to 85°C	SN65LVDS32D	SN65LVDS32PW	—	—	—	—
	SN65LVDS3486D		—	—	—	—
	SN65LVDS9637D		SN65LVDS9637DGN	—	—	—
	—		SN65LVDS9637DGK	—	—	—
–55°C to 125°C	—	—	—	SN55LVDS32FK	SN55LVDS32J	SN55LVDS32W

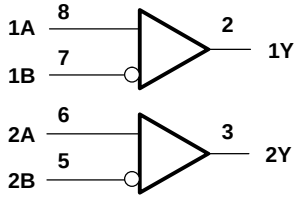
'LVDS32 logic diagram (positive logic)



'LVDS3486D logic diagram (positive logic)



'LVDS9637D logic diagram (positive logic)



- **Meets or Exceeds the Requirements of ANSI EIA/TIA-644 Standard for Signaling Rates† up to 400 Mbps**
- **Operates With a Single 3.3-V Supply**
- **–2-V to 4.4-V Common-Mode Input Voltage Range**
- **Differential Input Thresholds <50 mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range**
- **Integrated 110-Ω Line Termination Resistors Offered With the LVDT Series**
- **Propagation Delay Times 4 ns (typ)**
- **Active Fail Safe Assures a High-Level Output With No Input**
- **Bus-Pin ESD Protection Exceeds 15 kV HBM**
- **Inputs Remain High-Impedance on Power Down**
- **Recommended Maximum Parallel Rate of 200 M-Transfers/s**
- **Available in Small-Outline Package With 1,27 mm Terminal Pitch**
- **Pin-Compatible With the AM26LS32, MC3486, or μA9637**

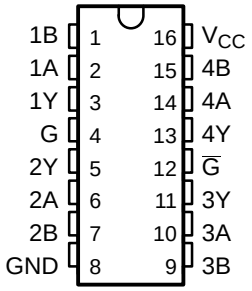
description

This family of differential line receivers offers improved performance and features that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS is defined in the TIA/EIA-644 standard. This improved performance represents the second generation of receiver products for this standard, providing a better overall solution for the cabled environment. This generation of products is an extension to TI's overall product portfolio and is not necessarily a replacement for older LVDS receivers.

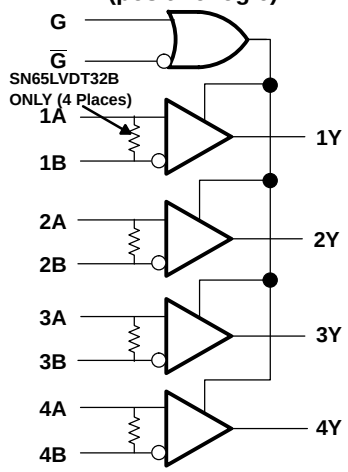
Improved features include an input common-mode voltage range 2 V wider than the minimum required by the standard. This will allow longer cable lengths by tripling the allowable ground noise tolerance to 3 V between a driver and receiver. TI has additionally introduced an even wider input common-mode voltage range of –4 to 5 V in their SN65LVDS/T33 and SN65LVDS/T34.

SN65LVDS32B
SN65LVDT32B

D PACKAGE
(TOP VIEW)

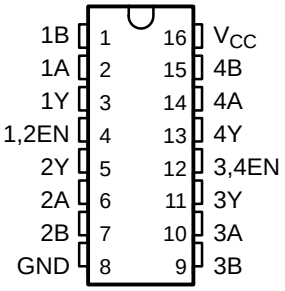


Logic Diagram
(positive logic)

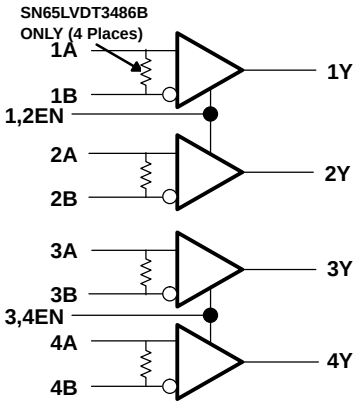


SN65LVDS3486B
SN65LVDT3486B

D PACKAGE
(TOP VIEW)

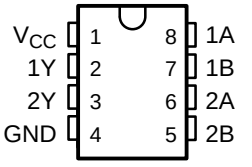


Logic Diagram
(positive logic)

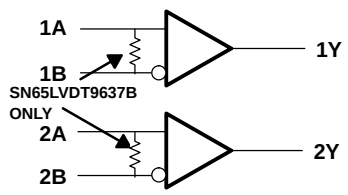


SN65LVDS9637B
SN65LVDT9637B

D PACKAGE
(TOP VIEW)



Logic Diagram
(positive logic)



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† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

description (continued)

Precise control of the differential input voltage thresholds now allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than ±50 mV over the full input common-mode voltage range.

The high-speed switching of LVDS signals almost always necessitates the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. The SN65LVDT series of receivers eliminates this external resistor by integrating it with the receiver. The nonterminated SN65LVDS series is also available for multidrop or other termination circuits.

The receivers can withstand ±15-kV human-body model (HBM) and ±600 V-machine model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) fail-safe circuit that will provide a high-level output within 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. This prevents noise from being received as valid data under these fault conditions. This feature may also be used for wired-OR bus signaling.

The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B, SN65LVDT3486B, SN65LVDS9637B, and SN65LVDT9637B are characterized for operation from -40°C to 85°C.

AVAILABLE OPTIONS

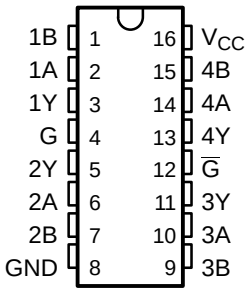
PART NUMBER†	NUMBER OF RECEIVERS	TERMINATION RESISTOR†	SYMBOLIZATION
SN65LVDS32BD	4	No	LVDS32B
SN65LVDT32BD	4	Yes	LVDT32B
SN65LVDS3486BD	4	No	LVDS3486
SN65LVDT3486BD	4	Yes	LVDT3486
SN65LVDS9637BD	2	No	DK637B
SN65LVDT9637BD	2	Yes	DR637B

† Add the suffix R for taped and reeled carrier.

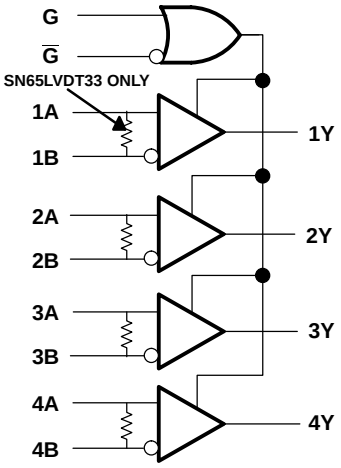
- **400-Mbps Signaling Rate[1] and 200-Mxfr/s Data Transfer Rate**
- **Operates With a Single 3.3-V Supply**
- **–4-V to 5-V Common-Mode Input Voltage Range**
- **Differential Input Thresholds <±50 mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range**
- **Integrated 110-Ω Line Termination Resistors On LVDT Products**
- **TSSOP Packaging (33 Only)**
- **Complies With TIA/EIA-644 (LVDS)**
- **Active Failsafe Assures a High-Level Output With No Input**
- **Bus-Pin ESD Protection Exceeds 15 kV HBM**
- **Input Remains High-Impedance on Power Down**
- **TTL Inputs Are 5-V Tolerant**
- **Pin-Compatible With the AM26LS32, SN65LVDS32B, μA9637, SN65LVDS9637B**

SN65LVDS33D
SN65LVDT33D
SN65LVDS33PW
SN65LVDT33PW

D OR PW PACKAGE
(TOP VIEW)

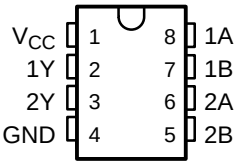


logic diagram (positive logic)

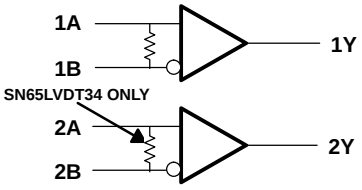


SN65LVDS34D
SN65LVDT34D

D PACKAGE
(TOP VIEW)



logic diagram (positive logic)



description

This family of four LVDS data line receivers offers the widest common-mode input voltage range in the industry. These receivers provide an input voltage range specification compatible with a 5-V PECL signal as well as an overall increased ground-noise tolerance. They are in industry standard footprints with integrated termination as an option.

Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than ±50 mV over the full input common-mode voltage range.

The high-speed switching of LVDS signals usually necessitates the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. The SN65LVDT series of receivers eliminates this external resistor by integrating it with the receiver. The nonterminated SN65LVDS series is also available for multidrop or other termination circuits.

AVAILABLE OPTIONS

PART NUMBER†	NUMBER OF RECEIVERS	TERMINATION RESISTOR	SYMBOLIZATION
SN65LVDS33D	4	No	LVDS33
SN65LVDS33PW	4	No	LVDS33
SN65LVDT33D	4	Yes	LVDT33
SN65LVDT33PW	4	Yes	LVDT33
SN65LVDS34D	2	No	LVDS34
SN65LVDT34D	2	Yes	LVDT34

† Add the suffix R for taped and reeled carrier.

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[1]The signalling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

description (continued)

The receivers can withstand ±15 kV human-body model (HBM) and ±600 V machine model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) failsafe circuit that will provide a high-level output within 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. The failsafe circuit prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling. See *The Active Failsafe Feature of the SN65LVDS32B* application note.

The intended application and signaling technique of these devices is point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS33, SN65LVDT33, SN65LVDS34 and SN65LVDT34 are characterized for operation from –40°C to 85°C.

Function Tables

SN65LVDS33 and SN65LVDT33

DIFFERENTIAL INPUT	ENABLES		OUTPUT
$V_{ID} = V_A - V_B$	G	$\overline{G}$	Y
$V_{ID} \geq$ -32 mV	H	X	H
	X	L	H
–100 mV < $V_{ID} \leq$ –32 mV	H	X	?
	X	L	?
$V_{ID} \leq$ –100 mV	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

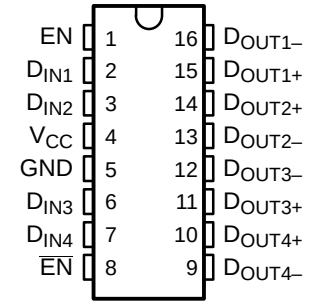
SN65LVDS34 and SN65LVDT34

DIFFERENTIAL INPUT	OUTPUT
$V_{ID} = V_A - V_B$	Y
$V_{ID} \geq$ -32 mV	H
–100 mV < $V_{ID} \leq$ –32 mV	?
$V_{ID} \leq$ -100 mV	L
Open	H

H = high level, L = low level,
? = indeterminate

- **>400 Mbps (200 MHz) Signaling Rates**
- **Flow-Through Pinout Simplifies PCB Layout**
- **300 ps Maximum Differential Skew**
- **Propagation Delay Times 1.8 ns (Typical)**
- **3.3 V Power Supply Design**
- **±350 mV Differential Signaling**
- **High Impedance on LVDS Outputs on Power Down**
- **Conforms to TIA/EIA-644 LVDS Standard**
- **Industrial Operating Temperature Range (–40°C to 85°C)**
- **Available in SOIC and TSSOP Packages**

D OR PW PACKAGE
(Marked as LVDS047)
(TOP VIEW)



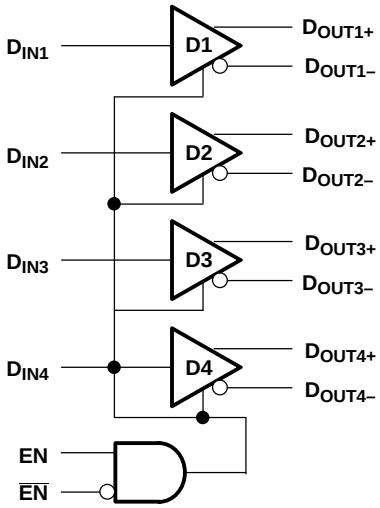
description

The SN65LVDS047 is a quad differential line driver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of this device and signaling technique is for point-to-point and multidrop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

The SN65LVDS047 is characterized for operation from –40°C to 85°C.

functional block diagram

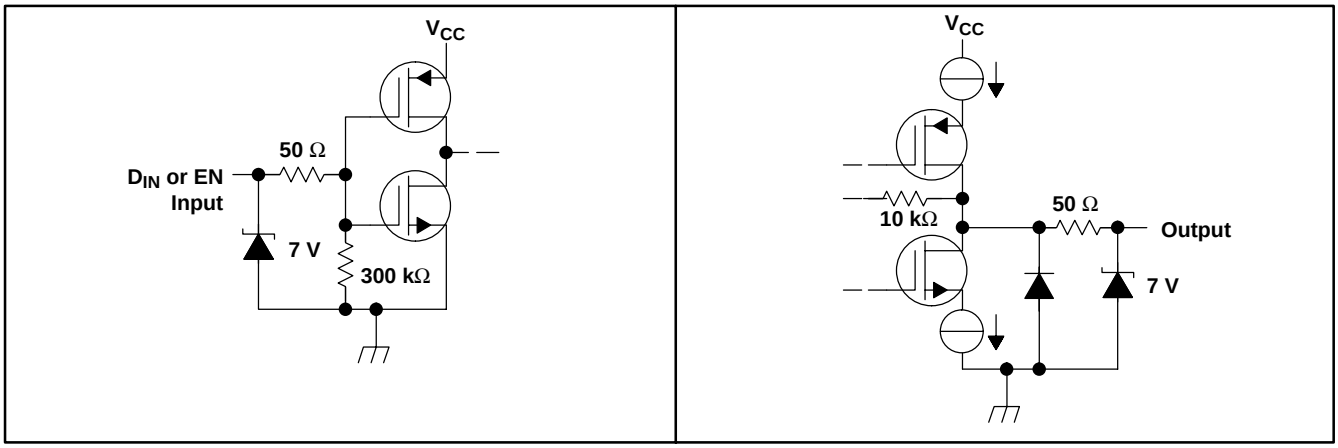


TRUTH TABLE

INPUT	ENABLES		OUTPUTS	
D_{IN}	EN	$\overline{EN}$	D_{OUT+}	D_{OUT-}
L	H	L or OPEN	L	H
H			H	L
X	All other conditions		Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (see Note 1) (unless otherwise noted)†

Supply voltage (V_{CC}) . . . . . –0.3 V to 4 V
Input voltage range, $V_I(D_{IN})$ . . . . . –0.3 V to (V_{CC} +0.3 V)
Enable input voltage (EN, $\overline{EN}$) . . . . . –0.3 V to (V_{CC} +0.3 V)
Output voltage, $V_O(D_{OUT+}, D_{OUT-})$ . . . . . –0.3 V to 3.9 V
Bus-pin (D_{OUT+},D_{OUT-}) electrostatic discharge, (see Note 2) . . . . . >10 kV
Short circuit duration (D_{OUT+},(D_{OUT-}) . . . . . Continuous
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

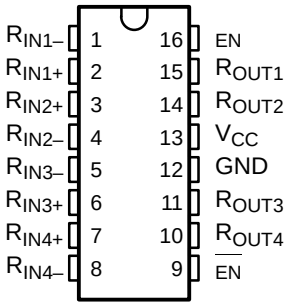
‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

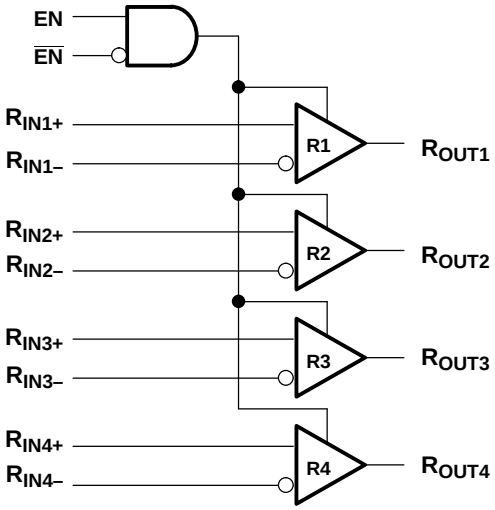
	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Operating free-air temperature, T_A	–40	25	85	°C

- **>400 Mbps (200 MHz) Signaling Rates**
- **Flow-Through Pinout Simplifies PCB Layout**
- **50 ps Channel-to-Channel Skew (Typ)**
- **200 ps Differential Skew (Typ)**
- **Propagation Delay Times 2.7 ns (Typ)**
- **3.3-V Power Supply Design**
- **High Impedance LVDS Inputs on Power Down**
- **Low-Power Dissipation (40 mW at 3.3 V Static)**
- **Accepts Small Swing (350 mV) Differential Signal Levels**
- **Supports Open, Short, and Terminated Input Fail-Safe**
- **Industrial Operating Temperature Range (–40°C to 85°C)**
- **Conforms to TIA/EIA-644 LVDS Standard**
- **Available in SOIC and TSSOP Packages**
- **Pin-Compatible With DS90LV048A From National**

SN65LVDS048AD (Marked as LVDS048A)
SN65LVDS048APW (Marked as DL048A)
(TOP VIEW)



functional diagram



description

The SN65LVDS048A is a quad differential line receiver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the quad differential receivers will provide a valid logical output state with a ±100-mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

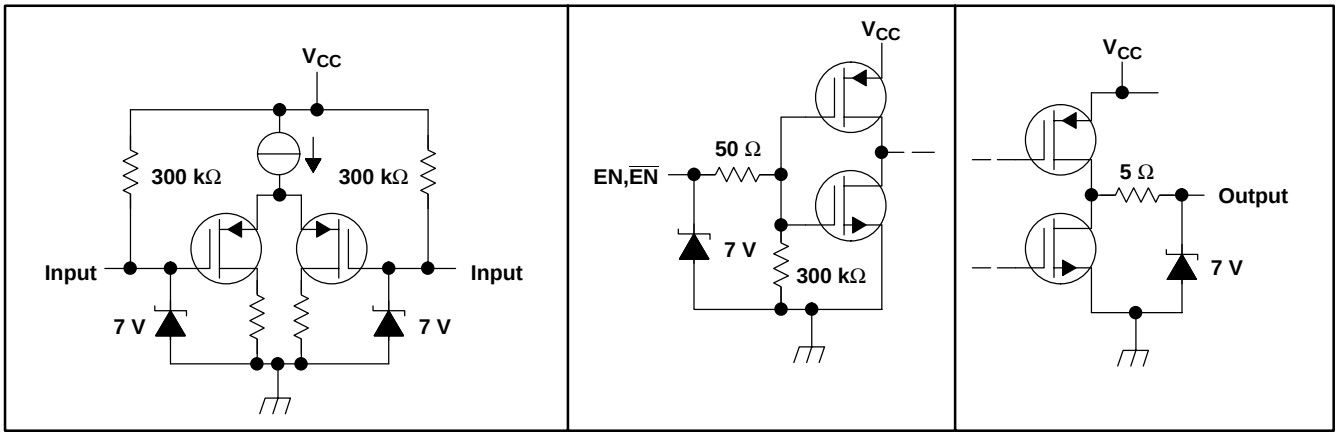
The SN65LVDS048A is characterized for operation from –40°C to 85°C.

TRUTH TABLE

DIFFERENTIAL INPUT	ENABLES		OUTPUT
$R_{IN+} - R_{IN-}$	EN	$\overline{EN}$	R_{OUT}
$V_{ID} \geq 100$ mV	H	L or OPEN	H
$V_{ID} \leq -100$ mV			L
Open/short or terminated			H
X	All other conditions		Z

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range (V_{CC}) . . . . . –0.3 V to 4 V
Input voltage range, V_I(R_{IN+}, R_{IN-}) . . . . . –0.3 V to 4 V
Enable input voltage (EN, $\overline{EN}$) . . . . . –0.3 V to (V_{CC} +0.3 V)
Output voltage, V_O(R_{OUT}) . . . . . –0.3 V to (V_{CC} +0.3 V)
Bus-pin (R_{IN+}, R_{IN-}) Electrostatic discharge (see Note 2) . . . . . > 10 kV
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

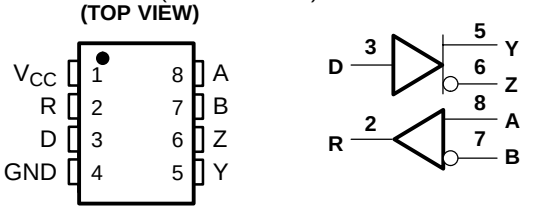
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

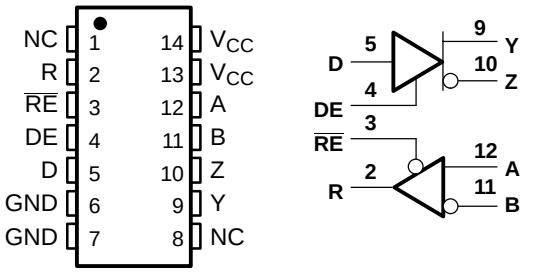
‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard**
- **Signaling Rates up to 400 Mbps**
- **Bus-Terminal ESD Exceeds 12 kV**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 100-Ω Load**
- **Propagation Delay Times**
  - **Driver: 1.7 ns Typ**
  - **Receiver: 3.7 ns Typ**
- **Power Dissipation at 200 MHz**
  - **Driver: 25 mW Typical**
  - **Receiver: 60 mW Typical**
- **LVTTL Input Levels Are 5-V Tolerant**
- **Driver is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Receiver Has Open-Circuit Fail Safe**

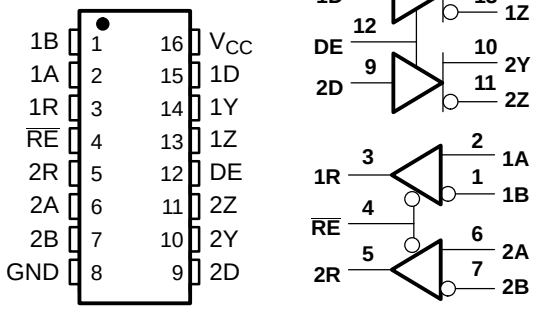
SN65LVDS179D (Marked as **DL179** or **LVD179**)
SN65LVDS179DGK (Marked as **S79**)
(TOP VIEW)



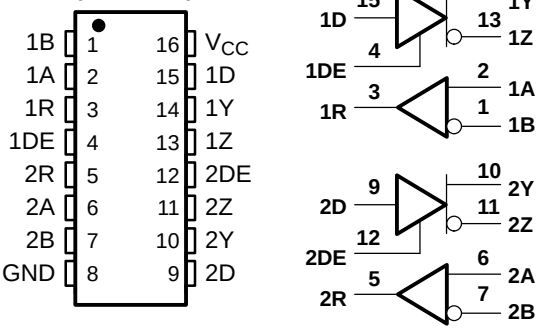
SN65LVDS180D (Marked as **LVDS180**)
SN65LVDS180PW (Marked as **LVDS180**)
(TOP VIEW)



SN65LVDS050D (Marked as **LVDS050**)
SN65LVDS050PW (Marked as **LVDS050**)
(TOP VIEW)



SN65LVDS051D (Marked as **LVDS051**)
SN65LVDS051PW (Marked as **LVDS051**)
(TOP VIEW)



description

The SN65LVDS179, SN65LVDS180, SN65LVDS050, and SN65LVDS051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The TIA/EIA-644 standard compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 50-mV signals with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The SN65LVDS179, SN65LVDS180, SN65LVDS050, and SN65LVDS051 are characterized for operation from –40°C to 85°C.

NOTE:

The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE (D)	SMALL OUTLINE (DGK)	SMALL OUTLINE (PW)
–40°C to 85°C	SN65LVDS050D	—	SN65LVDS050PW
	SN65LVDS051D	—	SN65LVDS051PW
	SN65LVDS179D	SN65LVDS179DGK	—
	SN65LVDS180D	—	SN65LVDS180PW

Function Tables

SN65LVDS179 RECEIVER

INPUTS	OUTPUT
$V_{ID} = V_A – V_B$	R
$V_{ID} \geq 50$ mV	H
$–50 \text{ mV} < V_{ID} < 50 \text{ mV}$	?
$V_{ID} \leq –50$ mV	L
Open	H

H = high level, L = low level, ? = indeterminate

SN65LVDS179 DRIVER

INPUT	OUTPUTS	
D	Y	Z
L	L	H
H	H	L
Open	L	H

H = high level, L = low level

SN65LVDS180, SN65LVDS050, and SN65LVDS051 RECEIVER

INPUTS		OUTPUT
$V_{ID} = V_A – V_B$	$\overline{RE}$	R
$V_{ID} \geq 50$ mV	L	H
$–50 \text{ mV} < V_{ID} < 50 \text{ mV}$	L	?
$V_{ID} \leq –50$ mV	L	L
Open	L	H
X	H	Z

H = high level, L = low level, Z = high impedance,
X = don't care

SN65LVDS180, SN65LVDS050, and SN65LVDS051 DRIVER

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

H = high level, L = low level, Z = high impedance,
X = don't care

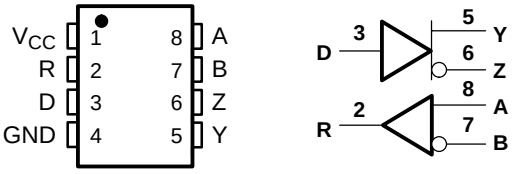
- **Low-Voltage Differential 50-Ω Line Drivers and Receivers**
- **Signaling Rates up to 500 Mbps**
- **Bus-Terminal ESD Exceeds 12 kV**
- **Operates From a Single 3.3 V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 340 mV With a 50-Ω Load**
- **Valid Output With as Little as 50-mV Input Voltage Difference**
- **Propagation Delay Times**
  - **Driver: 1.7 ns Typ**
  - **Receiver: 3.7 ns Typ**
- **Power Dissipation at 200 MHz**
  - **Driver: 50 mW Typical**
  - **Receiver: 60 mW Typical**
- **LVTTL Input Levels Are 5 V Tolerant**
- **Driver Is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Receiver Has Open-Circuit Fail Safe**

description

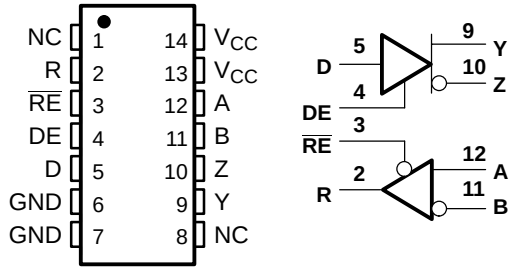
The SN65LVDM179, SN65LVDM180, SN65LVDM050, and SN65LVDM051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 500 Mbps (per TIA/EIA-644 definition). These circuits are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts, except that the output current of the drivers is doubled. This modification provides a minimum differential output voltage magnitude of 247 mV across a 50-Ω load simulating two transmission lines in parallel. This allows having data buses with more than one driver or with two line termination resistors. The receivers detect a voltage difference of 50 mV with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of these devices and signaling techniques is point-to-point and multipoint, baseband data transmission over a controlled impedance media of approximately 100 Ω of characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables.

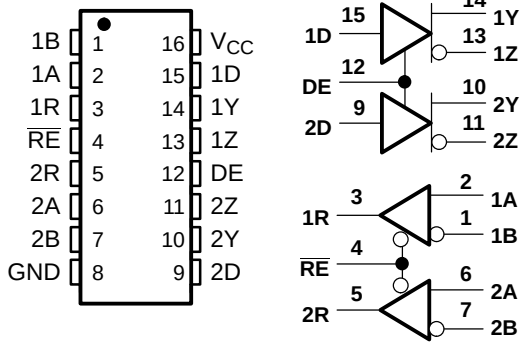
SN65LVDM179D (Marked as **DM179** or **LVM179)**
SN65LVDM179DGK (Marked as **M79**)
(TOP VIEW)



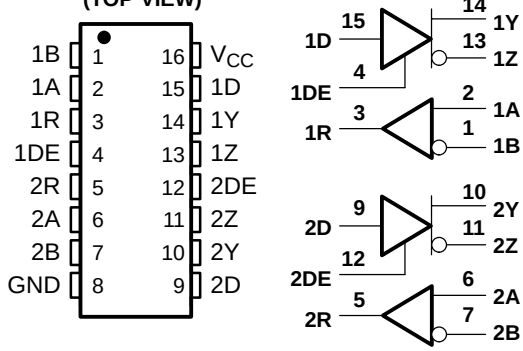
SN65LVDM180D (Marked as **LVDM180**)
SN65LVDM180PW (Marked as **LVDM180**)
(TOP VIEW)



SN65LVDM050D (Marked as **LVDM050**)
SN65LVDM050PW (Marked as **LVDM050**)
(TOP VIEW)



SN65LVDM051D (Marked as **LVDM051**)
SN65LVDM051PW (Marked as **LVDM051**)
(TOP VIEW)



The SN65LVDM179, SN65LVDM180, SN65LVDM050, and SN65LVDM051 are characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE (D)	SMALL OUTLINE (DGK)	SMALL OUTLINE (PW)
–40°C to 85°C	SN65LVDM050D	—	SN65LVDM050PW
	SN65LVDM051D	—	SN65LVDM051PW
	SN65LVDM179D	SN65LVDM179DGK	—
	SN65LVDM180D	—	SN65LVDM180PW

NOTE:

The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application-specific characteristics.

Function Tables

SN65LVDM179 RECEIVER

INPUTS	OUTPUT
$V_{ID} = V_A – V_B$	R
$V_{ID} \geq 50$ mV	H
–50 MV < V_{ID} < 50 mV	?
$V_{ID} \leq –50$ mV	L
Open	H

H = high level, L = low level, ? = indeterminate

SN65LVDM179 DRIVER

INPUT	OUTPUTS	
D	Y	Z
L	L	H
H	H	L
Open	L	H

H = high level, L = low level

SN65LVDM180, SN65LVDM050, and SN65LVDM051 RECEIVER

INPUTS		OUTPUT
$V_{ID} = V_A – V_B$	$\overline{RE}$	R
$V_{ID} \geq 50$ mV	L	H
–50 MV < V_{ID} < 50 mV	L	?
$V_{ID} \leq –50$ mV	L	L
Open	L	H
X	H	Z

H = high level, L = low level, Z = high impedance, X = don't care

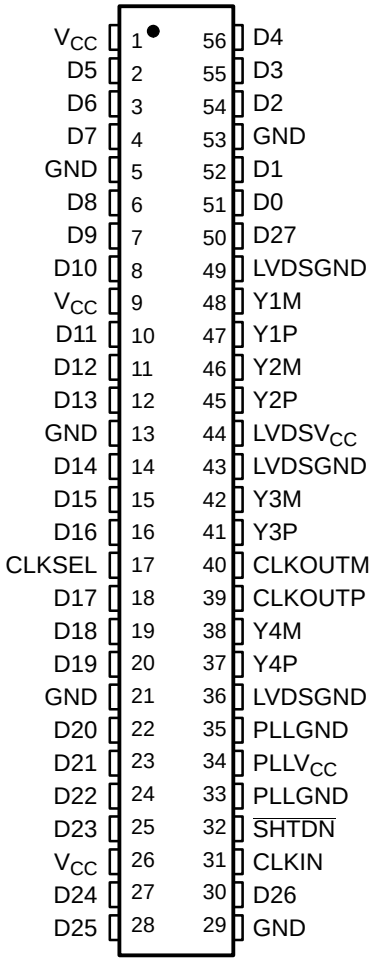
SN65LVDM180, SN65LVDM050, and SN65LVDM051 DRIVER

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

H = high level, L = low level, Z = high impedance, X = don't care

- **28:4 Data Channel Compression at up to 1.82 Gigabits per Second Throughput**
- **Suited for Point-to-Point Subsystem Communication With Very Low EMI**
- **28 Data Channels Plus Clock in Low-Voltage TTL and 4 Data Channels Plus Clock Out Low-Voltage Differential**
- **Selectable Rising or Falling Clock Edge Triggered Inputs**
- **Bus Pins Tolerate 6-kV HBM ESD**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant Data Inputs**
- **Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch**
- **Consumes <1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 20 MHz to 65 MHz**
- **No External Components Required for PLL**
- **Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Industrial Temperature Qualified T_A = –40°C to 85°C**
- **Replacement for the DS90CR285**

DGG PACKAGE
(TOP VIEW)



description

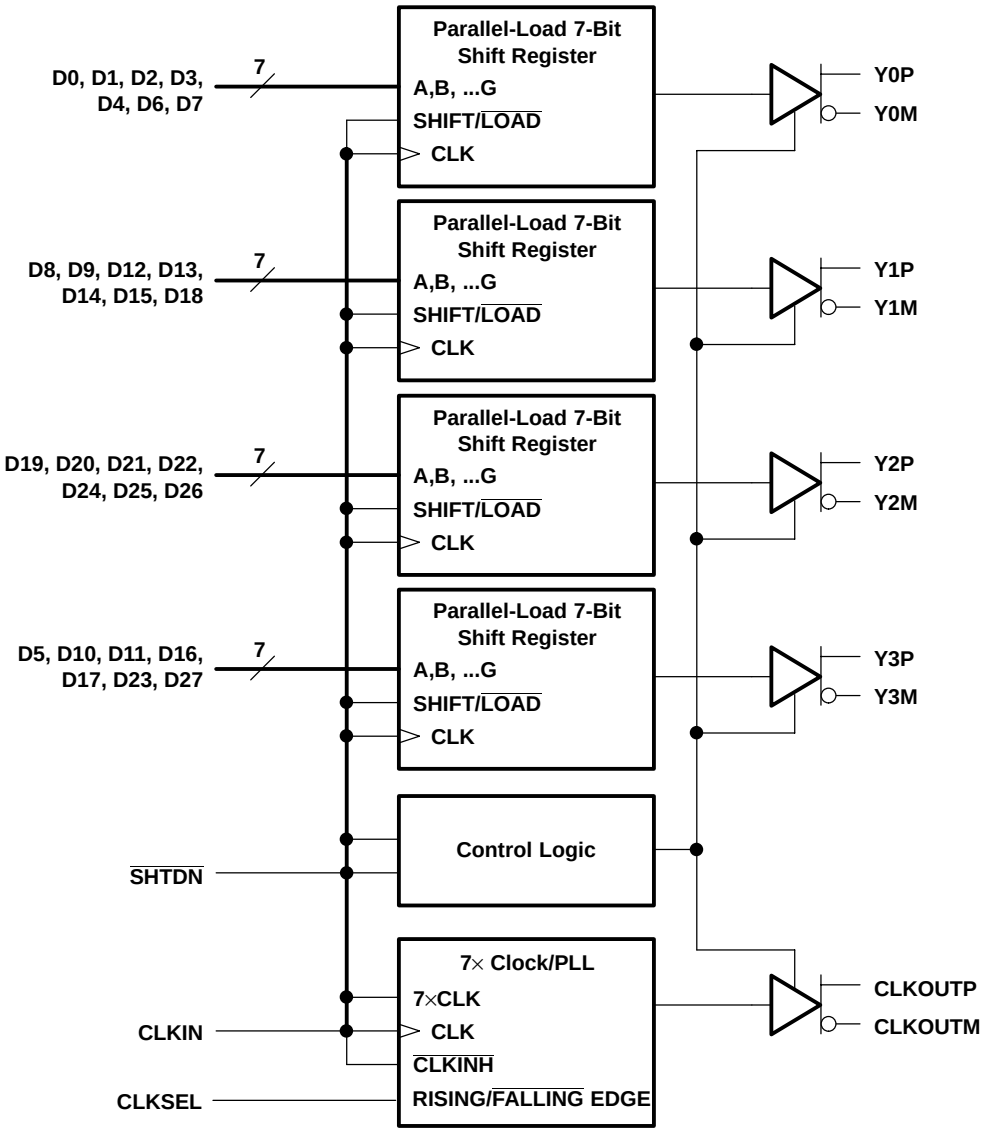
The SN65LVDS93 LVDS serdes (serializer/deserializer) transmitter contains four 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and five low-voltage differential signaling (LVDS) drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTL data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN65LVDS94.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected via the clock select (CLKSEL) pin. The frequency of CLKIN is multiplied seven times and then used to serially unload the data registers in 7-bit slices. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN65LVDS93 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a low-level input and the possible use of the shutdown/clear ($\overline{\text{SHTDN}}$). $\overline{\text{SHTDN}}$ is an active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers at a low level.

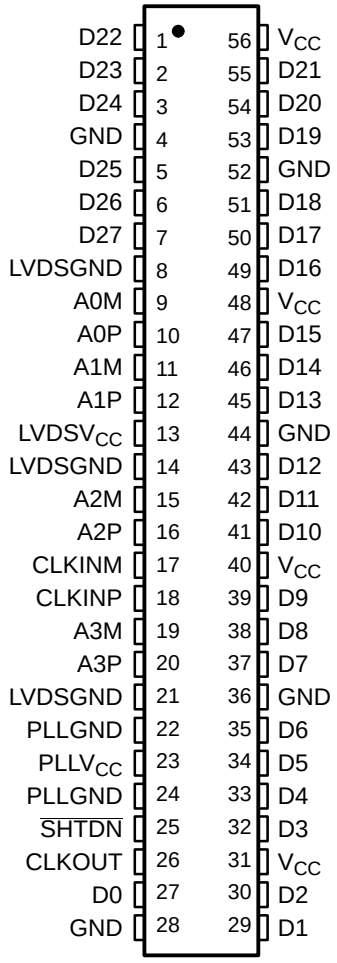
The SN65LVDS93 is characterized for operation over ambient air temperatures of –40°C to 85°C.

functional block diagram



- **4:28 Data Channel Expansion at up to 1.820 Gigabits per Second Throughput**
- **Suited for Point-to-Point Subsystem Communication With Very Low EMI**
- **4 Data Channels and Clock Low-Voltage Differential Channels in and 28 Data and Clock Out Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant $\overline{\text{SHTDN}}$ Input**
- **Rising Clock Edge Triggered Outputs**
- **Bus Pins Tolerate 4-kV HBM ESD**
- **Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch**
- **Consumes <1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 20 MHz to 65 MHz**
- **No External Components Required for PLL**
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-644 Standard**
- **Industrial Temperature Qualified T_A = –40°C to 85°C**
- **Replacement for the DS90CR286**

DGG PACKAGE
(TOP VIEW)



description

The SN65LVDS94 LVDS serdes (serializer/deserializer) receiver contains four serial-in 7-bit parallel-out shift registers, a 7× clock synthesizer, and five low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN65LVDS93 and SN65LVDS95, over five balanced-pair conductors and expansion to 28 bits of single-ended LVTTL synchronous data at a lower transfer rate.

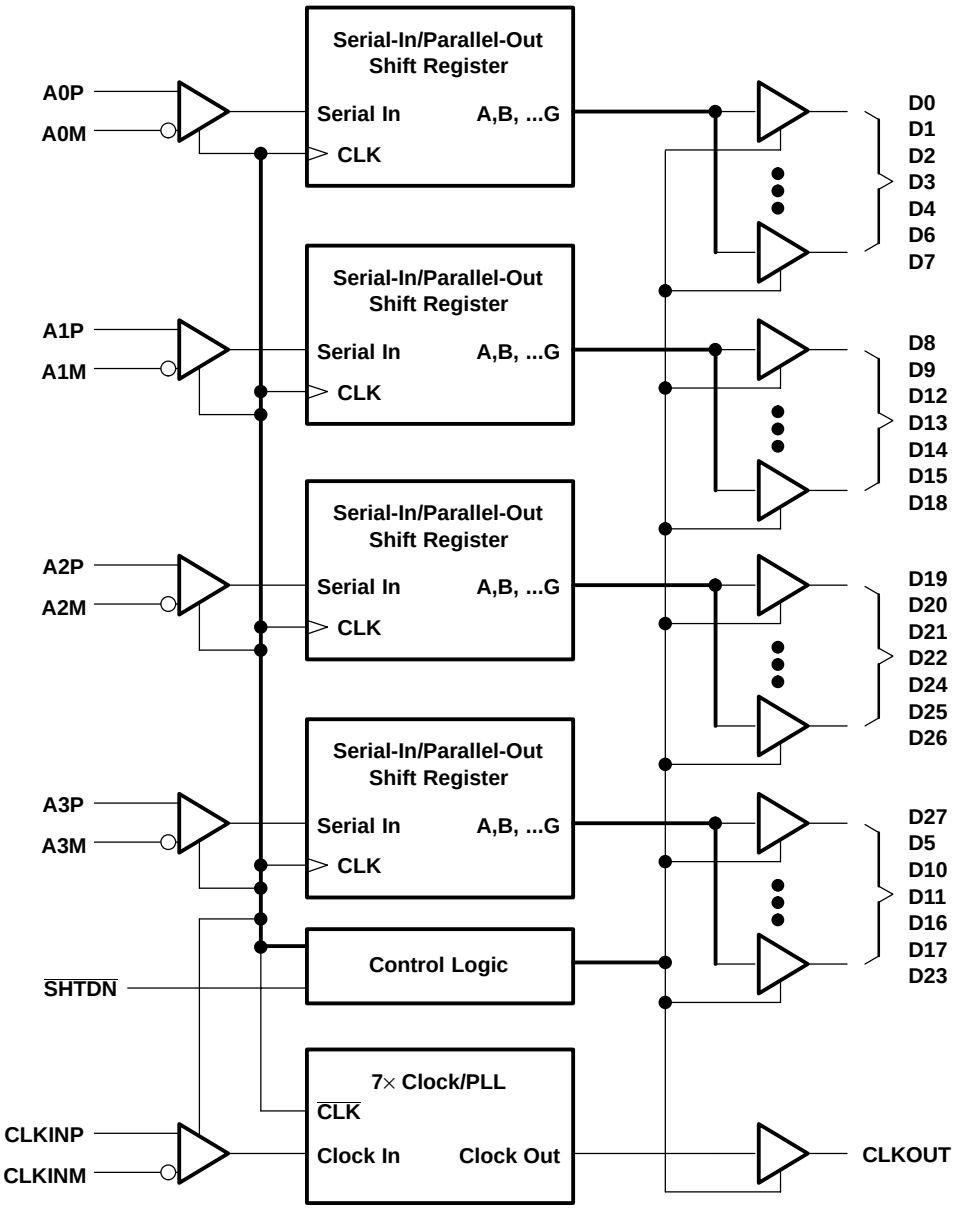
When receiving, the high-speed LVDS data is received and loaded into registers at the rate seven times the LVDS input clock (CLKIN). The data is then unloaded to a 28-bit wide LVTTL parallel bus at the CLKIN rate. A phase-locked loop clock synthesizer circuit generates a 7× clock for internal clocking and an output clock for the expanded data. The SN65LVDS94 presents valid data on the rising edge of the output clock (CLKOUT).

The SN65LVDS94 requires only five line termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN65LVDS94 is characterized for operation over ambient air temperatures of –40°C to 85°C.

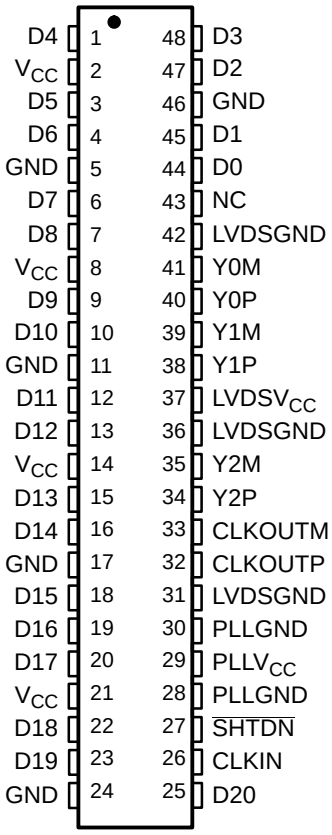
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



- **21:3 Data Channel Compression at up to 1.36 Gigabits per Second Throughput**
- **Suited for Point-to-Point Subsystem Communication With Very Low EMI**
- **21 Data Channels Plus Clock in Low-Voltage TTL and 3 Data Channels Plus Clock Out Low-Voltage Differential**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant Data Inputs**
- **'LVDS95 Has Rising Clock Edge Triggered Inputs**
- **Bus Pins Tolerate 6-kV HBM ESD**
- **Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch**
- **Consumes <1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 20 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Industrial Temperature Qualified T_A = –40°C to 85°C**
- **Replacement for the National DS90CR215**

DGG PACKAGE
(TOP VIEW)



description

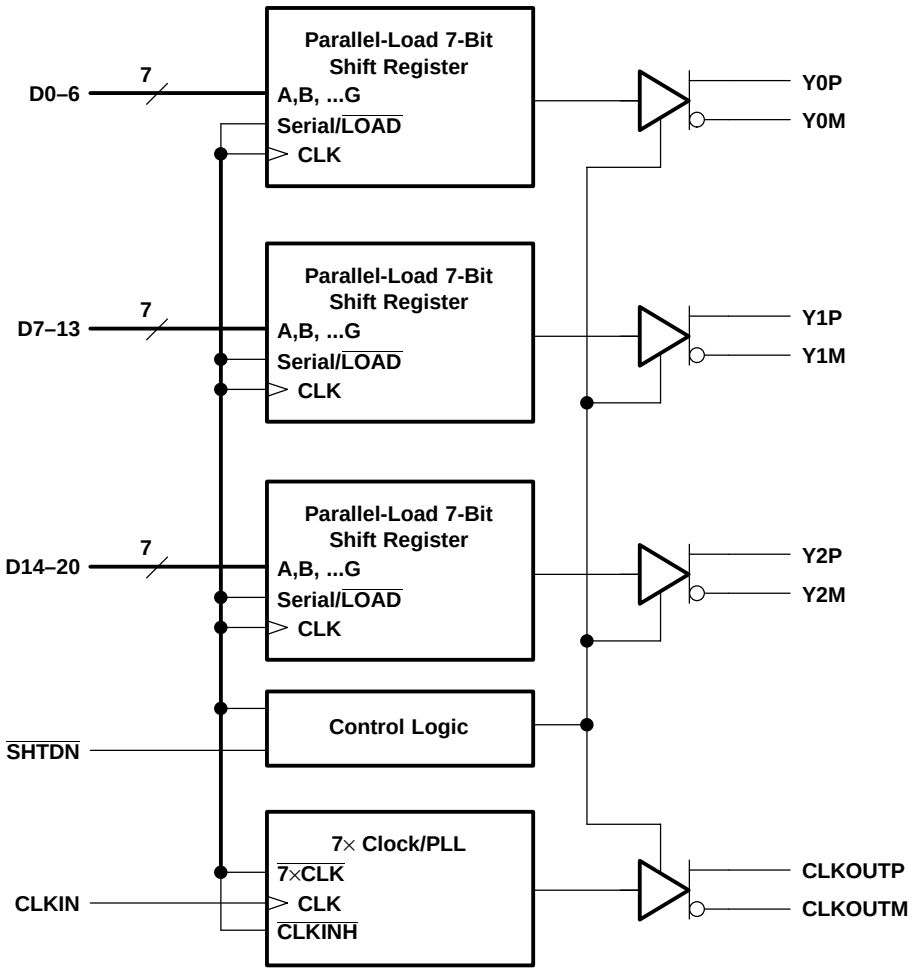
The SN65LVDS95 LVDS serdes (serializer/deserializer) transmitter contains three 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line drivers in a single integrated circuit. These functions allow 21 bits of single-ended LVTTL data to be synchronously transmitted over 4 balanced-pair conductors for receipt by a compatible receiver, such as the SN65LVDS96.

When transmitting, data bits D0 through D20 are each loaded into registers of the SN65LVDS95 on the rising edge of the input clock signal (CLKIN). The frequency of CLKIN is multiplied seven times and then used to serially unload the data registers in 7-bit slices. The three serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN65LVDS95 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

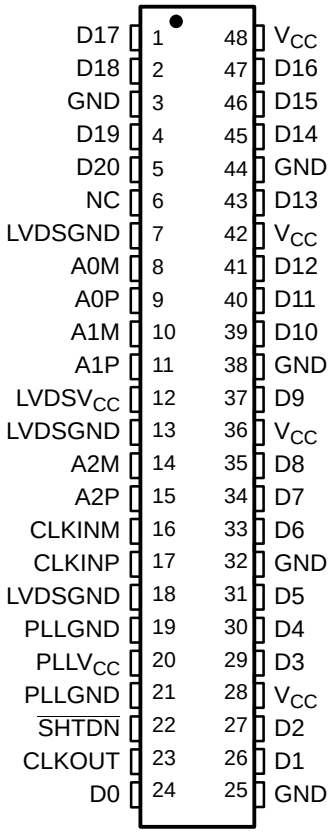
The SN65LVDS95 is characterized for operation over ambient air temperatures of –40°C to 85°C.

functional block diagram



- **3:21 Data Channel Expansion at up to 1.3 Gigabits per Second Throughput**
- **Suited for Point-to-Point Subsystem Communication With Very Low EMI**
- **3 Data Channels and Clock Low-Voltage Differential Channels in and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant $\overline{\text{SHTDN}}$ Input**
- **Rising Clock Edge Triggered Outputs**
- **Bus Pins Tolerate 4-kV HBM ESD**
- **Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch**
- **Consumes <1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 20 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Industrial Temperature Qualified T_A = –40°C to 85°C**
- **Replacement for the DS90CR216**

DGG PACKAGE
(TOP VIEW)



description

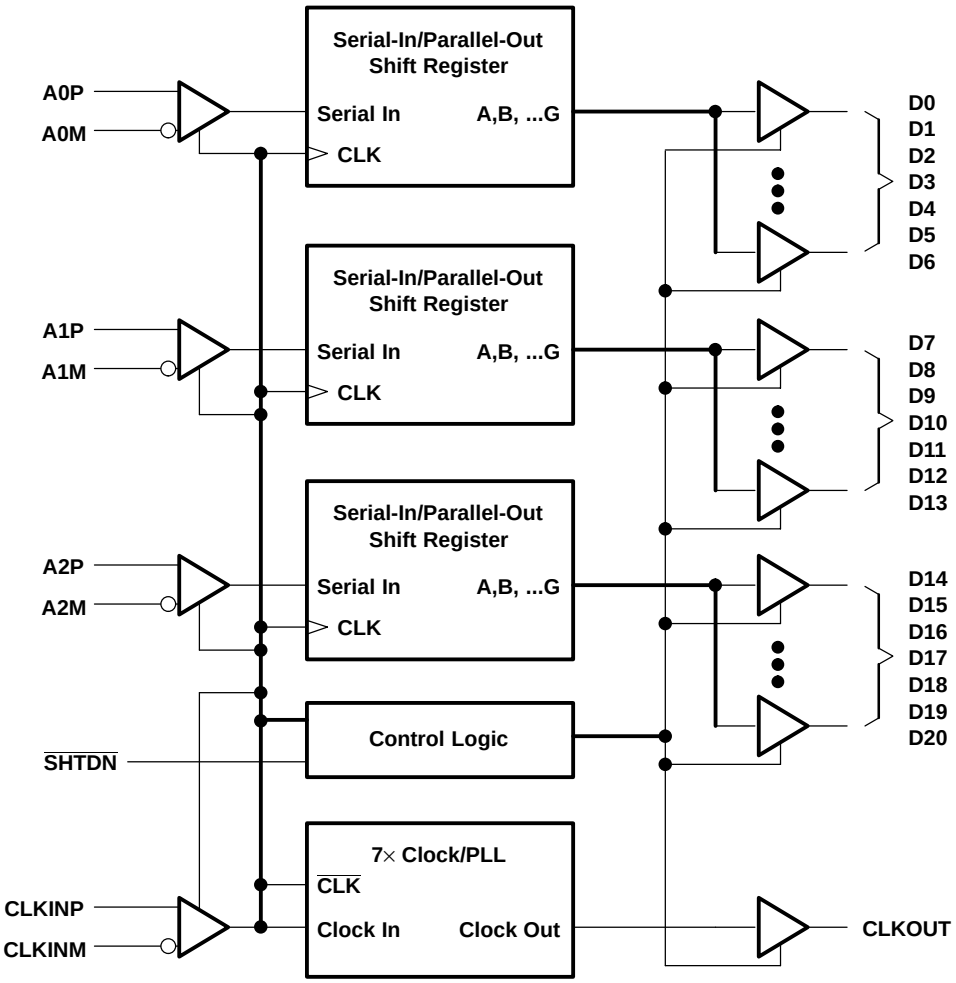
The SN65LVDS96 LVDS serdes (serializer/deserializer) receiver contains three serial-in 7-bit parallel-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN65LVDS95, over four balanced-pair conductors and expansion to 21 bits of single-ended LVTTL synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at the rate of seven times the LVDS input clock (CLKIN). The data is then unloaded to a 21-bit wide LVTTL parallel bus at the CLKIN rate. A phase-locked loop clock synthesizer circuit generates a 7× clock for internal clocking and an output clock for the expanded data. The SN65LVDS96 presents valid data on the rising edge of the output clock (CLKOUT).

The SN65LVDS96 requires only four line termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN65LVDS96 is characterized for operation over ambient air temperatures of –40°C to 85°C.

functional block diagram



SLLS516 – AUGUST 2002

2-Gbps DIFFERENTIAL TRANSLATOR/REPEATER

FEATURES

- **Designed for Signaling Rates[1] up to 2 Gbps**
- **Total Jitter < 65 ps**
- **Low-Power Alternative for the MC100EP16**
- **Low 100 ps (Max) Part-To-Part Skew**
- **25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range**
- **Inputs Electrically Compatible With LVPECL, CML, and LVDS Signal Levels**
- **3.3-V Supply Operation**
- **LVDT Integrates 110-Ω Terminating Resistor**
- **Offered in SOIC and MSOP**
- **Chip Scale Package (Product Preview)**

APPLICATIONS

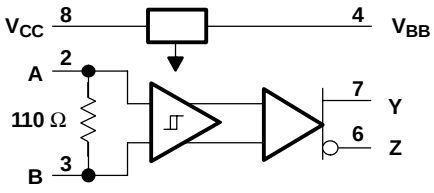
- **622 MHz Central Office Clock Distribution**
- **High-Speed Network Routing**
- **Wireless Basestations**
- **Low Jitter Clock Repeater**
- **Serdes LVPECL o/p to FPGA LVDS i/p Translator**

DESCRIPTION

These high-speed translators/repeaters were designed for signaling rates up to 2 Gbps to address various high-speed network routing applications. Inputs accept LVDS, LVPECL, and CML levels. The SN65LVDx100 provides LVDS outputs while the SN65LVDx101 supports LVPECL outputs. They are compatible with the TIA/EIA-644-A (LVDS) standard (exception; the LVPECL output). Utilization of the LVDS technology allows for low power and high-speed operation. Internal data paths from input to output are fully differential for lower noise generation and low pulse width distortion. Although these devices are designed for 2 Gbps, some applications at a 2.5 Gbps data rate can be supported depending on loading and signal quality. The V_{BB} pin is an internally generated voltage supply to allow operation with single-ended (LVPECL) inputs. For those applications where board space is a premium, the LVDT devices have the integrated 110-Ω termination resistor. All devices are characterized for operation from –40°C to 85°C.

DEVICE	INPUT	OUTPUT
SN65LVDS100	LVDS or LVPECL or CML	LVDS
SN65LVDT100		
SN65LVDS101	LVDS or LVPECL or CML	LVPECL
SN65LVDT101		

FUNCTIONAL DIAGRAM



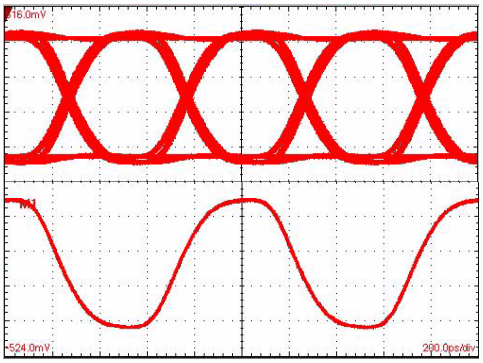
INTEGRATED TERMINATION ON 65LVDT'

EYE PATTERN

2 Gbps
2^{23} – 1 PRBS

V_{CC} = 3.3 V
$|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V
Vertical Scale= 200 mV/div

1 GHz



Horizontal Scale= 200 ps/div

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[1]The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

OUTPUT	TERMINATION RESISTOR	PART NUMBER	PART MARKING	PACKAGE	STATUS
LVDS	No	SN65LVDS100D	DL100	SOIC	Production
LVDS	No	SN65LVDS100DGK	AZK	MSOP	Production
LVDS	Yes	SN65LVDT100D	DE100	SOIC	Production
LVDS	Yes	SN65LVDT100DGK	AZL	MSOP	Production
LVPECL	No	SN65LVDS101D	DL101	SOIC	Production
LVPECL	No	SN65LVDS101DGK	AZM	MSOP	Production
LVPECL	Yes	SN65LVDT101D	DE101	SOIC	Production
LVPECL	Yes	SN65LVDT101DGK	BAF	MSOP	Production

Add the suffix R for taped and reeled carrier (i.e. SN65LVDS100DR).

(1) Chipscale packaging is under consideration for SN65LVDS100 and SN65LVDT100. Contact your local TI sales office for further information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			SN65LVDS100, SN65LVDT100 SN65LVDS101, SN65LVDT101
Supply voltage range,(2) V_{CC}			–0.5 V to 4 V
Sink/source, I_{BB}			±0.5 mA
Voltage range, (A, B, Y, Z)			0 V to 4.3 V
Differential voltage, $\|V_A - V_B\|$ (LVDT only)			1 V
ESD	Human Body Model(3)	A, B, Y, Z, and GND	±5 kV
		All pins	±2 kV
	Charged-Device Model(4)	All pins	±1500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range, T_{stg}			–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.

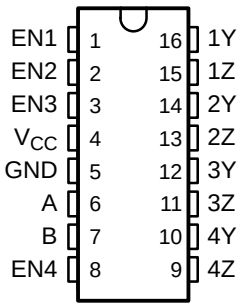
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

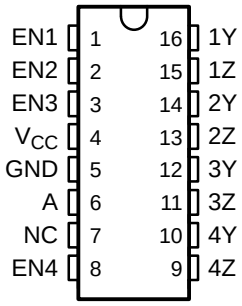
		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Magnitude of differential input voltage $\|V_{ID}\|$	LVDS	0.1		1	V
	LVDT	0.1		0.8	
Input voltage (any combination of common-mode or input signals)		0		4	V
V_{BB} output current				400	µA
Operating free-air temperature, T_A		–40		85	°C

- **Receiver and Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
  - **SN65LVDS105 Receives Low-Voltage TTL (LVTTL) Levels**
  - **SN65LVDS104 Receives Differential Input Levels, ±100 mV**
- **Designed for Signaling Rates up to 630 Mbps**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Propagation Delay Time**
  - **SN65LVDS105 . . . 2.2 ns (Typ)**
  - **SN65LVDS104 . . . 3.1 ns (Typ)**
- **LVTTL Levels Are 5-V Tolerant**
- **Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Networks**
- **Driver Outputs Are High Impedance When Disabled or With V_{CC} <1.5 V**
- **Bus-Pin ESD Protection Exceeds 16 kV**
- **SOIC and TSSOP Packaging**

SN65LVDS104
D OR PW PACKAGE
(Marked as LVDS104)
(TOP VIEW)

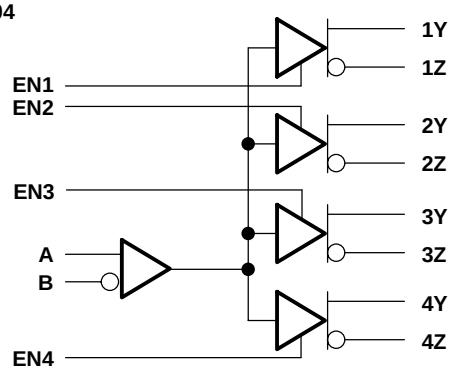


SN65LVDS105
D OR PW PACKAGE
(Marked as LVDS105)
(TOP VIEW)

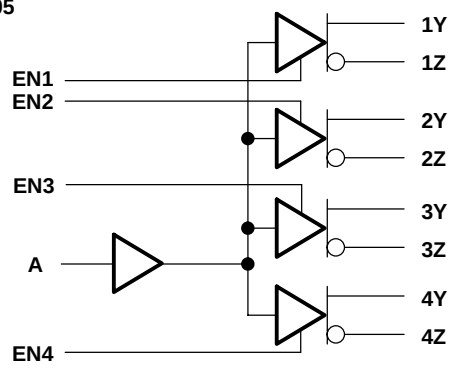


logic diagram (positive logic)

'LVDS104



'LVDS105



description

The SN65LVDS104 and SN65LVDS105 are a differential line receiver and a LVTTL input (respectively) connected to four differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644 is a data signaling technique that offers low-power, low-noise coupling, and switching speeds to transmit data at speeds up to 655 Mbps at relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. Having the drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of the signals repeated from the input. This is particularly advantageous in distribution or expansion of signals such as clock or serial data stream.

The SN65LVDS104 and SN65LVDS105 are characterized for operation from –40°C to 85°C.

description (continued)

The SN65LVDS104 and SN65LVDS105 are members of a family of LVDS repeaters. A brief overview of the family is provided in the table below.

Selection Guide to LVDS Repeaters

DEVICE	NO. INPUTS	NO. OUTPUTS	PACKAGE	COMMENT
SN65LVDS22	2 LVDS	2 LVDS	16-pin D	Dual multiplexed LVDS repeater
SN65LVDS104	1 LVDS	4 LVDS	16-pin D	4-Port LVDS repeater
SN65LVDS105	1 LVTTL	4 LVDS	16-pin D	4-Port TTL-to-LVDS repeater
SN65LVDS108	1 LVDS	8 LVDS	38-pin DBT	8-Port LVDS repeater
SN65LVDS109	2 LVDS	8 LVDS	38-pin DBT	Dual 4-port LVDS repeater
SN65LVDS116	1 LVDS	16 LVDS	64-pin DGG	16-Port LVDS repeater
SN65LVDS117	2 LVDS	16 LVDS	64-pin DGG	Dual 8-port LVDS repeater

Function Tables

SN65LVDS104

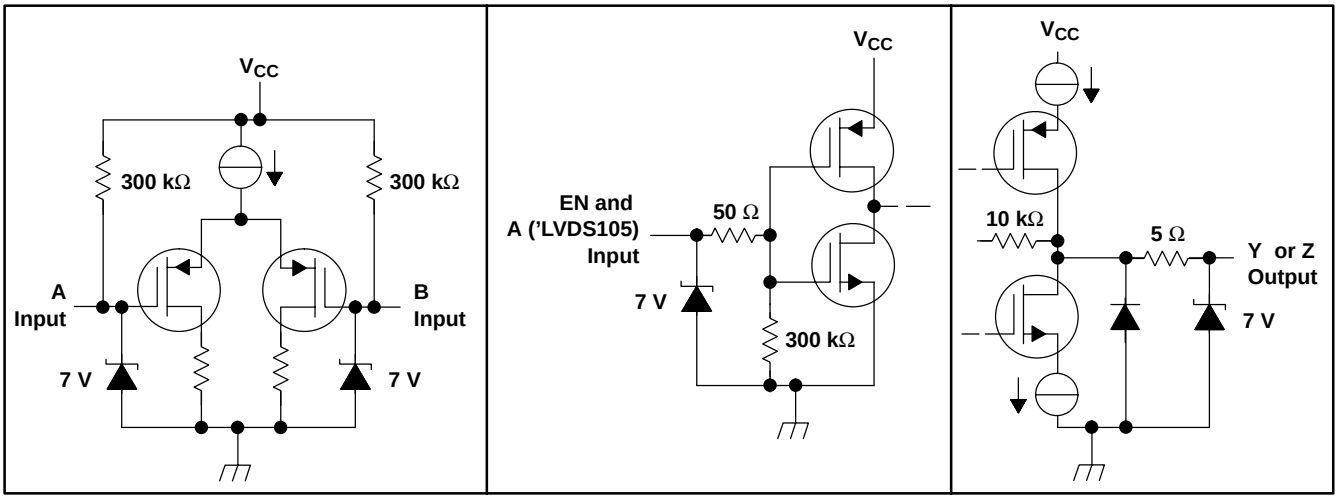
INPUT		OUTPUT	
$V_{ID} = V_A - V_B$	xEN	xY	xZ
X	X	Z	Z
X	L	Z	Z
$V_{ID} \geq 100$ mV	H	H	L
-100 mV $< V_{ID} < 100$ mV	H	?	?
$V_{ID} \leq -100$ mV	H	L	H

SN65LVDS105

INPUT		OUTPUT	
A	ENx	xY	xZ
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z
X	X	Z	Z

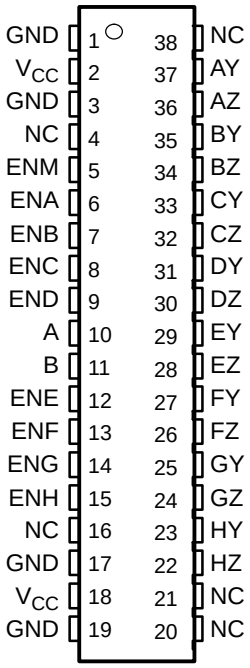
H = high level, L = low level, Z = high impedance, ? = indeterminate, X = don't care

equivalent input and output schematic diagrams



- **One Line Receiver and Eight Line Drivers Configured as an 8-Port LVDS Repeater**
- **Line Receiver and Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Designed for Signaling Rates up to 622 Mbps**
- **Enabling Logic Allows Individual Control of Each Driver Output, Plus All Outputs**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Termination Networks**
- **Propagation Delay Times < 4.7 ns**
- **Output Skew Less Than 300 ps and Part-to-Part Skew Less Than 1.5 ns**
- **Total Power Dissipation at 200 MHz Typically Less Than 330 mW With 8 Channels Enabled**
- **Driver Outputs or Receiver Input Equals High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Bus-Pin ESD Protection Exceeds 12 kV**
- **Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch**

DBT PACKAGE
(TOP VIEW)



NC – No internal connection

description

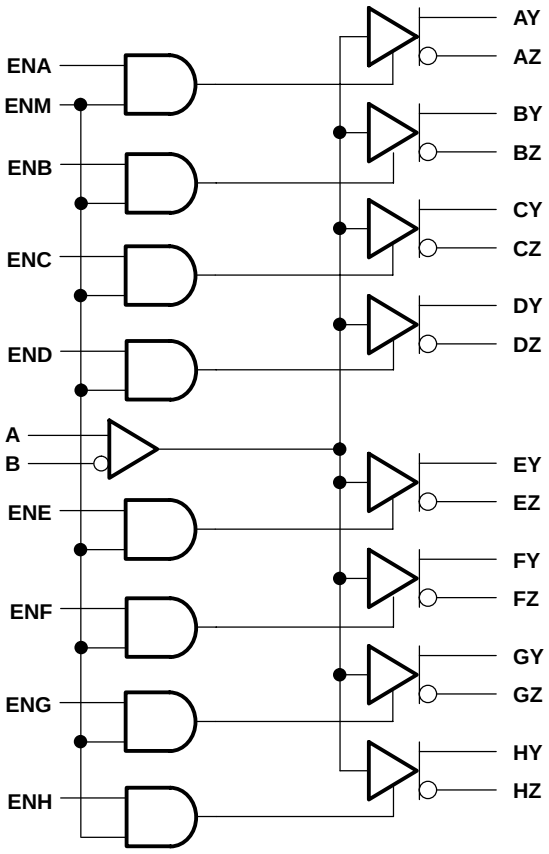
The SN65LVDS108 is configured as one differential line receiver connected to eight differential line drivers. Individual output enables are provided for each output and an additional enable is provided for all outputs.

The line receivers and line drivers implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644, is a data signaling technique that offers low power, low noise emission, high noise immunity, and high switching speeds. It can be used to transmit data at speeds up to at least 622 Mbps and over relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device, and the LVDS signaling technique, is for point-to-point or point-to-multipoint (distributed simplex) baseband data transmission on controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same silicon substrate, along with the low pulse skew of balanced signaling, provides extremely precise timing alignment of the signals being repeated from the inputs. This is particularly advantageous for implementing system clock or data distribution trees.

The SN65LVDS108 is characterized for operation from –40°C to 85°C.

logic diagram (positive logic)



selection guide to LVDS splitter

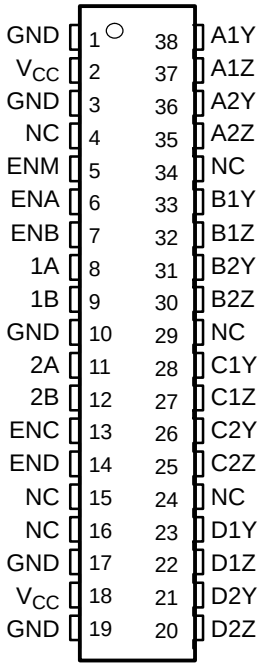
The SN65LVDS108 is one member of a family of LVDS splitters and repeaters. A brief overview of the family is provided in the following table.

LVDS SPLITTER AND REPEATER FAMILY

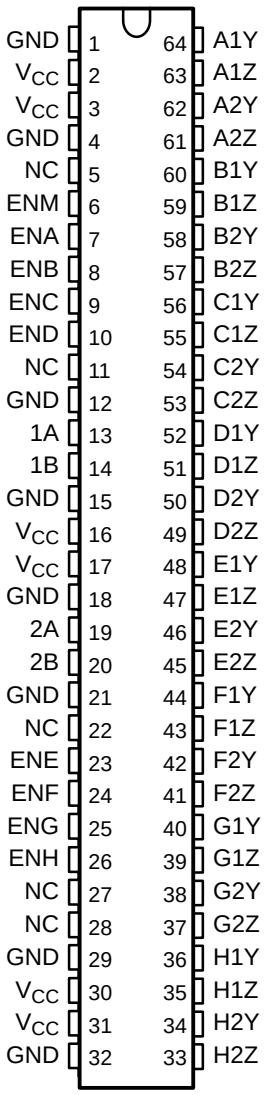
DEVICE	NUMBER OF INPUTS	NUMBER OF OUTPUTS	PACKAGE	COMMENTS
SN65LVDS104	1 LVDS	4 LVDS	16-pin D	4-Port LVDS repeater
SN65LVDS105	1 LVTTL	4 LVDS	16-pin D	4-Port TTL-to-LVDS repeater
SN65LVDS108	1 LVDS	8 LVDS	38-pin DBT	8-Port LVDS repeater
SN65LVDS109	2 LVDS	8 LVDS	38-pin DBT	Dual 4-port LVDS repeater
SN65LVDS116	1 LVDS	16 LVDS	64-pin DGG	16-Port LVDS repeater
SN65LVDS117	2 LVDS	16 LVDS	64-pin DGG	Dual 8-port LVDS repeater

- **Two Line Receivers and Eight (’109) or Sixteen (’117) Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Designed for Signaling Rates up to 632 Mbps**
- **Outputs Arranged in Pairs From Each Bank**
- **Enabling Logic Allows Individual Control of Each Driver Output Pair, Plus All Outputs**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Termination Networks**
- **Propagation Delay Times < 4.5 ns**
- **Output Skew Less Than 550 ps**
  Bank Skew Less Than150 ps
  Part-to-Part Skew Less Than 1.5 ns
- **Total Power Dissipation Typically <500 mW With All Ports Enabled and at 200 MHz**
- **Driver Outputs or Receiver Input Equals High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Bus-Pin ESD Protection Exceeds 12 kV**
- **Packaged in Thin Shrink Small-Outline Package With 20 mil Terminal Pitch**

SN65LVDS109
DBT PACKAGE
(TOP VIEW)



SN65LVDS117
DGG PACKAGE
(TOP VIEW)



description

The SN65LVDS109 and SN65LVDS117 are configured as two identical banks, each bank having one differential line receiver connected to either four (’109) or eight (’117) differential line drivers. The outputs are arranged in pairs having one output from each of the two banks. Individual output enables are provided for each pair of outputs and an additional enable is provided for all outputs.

The line receivers and line drivers implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644, is a data signaling technique that offers low power, low noise emission, high noise immunity, and high switching speeds. It can be used to transmit data at speeds up to at least 622 Mbps and over relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

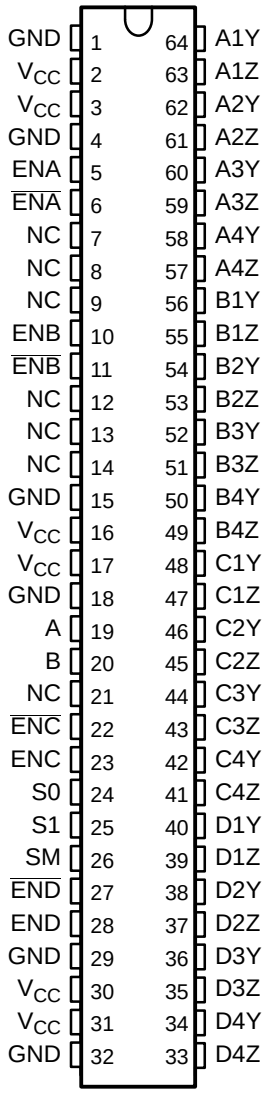
description (continued)

The intended application of these devices, and the LVDS signaling technique, is for point-to-point or point-to-multipoint (distributed simplex) baseband data transmission on controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same silicon substrate, along with the low pulse skew of balanced signaling, provides extremely precise timing alignment of the signals being repeated from the inputs. This is particularly advantageous for implementing system clock and data distribution trees.

The SN65LVDS109 and SN65LVDS117 are characterized for operation from –40°C to 85°C.

- **One Receiver and Sixteen Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Designed for Signaling Rates Up to 622 Mbps**
- **Enabling Logic Allows Separate Control of Each Bank of Four Channels or 2-Bit Selection of Any One of the Four Banks**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Termination Networks**
- **Propagation Delay Times < 4.7 ns**
- **Output Skew Is < 300 ps and Part-to-Part Skew < 1.5 ns**
- **Total Power Dissipation Typically 470 mW With All Ports Enabled and at 200 MHz**
- **Driver Outputs or Receiver Input Is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Bus-Pin ESD Protection Exceeds 12 kV**
- **Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch**

DGG PACKAGE
(TOP VIEW)



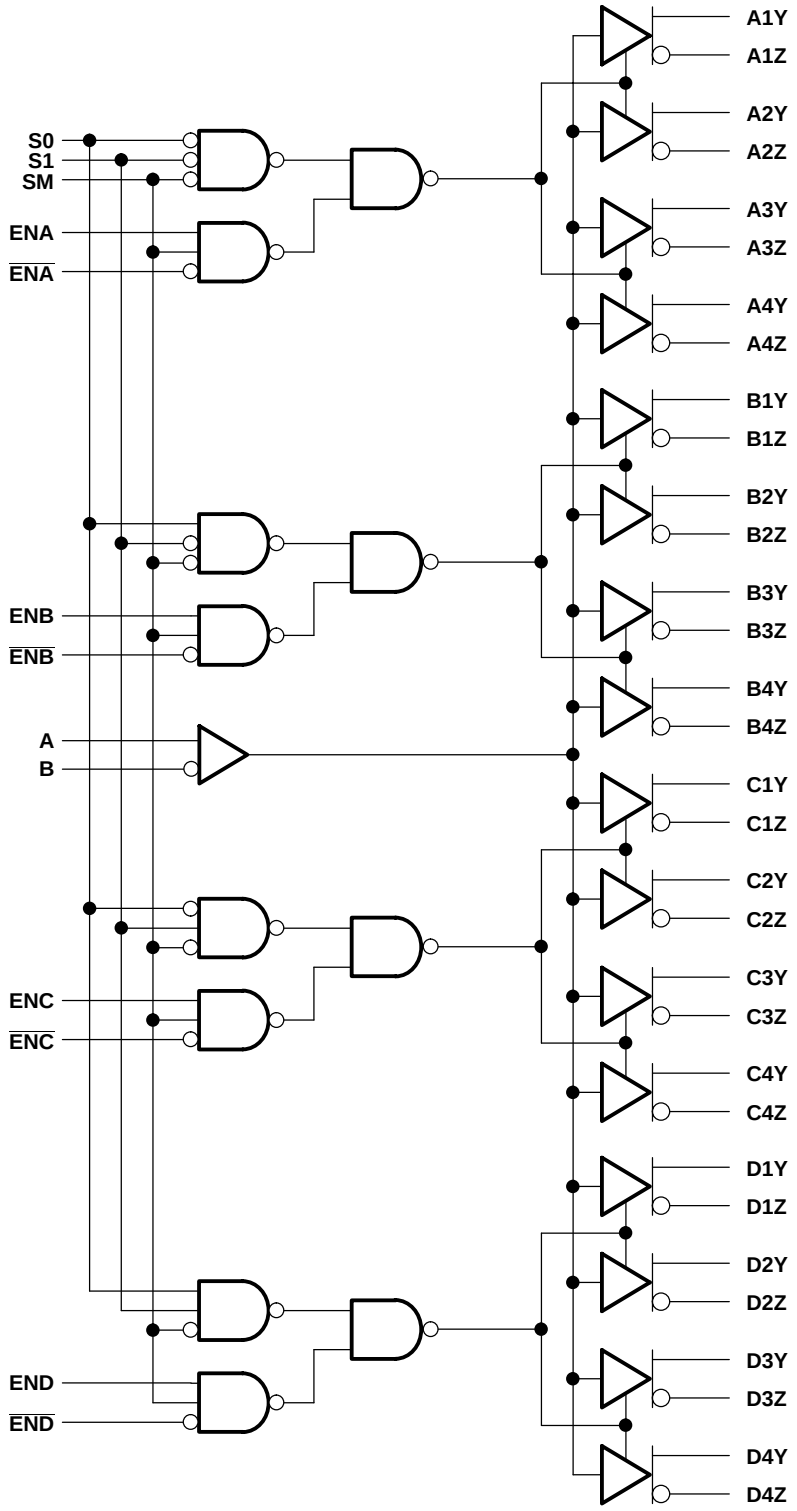
description

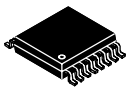
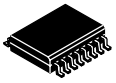
The SN65LVDS116 is one differential line receiver connected to sixteen differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644, is a data signaling technique that offers the low-power, low-noise coupling, and switching speeds to transmit data at speeds up to 622 Mbps and relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device and signaling technique is for point-to-point or multidrop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of the signals repeated from the input. This is particularly advantageous in system clock distribution.

The SN65LVDS116 is characterised for operation from –40°C to 85°C.

logic diagram (positive logic)



1.5-Gbps 2 x 2 LVDS CROSSPOINT SWITCH

FEATURES

- **Designed for Signaling Rates(1) Up To 1.5 Gbps**
- **Total Jitter < 65 ps**
- **Pin-Compatible With SN65LVDS22 and SN65LVDM22**
- **25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range**
- **Inputs Electrically Compatible With CML, LVPECL and LVDS Signal Levels**
- **Propagation Delay Times, 900 ps Maximum**
- **LVDT Integrates 110-Ω Terminating Resistor**
- **Offered in SOIC and TSSOP**

APPLICATIONS

- **10-G (OC–192) Optical Modules**
- **622 MHz Central Office Clock Distribution**
- **Wireless Basestations**
- **Low Jitter Clock Repeater/Multiplexer**
- **Protection Switching for Serial Backplanes**

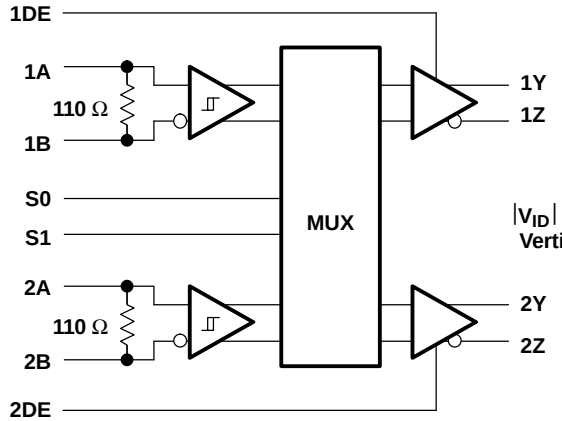
DESCRIPTION

The SN65LVDS122 and SN65LVDT122 are crosspoint switches that use low voltage differential signaling (LVDS) to achieve signaling rates as high as 1.5 Gbps. They are pin-compatible speed upgrades to the SN65LVDS22 and SN65LVDM22. The internal signal paths maintain differential signaling for high speeds and low signal skews. These devices have a 0 V to 4 V common-mode input range that accepts LVDS, LVPECL, CML inputs. Two logic pins (S0 and S1) set the internal configuration between the differential inputs and outputs. This allows the flexibility to perform the following configurations: 2 x 2 crosspoint switch, 2:1 mux, 1:2 splitter or dual repeater/translator within a single device. Additionally, SN65LVDT122 incorporates a 110-Ω termination resistor for those applications where board space is a premium. Although these devices are designed for 1.5 Gbps, some applications at a 2-Gbps data rate can be supported depending on loading and signal quality.

The intended application of this device is ideal for loopback switching for diagnostic routines, fanout buffering of clock/data distribution provide protection in fault-tolerant systems, clock muxing in optical modules, and for overall signal boosting over extended distances.

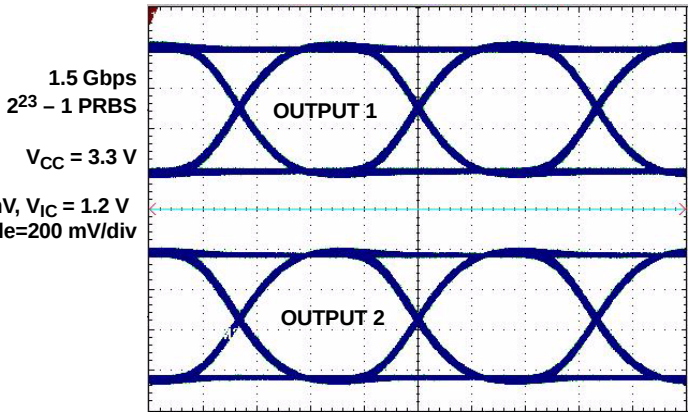
The SN65LVDS122 and SN65LVDT122 are characterized for operation from –40°C to 85°C.

FUNCTIONAL DIAGRAM



Integrated Termination On 65LVDT

EYE PATTERNS OF OUTPUTS OPERATING SIMULTANEOUSLY



Horizontal Scale= 200 ps/div

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

(1)The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PACKAGE	TERMINATION RESISTOR	PART NUMBER(1)	SYMBOLIZATION
SOIC	No	SN65LVDS122D	LVDS122
SOIC	Yes	SN65LVDT122D	LVDT122
TSSOP	No	SN65LVDS122PW	LVDS122
TSSOP	Yes	SN65LVDT122PW	LVDT122

(1) Add the suffix R for taped and reeled carrier

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			SN65LVDS122 SN65LVDT122
Supply voltage range,(2) V_{CC}			–0.5 V to 4 V
Voltage range:	(A, B)		–0.7 V to 4.3 V
	$\lvert V_A–V_B \rvert$ (LVDT only)		1 V
	(DE, S0, S1)		–0.5 V to 4 V
	(Y, Z)		–0.5 V to 4 V
ESD	Human Body Model(3)	A, B, Y, Z, and GND	±4 kV
		All pins	±2 kV
	Charged-Device Model(4)	All pins	±1500 kV
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range, T_{stg}			–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	S0, S1, 1DE, 2DE	2		5	V
Low-level input voltage, V_{IL}	S0, S1, 1DE, 2DE	0		0.8	V
Magnitude of differential input voltage $\lvert V_{ID} \rvert$	LVDS	0.1		1	V
	LVDT	0.1		0.8	
Input voltage (any combination of common-mode or input signals)		0		4	V
Operating free-air temperature, T_A		–40		85	°C

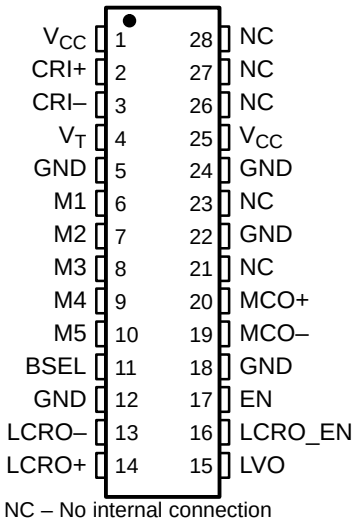
PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
PW	774 mW	6.2 mW/°C	402 mW
D	950 mW	7.6 mW/°C	494 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

- **A Member of the MuxIt™ Serializer-Deserializer Building-Block Chip Family**
- **Pin Selectable Frequency Multiplier Ratios Between 4 and 40**
- **Input Clock Frequencies From 5 to 50 MHz**
- **Multiplied Clock Frequencies up to 400 MHz**
- **Internal Loop Filters and Low PLL-Jitter of 20 ps RMS Typical at 200 MHz**
- **LVDS Compatible Differential Inputs and Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644-A**
- **LVTTL Compatible Inputs Are 5 V Tolerant**
- **LVDS Inputs and Outputs ESD Protection Exceeds 12 kV HBM**
- **Operates From a Single 3.3 V Supply**
- **Packaged in 28-Pin Thin Shrink Small-Outline Package With 26 mil Terminal Pitch**

SN65LVDS150
PW PACKAGE
(Marked as 65LVDS150)



NC – No internal connection

description

The MuxIt is a family of general-purpose, multiple-chip building blocks for implementing parallel data serializers and deserializers. The system allows for wide parallel data to be transmitted through a reduced number of differential transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) data interface. The number of bits multiplexed per transmission line is user selectable, allowing for higher transmission efficiencies than with other existing fixed ratio solutions. MuxIt utilizes the LVDS (TIA/EIA-644) low voltage differential signaling technology for communications between the data source and data destination.

The MuxIt family initially includes three devices supporting simplex communications; *The SN65LVDS150 Phase Locked Loop-Frequency Multiplier, The SN65LVDS151 Serializer-Transmitter,* and *The SN65LVDS152 Receiver-Deserializer.*

The SN65LVDS150 is a PLL based frequency multiplier designed for use with the other members of the MuxIt family of serializers and deserializers. The frequency multiplication ratio is pin selectable over a wide range of values from 4 through 40 to accommodate a broad spectrum of user needs. No external filter components are needed. A PLL lock indicator output is available which may be used to enable link data transfers.

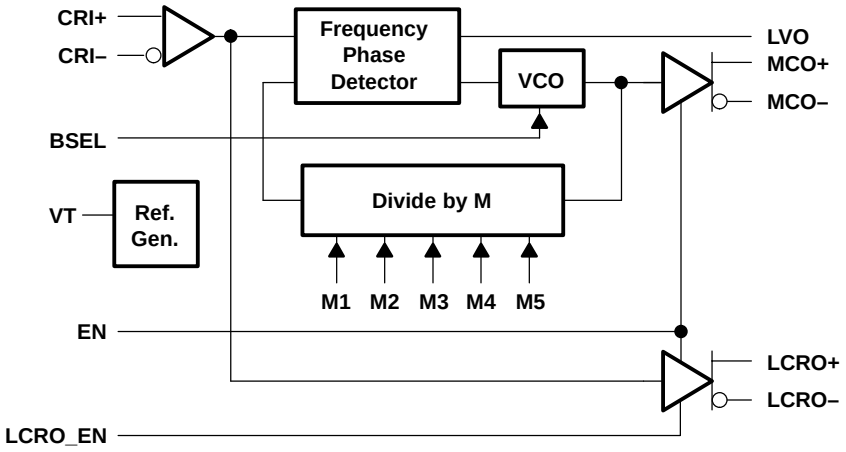
The design of the SN65LVDS150 allows it to be used at either the transmit end or the receive end of the MuxIt serial link. The differential clock reference input (CRI) is driven by the system's parallel data clock when at the source end of the link, or by the link clock when at the destination end of the link. The differential clock reference input may be driven by either an LVDS differential signal, or by a single ended clock of either polarity. For single-ended use the nonclocked input is biased to the logic threshold voltage. A $V_{CC}/2$ threshold reference, VT, is provided on a pin adjacent the differential CRI pins for convenience when the input is used in a single-ended mode.

description (continued)

The multiplied clock output (MCO) is an LVDS differential signal used to drive the high-speed shift registers in either the SN65LVDS151 serializer-transmitter or the SN65LVDS152 receiver-deserializer. The link clock reference output (LCRO) is an LVDS differential signal provided to the SN65LVDS151 serializer-transmitter for transmission over the link.

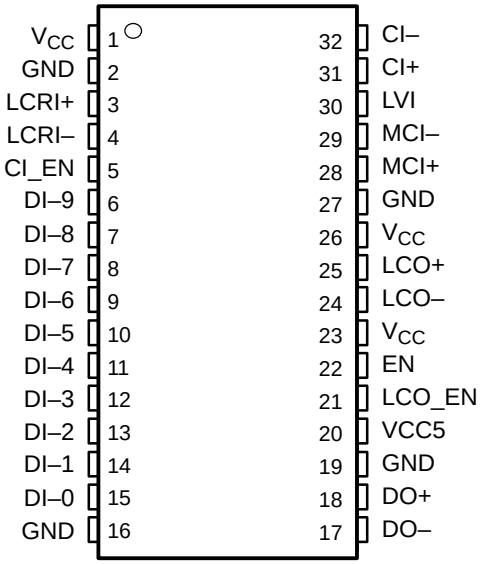
An internal power on reset and an enable input (EN) control the operation of the SN65LVDS150. When V_{CC} is below 1.5 V, or when EN is low, the device is in a low power disabled state and the MCO and LCRO differential outputs are in a high-impedance state. When V_{CC} is above 3 V and EN is high, the device and the two differential outputs are enabled and operating to specifications. The link clock reference output enable input (LCRO_EN) is used to turn off the LCRO output when it is not being used. A band select input (BSEL) is used to optimize the VCO performance as a function of M-clock frequencies and M multiplier that is being used: The f_{max} parameter in the switching characteristic table includes details on the MCO frequency and choices of BSEL and M.

block diagram



- **A Member of the MuxIt™ Serializer-Deserializer Building-Block Chip Family**
- **Supports Serialization of up to 10 Bits of Parallel Data Input at Rates up to 200 Mbps**
- **PLL Lock/Valid Input Provided to Enable Link Data Transfers**
- **Cascadable With Additional SN65LVDS151 MuxIt Serializer-Transmitters for Wider Parallel Input Data Channel Widths**
- **LVDS Compatible Differential Inputs and Outputs Meet or Exceed the Requirements of ANSI TIA/EIA-644-A**
- **LVDS Inputs and Outputs ESD Protection Exceeds 12 kV HBM**
- **LVTTL Compatible Inputs for Lock/Valid, Enables, and Parallel Data Inputs Are 5-V Tolerant**
- **Operates With 3.3 V Supply**
- **Packaged in 32-Pin DA Thin Shrink Small-Outline Package With 26 Mil Terminal Pitch**

SN65LVDS151DA
(Marked as 65LVDS151)



description

MuxIt is a family of general-purpose, multiple-chip building blocks for implementing parallel data serializers and deserializers. The system allows for wide parallel data to be transmitted through a reduced number of transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) data interface. The number of bits multiplexed per transmission line is user-selectable and allows for higher transmission efficiencies than with existing fixed ratio solutions. MuxIt utilizes the LVDS (TIA/EIA-644-A) low voltage differential signaling technology for communications between the data source and data destination.

The MuxIt family initially includes three devices supporting simplex communications: the SN65LVDS150 phase locked loop frequency multiplier, the SN65LVDS151 serializer-transmitter, and the SN65LVDS152 receiver-deserializer.

The SN65LVDS151 consists of a 10-bit parallel-in/serial-out shift register, three LVDS differential transmission line receivers, a pair of LVDS differential transmission line drivers, plus associated input buffers. It accepts up to 10 bits of user data on parallel data inputs (DI–0 → DI–9) and serializes (multiplexes) the data for transmission over an LVDS transmission line link. Two or more SN65LVDS151 units may be connected in series (cascaded) to accommodate wider parallel data paths for higher serialization values. Data is transmitted over the LVDS serial link at M times the input parallel data clock frequency. The multiplexing ratio M, or number of bits per data clock cycle, is programmed on the companion SN65LVDS150 MuxIt programmable PLL frequency multiplier with configuration pins (M1 → M5). The range of multiplexing ratio M supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier is between 4 and 40**.** Table 1 shows some of the combinations of LCRI and MCI supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier.

description (continued)

Data is parallel loaded into the SN65LVDS151 input latches on the first rising edge of the M-clock input (MCI) signal following a rising edge of the link clock reference input (LCRI). The data is read out serially from the SN65LVDS151 shift registers on the rising edges of the M-clock input (MCI). The lowest order bit of parallel input data, DI–0, is output from DO on the third rising edge of MCI following the rising edge of LCRI. The remaining bits of parallel input data, DI-1 $\rightarrow$ DI-(M-1) are clocked out sequentially, in ascending order, by subsequent MCI rising edges. The link clock output (LCO) signal rising edge is synchronized to the data output (DO) by an internal circuit clocked by MCI. The LCO signal rising edge follows the first rising edge of MCI after the rising edge of LCRI. Examples of operating waveforms for values of M = 4 and M = 10 are provided in Figure 1.

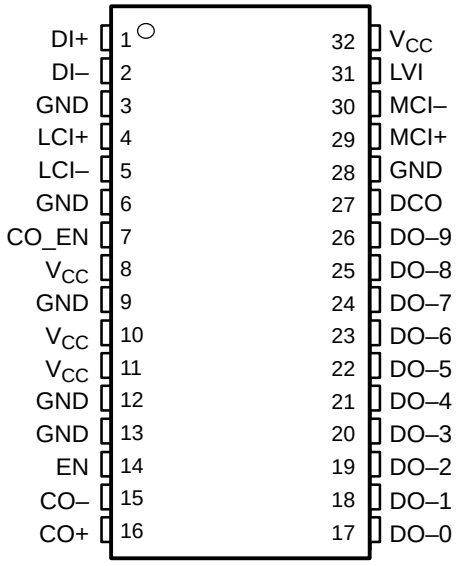
Both the LCRI and MCI signals are intended to be sourced from the SN65LVDS150 MuxIt programmable frequency multiplier. They are carried over LVDS differential connections to minimize skew and jitter. The SN65LVDS151 includes LVDS differential line drivers for both the serialized data output (DO) stream and the link clock output (LCO). The cascade input (CI) is also an LVDS connection, and when it is used it is tied to the DO output of the preceding SN65LVDS151.

An internal power-on reset (POR) and an enable input (EN) control the operation of the SN65LVDS151. When V_{CC} is below 1.5 V, or when EN is low, the device is in a low-power disabled state, and the DO and LCO differential outputs are in a high-impedance state. When V_{CC} is above 3 V and EN is high, the device and the two differential outputs are enabled and operating to specifications. The link clock output enable input (LCO_EN) is used to turn off the LCO output when it is not being used. Cascade input enable (CI_EN) is used to turn off the CI input when it is not being used.

Serialized data bits are output from the DO output, starting in ascending order, from parallel input bit DI–0. The number of serialized data bits output per data clock cycle is determined by the multiplexing ratio M. For values of M less than or equal to 10, the cascade input (CI$\pm$) is not used, and only the first M parallel input bits (DI–0 thought DI–[M–1]) are used. For values of M greater than 10, all ten parallel input bits (DI–0 though DI–9) are used, and the cascade input is used to shift in the remaining data bits from additional SN65LVDS151 serializers. Table 2 shows which input data bits are used as a function of the multiplier M.

- **A Member of the MuxIt™ Serializer-Deserializer Building-Block Chip Family**
- **Supports Deserialization of One Serial Link Data Channel Input at Rates up to 200 Mbps**
- **PLL Lock/Valid Input Provided to Enable Parallel Data and Clock Outputs**
- **Cascadable With Additional SN65LVDS152 MuxIt Receiver–Deserializers for Wider Parallel Output Data Channel Widths**
- **LVDS Compatible Differential Inputs and Outputs Meet or Exceed the Requirements of ANSI TIA/EIA-644-A**
- **LVDS Input and Output ESD Protection Exceeds 12 kV HBM**
- **LVTTL Compatible Inputs for Lock/Valid and Enables Are 5-V Tolerant**
- **Operates With 3.3-V Supply**
- **Packaged in 32-Pin DA Thin Shrink Small-Outline Package With 26-Mil Terminal Pitch**

SN65LVDS152DA
(Marked as 65LVDS152)
(TOP VIEW)



description

MuxIt is a family of general-purpose, multiple-chip building blocks for implementing parallel data serializers and deserializers. The system allows for wide parallel data to be transmitted through a reduced number of transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) data interface. The number of bits multiplexed per transmission line is user selectable, allowing for higher transmission efficiencies than with other existing fixed ratio solutions. MuxIt utilizes the LVDS (TIA/EIA-644-A) low voltage differential signaling technology for communications between the data source and data destination.

The MuxIt family initially includes three devices supporting simplex communications: the SN65LVDS150 phase locked loop frequency multiplier, the SN65LVDS151 serializer-transmitter, and the SN65LVDS152 receiver-deserializer.

The SN65LVDS152 consists of three LVDS differential transmission line receivers, an LVDS differential transmission line driver, a 10-bit serial-in/parallel-out shift register, plus associated input and output buffers. It receives serialized data over an LVDS transmission line link, deserializes (demultiplexes) it, and delivers it on parallel data outputs, DO–0 through DO–9. Data received over the link is clocked at a factor of M times the original parallel data frequency. The multiplexing ratio M, or number of bits per data clock cycle, is programmed with configuration pins (M1 → M5) on the companion SN65LVDS150 MuxIt programmable PLL frequency multiplier. Up to 10 bits of data may be deserialized and output by each SN65LVDS152. Two or more SN65LVDS152 units may be connected in series (cascaded) to accommodate wider parallel data paths for higher serialization values. The range of multiplexing ratio M supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier is between 4 and 40**.** Table 1 shows some of the combinations of LCI and MCI supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier.

description (continued)

Data is serially shifted into the SN65LVDS152 shift register on the falling edges of the M-clock input (MCI). The data is latched out in parallel from the SN65LVDS152 shift register on the second rising edge after the first falling edge of the M-clock following a rising edge of the link clock input (LCI). The SN65LVDS152 includes LVDS differential line receivers for both the serialized link data stream (DI) and link clock (LCI). High-speed signals from the SN65LVDS150 MuxIt programmable frequency multiplier (MCI), plus the input and output for cascaded data (DI, CO) are carried over differential connections to minimize skew and jitter. Examples of operating waveforms for values of M = 4 and M = 10 are provided in Figure 1.

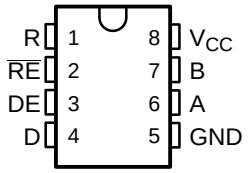
The enable input (EN) along with internal power-on reset (POR) controls the outputs. When Vcc is below 1.5 volts, or when EN is low, outputs are disabled. When V_{CC} is above 3 V and EN is high, outputs are enabled and operating to specifications.

Parallel data bits are output from DO–n outputs in an order dependent on the value of the multiplexing ratio (frequency multiplier value) M. For values of M from 4 through 10, the cascade output (CO+/–) is not used, and only the top M parallel outputs (DO–9 through DO–[10–M]) are used. The data bit output on DO–9 corresponds to the data bit input on DI–[M–1] of the SN65LVDS151 serializer. Likewise, the data bit output on DO–[10–M] will correspond to the data bit input on DI–0 of the SN65LVDS151 serializer.

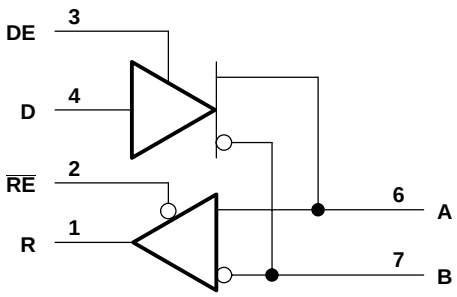
For values of M greater than 10, the cascade output (CO+/–) is used to connect multiple SN65LVDS152 deserializers. In this case the higher-order unit(s) output 10 bits each of the highest numbered bits that are input into the SN65LVDS151 serializer(s). The lowest numbered input bits are output on the lowest-order SN65LVDS152 deserializer in descending order from output DO–9. The number of bits is equal to M mod(10). Table 2 reflects this information, where X = M mod(10)

- **Low-Voltage Differential Driver and Receiver for Half-Duplex Operation**
- **Designed for Signaling Rates of 400 Mbit/s**
- **ESD Protection Exceeds 15 kV on Bus Pins**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 50-Ω Load**
- **Valid Output With as Little as 50 mV Input Voltage Difference**
- **Propagation Delay Times**
  - **Driver: 1.7 ns Typ**
  - **Receiver: 3.7 ns Typ**
- **Power Dissipation at 200 MHz**
  - **Driver: 50 mW Typical**
  - **Receiver: 60 mW Typical**
- **LVTTL Levels Are 5-V Tolerant**
- **Bus Pins Are High Impedance When Disabled or With V_{CC} Less Than 1.5 V**
- **Open-Circuit Fail-Safe Receiver**
- **Surface-Mount Packaging**
  - **D Package (SOIC)**
  - **DGK Package (MSOP)**

SN65LVDM176D (Marked as **DM176** or **LVM176)**
SN65LVDM176DGK (Marked as **M76**)
(TOP VIEW)



logic diagram (positive logic)



description

The SN65LVDM176 is a differential line driver and receiver configured as a transceiver that uses low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbit/s. These circuits are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts except that the output current of the drivers is doubled. This modification provides a minimum differential output voltage magnitude of 247 mV into a 50-Ω load and allows double-terminated lines and half-duplex operation. The receivers detect a voltage difference of less than 50 mV with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of this device and signaling technique is for half-duplex or multiplex baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The SN65LVDM176 is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)†	MSOP (DGK)†
–40°C to 85°C	SN65LVDM176D	SN65LVDM176DGK

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN65LVDM176DR).

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance

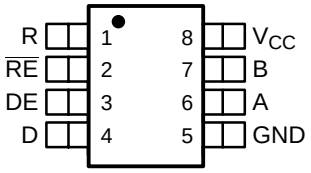
RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 50$ mV	L	H
–50 mV < V_{ID} < 50 mV	L	?
$V_{ID} \leq$ –50 mV	L	L
Open	L	H
X	H	Z

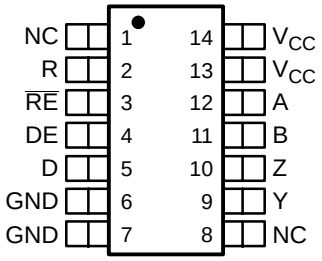
H = high level, L = low level, X = irrelevant,
Z = high impedance

- **Low-Voltage Differential 30-Ω Line Drivers and Receivers for Signaling Rates† up to 200 Mbps**
- **Power Dissipation at 100 Mbps**
  - **Driver: 50 mW Typical**
  - **Receiver: 30 mW Typical**
- **Meets or Exceeds Current Revision of M-LVDS Standard TIA/EIA–899 for Multipoint Data Interchange**
- **Controlled Driver Output Voltage Transition Times for Improved Signal Quality**
- **–1-V to 3.4-V Common-Mode Voltage Range Allows Data Transfer With up to 1 V of Ground Noise**
- **Type-1 Receivers Incorporate 25 mV of Hysteresis**
- **Type-2 Receivers Provide an Offset (100 mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions**
- **Operates From a Single 3.3-V Supply**
- **Propagation Delay Times Typically 2.3 ns for Drivers and 5 ns for Receivers**
- **Power-Up/Down Glitch-Free Driver**
- **Driver Handles Operation Into a Continuous Short Circuit Without Damage**

SN65MLVD200D (Marked as MF200)
SN65MLVD201D (Product Preview)
SN65MLVD204D (Marked as MF204)
(TOP VIEW)



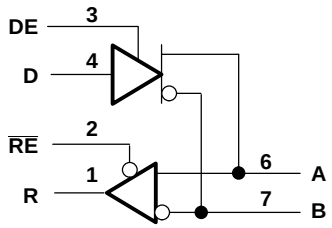
SN65MLVD202D (Marked as MLVD202)
SN65MLVD203D (Product Preview)
SN65MLVD205D (Marked as MLVD205)
(TOP VIEW)



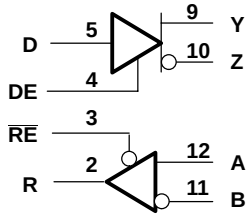
NC – No internal connection

logic diagram (positive logic)

SN65MLVD200, SN65MLVD201, SN65MLVD204



SN65MLVD202, SN65MLVD203, SN65MLVD205



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†The signaling rate of a line is the number of voltage transitions that are made per second expressed in bps (bits per second) units.

description

The SN65MLVD200, SN65MLVD201, SN65MLVD202, SN65MLVD203, SN65MLVD204, and SN65MLVD205 are low-voltage differential line drivers and receivers complying with the proposed multipoint low-voltage differential signaling (M-LVDS) standard (TIA/EIA–899). These circuits are similar to their TIA/EIA-644 standard compliant LVDS counterparts, with added features to address multipoint applications. Driver output current has been increased to support doubly-terminated, 50-Ω load multipoint applications. Driver output slew rates are optimized for signaling rates of 100 Mbps (SN65MLVD200, SN65MLVD202, SN65MLVD204, and SN65MLVD205), and 200 Mbps (SN65MLVD201 and SN65MLVD203).

Types 1 and 2 receivers are available. Both types of receivers operate over a common-mode voltage range of –1 V to 3.4 V to provide increased noise immunity in harsh electrical environments. Type-1 receivers have their differential input voltage thresholds near zero volts (±50 mV), and include 25 mV of hysteresis to prevent output oscillations in the presence of noise. Type-2 receivers include an offset threshold to detect open-circuit, idle-bus, and other fault conditions, and provide a known output state under these conditions.

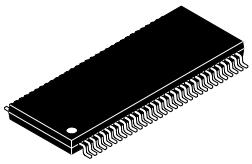
The intended application of these devices is in half-duplex or multipoint baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application-specific characteristics).

The SN65MLVD200, SN65MLVD201, SN65MLVD202, SN65MLVD203, SN65MLVD204, and SN65MLVD205 are characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

NOMINAL SIGNALING RATE, Mbps	FOOTPRINT	RECEIVER TYPE	PART NUMBER†	STATUS
100	SN75176	Type 1	SN65MLVD200D	Production
200	SN75176	Type 1	SN65MLVD201D	Product Preview
100	SN75ALS180	Type 1	SN65MLVD202D	Production
200	SN75ALS180	Type 1	SN65MLVD203D	Product Preview
100	SN75176	Type 2	SN65MLVD204D	Production
100	SN75ALS180	Type 2	SN65MLVD205D	Production

† The D package is available taped and reeled. Add the R suffix to the device type (e.g., SN65MLVD200DR)



SLLS462 – AUGUST 2001

HIGH-SPEED DIFFERENTIAL 8-BIT REGISTERED TRANSCEIVER

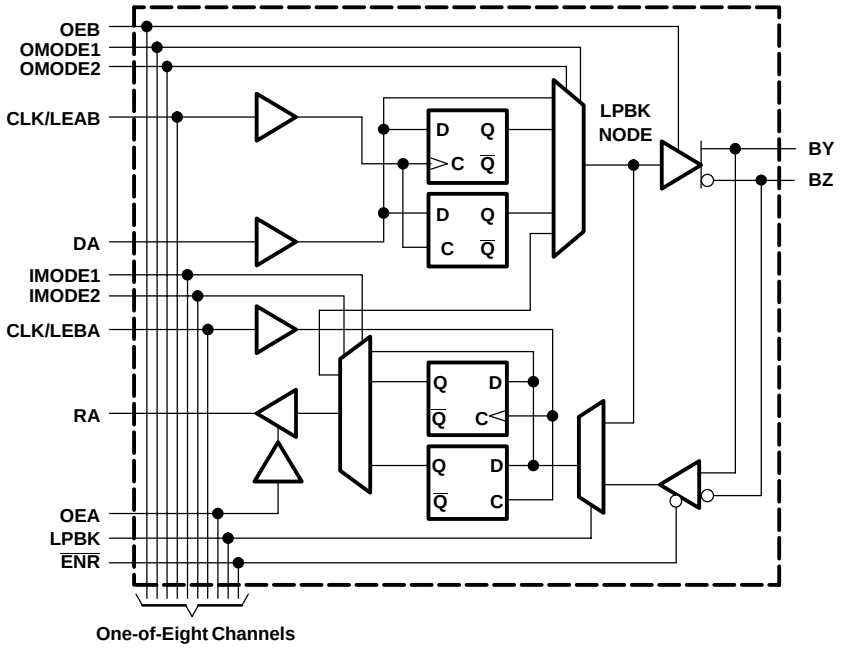
FEATURES

- 8-Bit Bidirectional Data Storage Register With Full Parallel Access
- Parallel Transfer Rates†
  - Buffer Mode: Up to 475 Megatransfers
  - Flip-Flop Mode: Up to 300 Megatransfers
  - Latch Mode: Up to 300 Megatransfers
- Operates With a Single 3.3-V Supply
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV Across a 50-Ω Load
- Bus and Logic Loopback Capability
- Very Low Radiation Emission
- Low Skew Performance
  - Pulse Skew Less Than 100 ps
  - Output Skew Less Than 320 ps
  - Part-to-Part Skew Less Than 1 ns
- Open-Circuit Differential Receiver Fail Safe Assures a Low-Level Output
- Reset at Power Up
- 12-kV Bus-Pin ESD Protection
- Bus Pins Remain High-Impedance When Disabled or With V_{CC} Below 1.5 V for Power-Up/Down Glitch-Free Performance and Hot Plugging
- 5-V Tolerant LVCMOS Inputs

APPLICATIONS

- Telecom Switching
- Printers and Copiers
- Audio Mixing Consoles
- Automated Test Equipment

logic diagram



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†Parallel data transfer through all channels simultaneously as defined by TIA/EIA–644 with t_r of t_f less than 30%of the unit interval.

DESCRIPTION

The SN65LVDM320 is an 8-bit data storage register with differential line drivers and receivers that are electrically compatible with ANSI EIA/TIA-644 for multipoint architectures with standard-compliant parallel transfer rates of 475 Mbps. The SN65LVDM320 includes transmitter and receiver data registers that remain active regardless of the state of their associated outputs.

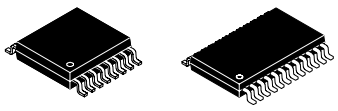
The logic element for data flow in each direction is configured by mode-control inputs. IMODE1 and IMODE2 control data flow in the B-to-A (bus side to digital side) direction when configured as a buffer, a D-type flip-flop, or a D-type latch. OMODE1 and OMODE2 control data flow in each of the operating modes for the A-to-B (digital side to bus side) direction. When configured in buffer mode, input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input, CLKAB/LEAB or CLKBA/LEBA. In the latch mode, this clock pin also serves as an active-high transparent latch enable.

Data flow is further controlled by the A-side loopback (LPBK) input. When LPBK is high, DA input data is looped back to the RA output. B-side bus data is looped back to the bus in latch mode by means of the IMODE and OMODE logic states.

The A-side output enable/disable control is provided by OEA. When OEA is low or V_{CC} is less than 2 V, the A side is in the high-impedance state. When OEA is high, the A side is active (high or low logic levels). The B-side output enable/disable control is provided by OEB. When OEB is low or V_{CC} is less than 2 V, the B side is in the high impedance state. When OEB is high, the B side is active (high or low logic levels).

The A-to-B and B-to-A logic elements are active regardless of the state of their associated outputs. New data can be entered (in latch and flip-flop modes) or previously stored data can be retained while the associated outputs are in the high-impedance or inactive states. The SN65LVDM320 also includes internally isolated analog (B-side) and digital (A-side) grounds for enhanced operation.

The SN65LVDM320 is characterized for operation from –40°C to 85°C.



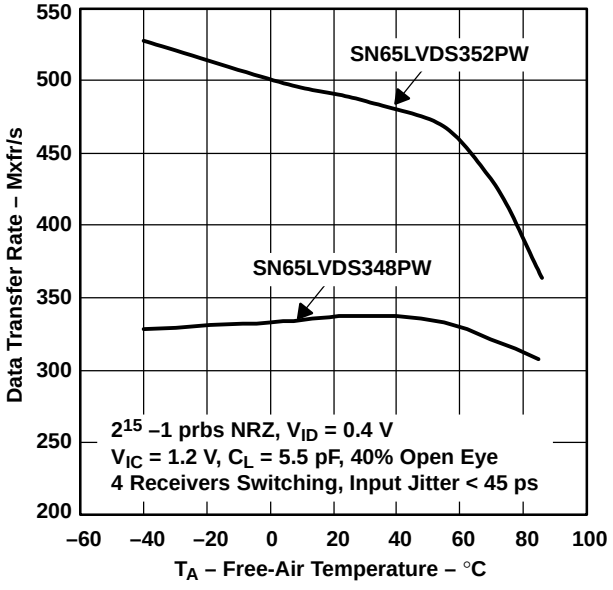
SLLS523B – FEBRUARY 2002 REVISED JULY 2002

QUAD HIGH-SPEED DIFFERENTIAL RECEIVERS

FEATURES

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644A Standard**
- **Single-Channel Signaling Rates[1] up to 560 Mbps**
- **–4 V to 5 V Common-Mode Input Voltage Range**
- **Flow-Through Architecture**
- **Active Failsafe Assures a High-level Output When an Input Signal Is not Present**
- **SN65LVDS348 Provides a Wide Common-Mode Range Replacement for the SN65LVDS048A or the DS90LV048A**

DATA TRANSFER RATE vs FREE-AIR TEMPERATURE

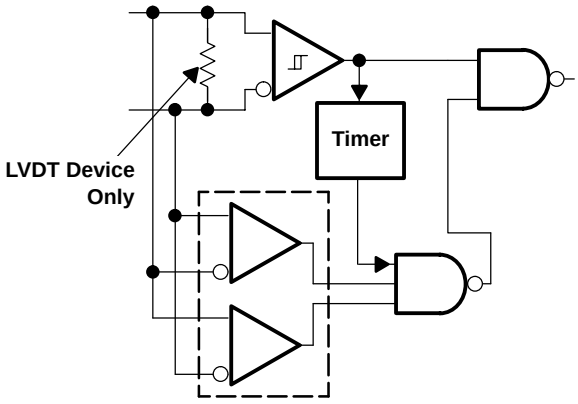


APPLICATIONS

- **Logic Level Translator**
- **Point-to-Point Baseband Data Transmission Over 100-Ω Media**
- **ECL/PECL-to-LVTTL Conversion**
- **Wireless Base Stations**
- **Central Office or PABX Switches**

DESCRIPTION

The SN65LVDS348, SN65LVDT348, SN65LVDS352, and SN65LVDT352 are high-speed, quadruple differential receivers with a wide common-mode input voltage range. This allows receipt of TIA/EIA-644 signals with up to 3-V of ground noise or a variety of differential and single-ended logic levels. The ‘348 is in a 16-pin package to match the industry-standard footprint of the DS90LV048. The ‘352 adds two additional V_{CC} and GND pins in a 24-pin package to provide higher data transfer rates with multiple receivers in operation. All offer a flow-through architecture with all inputs on one side and outputs on the other to ease board layout and reduce crosstalk between receivers. LVDT versions of both integrate a 110-Ω line termination resistor.



(One of Four Shown)

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[1] The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

description (continued)

These receivers also provide 3x the standard's minimum common-mode noise voltage tolerance. The –4 V to 5 V common-mode range allows usage in harsh operating environments or accepts LVPECL, PECL, LVECL, ECL, CMOS, and LVCMOS levels without level shifting circuitry. See the Application Information Section for more details on the ECL/PECL to LVDS interface.

Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input-voltage hysteresis to improve noise rejection. The differential input thresholds are still no more than ±50 mV over the full input common-mode voltage range.

The receiver inputs can withstand ±15 kV human-body model (HBM), with respect to ground, without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

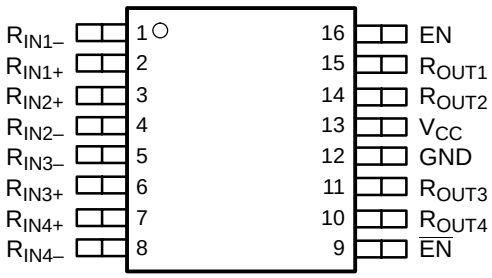
The receivers also include a (patent-pending) failsafe circuit that provides a high-level output within 500 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. This prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling.

The SN65LVDT348 and SN65LVDT352 include an integrated termination resistor. This reduces board space requirements and parts count by eliminating the need for a separate termination resistor. This can also improve signal integrity at the receiver by reducing the stub length from the line termination to the receiver.

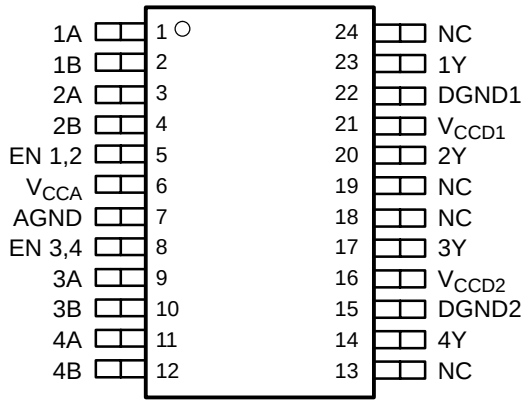
The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS348, SN65LVDT348, SN65LVDS352 and SN65LVDT352 are characterized for operation from –40°C to 85°C.

SN65LVDS348, SN65LVDT348
D or PW PACKAGE
(TOP VIEW)



SN65LVDS352, SN65LVDT352
PW PACKAGE
(TOP VIEW)



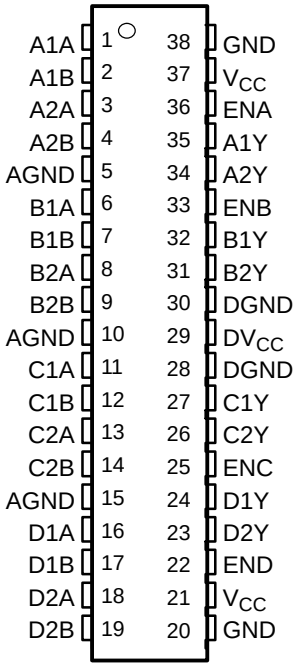
NC – No internal connection

- **Four (’390), Eight (‘388A), or Sixteen (‘386) Line Receivers Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard**
- **Integrated 110-Ω Line Termination Resistors on LVDT Products**
- **Designed for Signaling Rates† Up To 630 Mbps**
- **SN65 Version’s Bus-Terminal ESD Exceeds 15 kV**
- **Operates From a Single 3.3-V Supply**
- **Typical Propagation Delay Time of 2.6 ns**
- **Output Skew 100 ps (Typ)**
  Part-To-Part Skew Is Less Than 1 ns
- **LVTTL Levels Are 5-V Tolerant**
- **Open-Circuit Fail Safe**
- **Flow-Through Pin Out**
- **Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch**

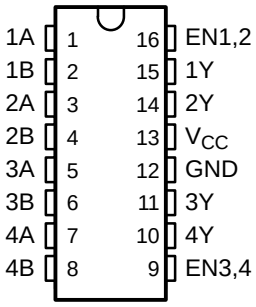
description

This family of four, eight, or sixteen differential line receivers (with optional integrated termination) implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3-V supply rail. Any of the eight or sixteen differential receivers will provide a valid logical output state with a ±100 mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes. Additionally, the high-speed switching of LVDS signals almost always requires the use of a line impedance matching resistor at the receiving end of the cable or transmission media. The LVDT products eliminate this external resistor by integrating it with the receiver.

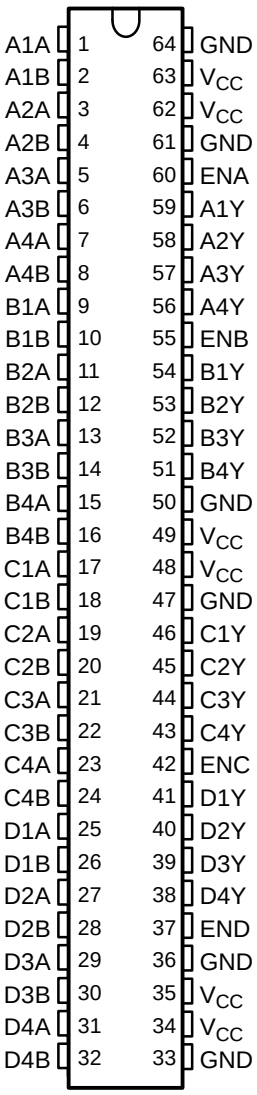
’LVDS388A, ’LVDT388A
DBT PACKAGE
(TOP VIEW)



’LVDS390, ’LVDT390
D OR PW PACKAGE
(TOP VIEW)



’LVDS386, ’LVDT386
DGG PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

description (continued)

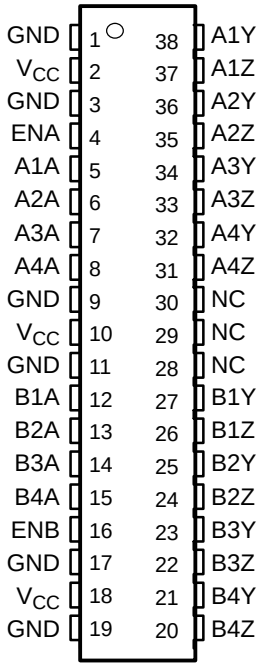
The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of receivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with its companion, 8- or 16-channel driver, the SN65LVDS389 or SN65LVDS387, over 300 million data transfers per second in single-edge clocked systems are possible with very little power. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

AVAILABLE OPTIONS

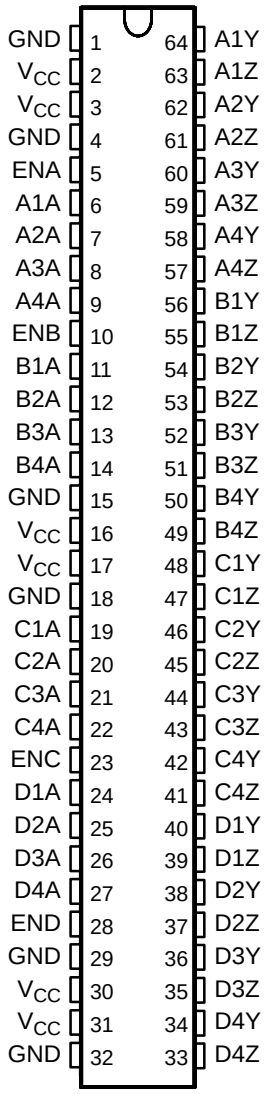
PART NUMBER	TEMPERATURE RANGE	NUMBER OF RECEIVERS	BUS-PIN ESD	SYMBOLIZATION
SN65LVDS386DGG	–40°C to 85°C	16	15 kV	LVDS386
SN65LVDT386DGG	–40°C to 85°C	16	15 kV	LVDT386
SN75LVDS386DGG	0°C to 70°C	16	4 kV	75LVDS386
SN75LVDT386DGG	0°C to 70°C	16	4 kV	75LVDT386
SN65LVDS388ADBT	–40°C to 85°C	8	15 kV	LVDS388A
SN65LVDT388ADBT	–40°C to 85°C	8	15 kV	LVDT388A
SN75LVDS388ADBT	0°C to 70°C	8	4 kV	75LVDS388A
SN75LVDT388ADBT	0°C to 70°C	8	4 kV	75LVDT388A
SN65LVDS390D	–40°C to 85°C	4	15 kV	LVDS390
SN65LVDS390PW	–40°C to 85°C	4	15 kV	LVDS390
SN65LVDT390D	–40°C to 85°C	4	15 kV	LVDT390
SN65LVDT390PW	–40°C to 85°C	4	15 kV	LVDT390
SN75LVDS390D	0°C to 70°C	4	4 kV	75LVDS390
SN75LVDS390PW	0°C to 70°C	4	4 kV	DS390
SN75LVDT390D	0°C to 70°C	4	4 kV	75LVDT390
SN75LVDT390PW	0°C to 70°C	4	4 kV	DG390

- **Four (’391), Eight (’389) or Sixteen (’387) Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Designed for Signaling Rates† up to 630 Mbps With Very Low Radiation (EMI)**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Propagation Delay Times Less Than 2.9 ns**
- **Output Skew Is Less Than 150 ps**
- **Part-to-Part Skew Is Less Than 1.5 ns**
- **35-mW Total Power Dissipation in Each Driver Operating at 200 MHz**
- **Driver Is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **SN65’ Version Bus-Pin ESD Protection Exceeds 15 kV**
- **Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch**
- **Low-Voltage TTL (LVTTL) Logic Inputs Are 5-V Tolerant**

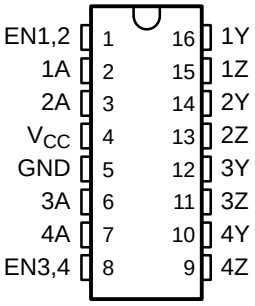
’LVDS389
DBT PACKAGE
(TOP VIEW)



’LVDS387
DGG PACKAGE
(TOP VIEW)



’LVDS391
D OR PW PACKAGE
(TOP VIEW)



description

This family of four, eight, and sixteen differential line drivers implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the sixteen current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of this device and signaling technique is for point-to-point and multidrop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media can be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with the companion 16- or 8-channel receivers, the SN65LVDS386 or SN65LVDS388, over 300 million data transfers per second in single-edge clocked systems are possible with very little power. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

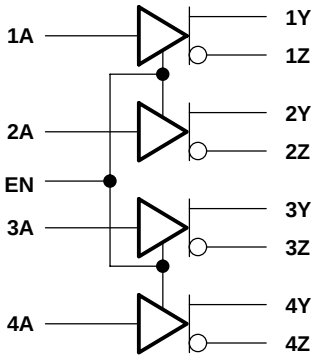
† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

description (continued)

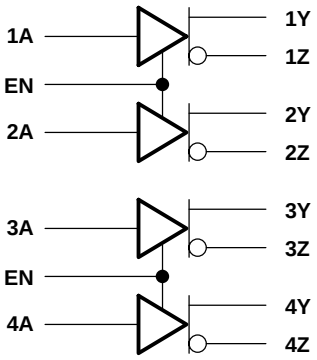
When disabled, the driver outputs are high impedance. Each driver input (A) and enable (EN) have an internal pulldown that will drive the input to a low level when open circuited.

The SN65LVDS387, SN65LVDS389, and SN65LVDS391 are characterized for operation from –40°C to 85°C. The SN75LVDS387, SN75LVDS389, and SN75LVDS391 are characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



(1/4 of ’LVDS387 or 1/2 of ’LVDS389 shown)



(’LVDS391 shown)

AVAILABLE OPTIONS

PART NUMBER†	TEMPERATURE RANGE	NO. OF DRIVERS	BUS-PIN ESD
SN65LVDS387DGG	–40°C to 85°C	16	15 kV
SN75LVDS387DGG	0°C to 70°C	16	4 kV
SN65LVDS389DBT	–40°C to 85°C	8	15 kV
SN75LVDS389DBT	0°C to 70°C	8	4 kV
SN65LVDS391D	–40°C to 85°C	4	15 kV
SN75LVDS391D	0°C to 70°C	4	4 kV
SN65LVDS391PW	–40°C to 85°C	4	15 kV
SN75LVDS391PW	0°C to 70°C	4	4 kV

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., SN65LVDS387DGGR).

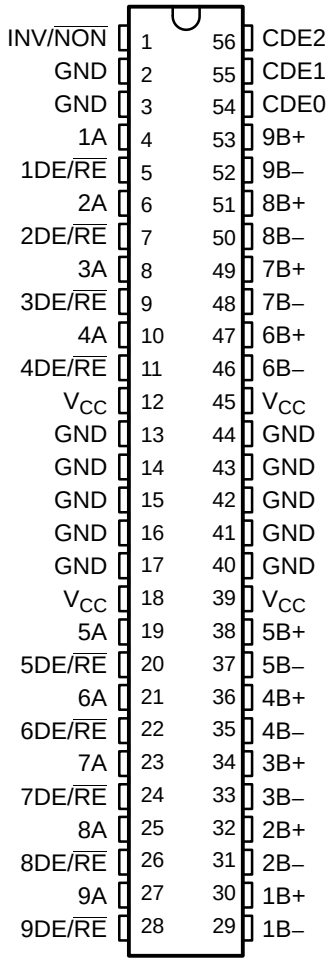
DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS	
A	EN	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
OPEN	H	L	H

H = high-level, L = low-level, X = irrelevant,
Z = high-impedance (off)

- **9 Channels for the Data and Control Paths of the Small Computer Systems Interface (SCSI)**
- **Supports Single-Ended and Low-Voltage Differential (LVD) SCSI**
- **CMOS Input Levels (’LVDM976) or TTL Input Levels (’LVDM977) Available**
- **Includes DIFFSENS Comparators on CDE0**
- **Single-Ended Receivers Include Noise Pulse Rejection Circuitry**
- **Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch**
- **Low Disabled Supply Current 7 mA Maximum**
- **Power-Up/Down Glitch Protection**
- **Bus is High-Impedance With V_{CC} = 1.5 V**
- **Pin-Compatible With the SN75976ADGG High-Voltage Differential Transceiver**

DGG PACKAGE
(TOP VIEW)



description

The SN75LVDM976 and SN75LVDM977 have nine transceivers for transmitting or receiving the signals to or from a SCSI data bus. They offer electrical compatibility to both the single-ended signaling of X3.277:1996–SCSI–3 Parallel Interface (Fast–20) and the new low-voltage differential signaling method of proposed standard 1142–D SCSI Parallel Interface – 2 (SPI–2).

The differential drivers are nonsymmetrical. The SCSI bus uses a dc bias on the line to allow terminated fail safe and wired-OR signaling. This bias can be as high as 125 mV and induces a difference in the high-to-low and low-to-high transition times of a symmetrical driver. In order to reduce pulse skew, an LVD SCSI driver’s output characteristics become nonsymmetrical. In other words, there is more assertion current than negation current to or from the driver. This allows the actual differential signal voltage on the bus to be symmetrical about 0 V. Even though the driver output characteristics are nonsymmetrical, the design of the ’LVDM976 drivers maintains balanced signaling. Balanced means that the current that flows in each signal line is nearly equal but opposite in direction and is one of the keys to the low-noise performance of a differential bus.

AVAILABLE OPTIONS

T_A	PACKAGE	
	TSSOP (DGG) CMOS INPUT LEVELS	TSSOP (DGG) TTL INPUTS LEVELS
0°C to 70°C	SN75LVDM976DGG SN75LVDM976DGGR†	SN75LVDM977DGG SN75LVDM977DGGR†

† The R suffix designates a taped and reeled package.

description (continued)

The signal symmetry requirements of the LVD-SCSI bus mean you can no longer obtain logical inversion of a signal by simply reversing the differential signal connections. This requires the ability to invert the logic convention through the INV/$\overline{\text{NON}}$ terminal. This input would be a low for SCSI controllers with active-high data and high for active-low data. In either case, the B+ signals of the transceiver must be connected to the SIGNAL+ line of the SCSI bus and the B– of the transceiver to the SIGNAL– line.

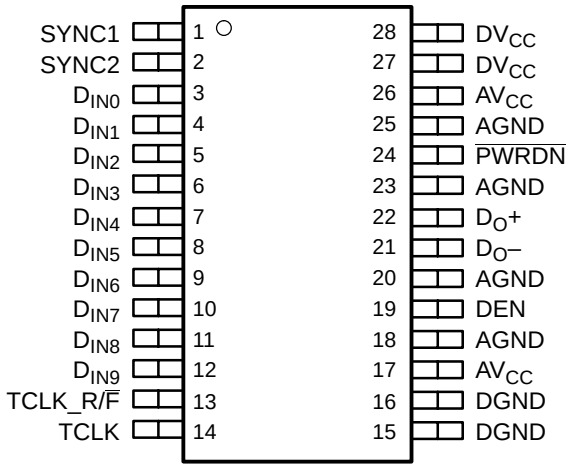
The CDE0 input incorporates a window comparator to detect the status of the DIFFSENS line of a SCSI bus. This line is below 0.5 V, if using single-ended signals, between 1.7 V and 1.9 V if low-voltage differential, and between 2.4 V and 5.5 V if high-voltage differential. The outputs assume the characteristics of single-ended or LVD accordingly or place the outputs into high-impedance, when HVD is detected. This, and the INV/$\overline{\text{NON}}$ input, are the only differences to the trade-standard function of the SN75976A HVD transceiver.

Two options are offered to minimize the signal noise margins on the interface between the communications controller and the transceiver. The SN75LVDM976 has logic input voltage thresholds of about 0.5 V_{CC}. The SN75LVDM977 has a fixed logic input voltage threshold of about 1.5 V. The input voltage threshold should be selected to be near the middle of the output voltage swing of the corresponding driver circuit.

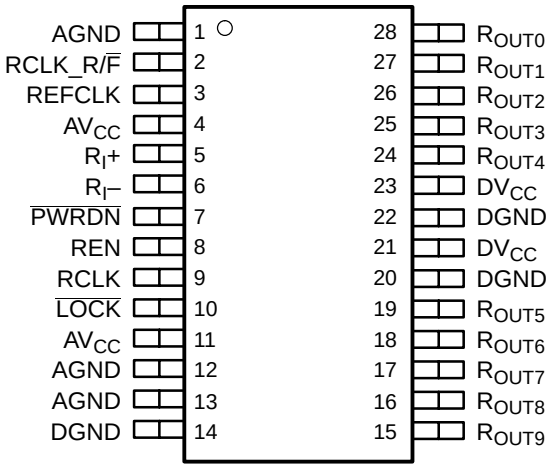
The SN75LVDM976 and SN75LVDM977 are characterized for operation over an free-air temperature range of T_A = 0°C to 70°C.

- **100-Mbps to 400-Mbps Serial LVDS Data Payload Bandwidth at 10-MHz to 40-MHz System Clock**
- **Pin-Compatible Superset of NSM DS92LV1021/DS92LV1212**
- **Chipset (Serializer/Deserializer) Power Consumption <350 mW (Typ) at 40 MHz**
- **Synchronization Mode for Faster Lock**
- **Lock Indicator**
- **No External Components Required for PLL**
- **Low-Cost 28-Pin SSOP Package**
- **Industrial Temperature Qualified, T_A = –40°C to 85°C**
- **Programmable Edge Trigger on Clock (Rising or Falling Edge)**
- **Flow-Through Pinout for Easy PCB Layout**

SN65LV1021
Serializer



SN65LV1212
Deserializer



description

The SN65LV1021 serializer and SN65LV1212 deserializer comprise a 10-bit serdes chipset designed to transmit and receive serial data over LVDS differential backplanes at equivalent parallel word rates from 10 MHz to 40 MHz. Including overhead, this translates into a serial data rate between 120-Mbps and 480-Mbps payload-encoded throughput.

Upon power up, the chipset link can be initialized via a synchronization mode with internally generated SYNC patterns, or the deserializer can be allowed to synchronize to random data. By using the synchronization mode, the deserializer establishes lock within specified, shorter time parameters.

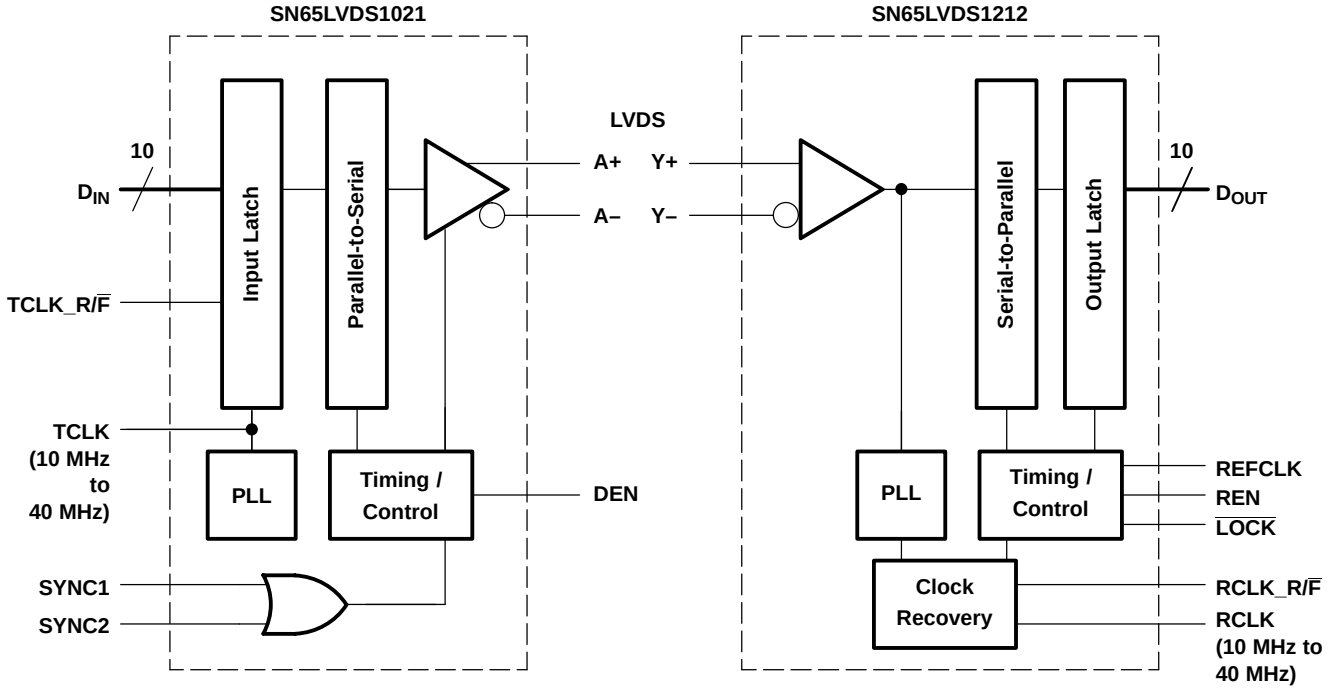
The device can be entered into a power-down state when no data transfer is required. Alternatively, a mode is available to place the output pins in the high-impedance state without losing PLL lock.

The SN65LV1021 and SN65LV1212 are characterized for operation over ambient air temperature of –40°C to 85°C.

ORDERING INFORMATION

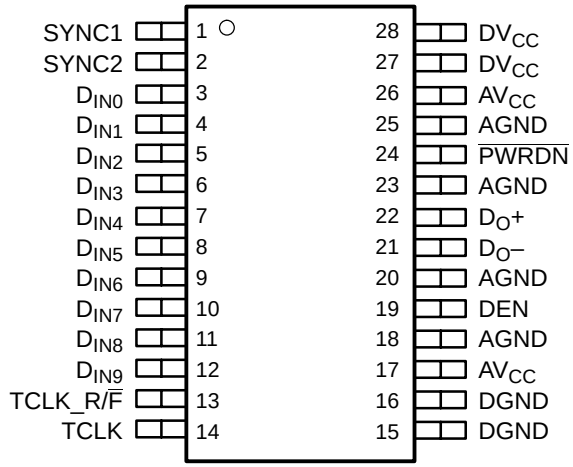
DEVICE	PART NUMBER
Serializer	SN65LV1021DB
Deserializer	SN65LV1212DB

block diagrams

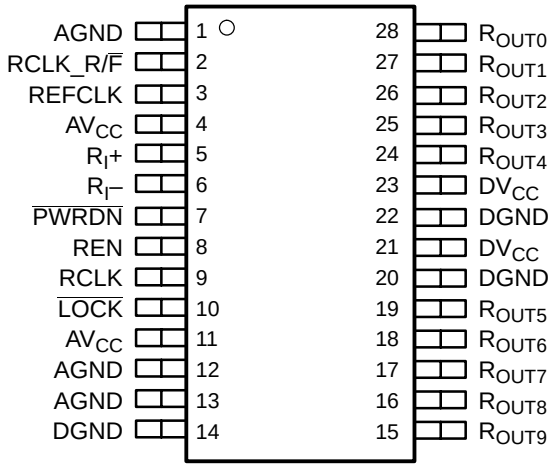


- **300-Mbps to 660-Mbps Serial LVDS Data Payload Bandwidth at 30-MHz to 66-MHz System Clock**
- **Pin-Compatible Superset of NSM DS92LV1023/DS92LV1224**
- **Chipset (Serializer/Deserializer) Power Consumption <450 mW (Typ) at 66 MHz**
- **Synchronization Mode for Faster Lock**
- **Lock Indicator**
- **No External Components Required for PLL**
- **Low-Cost 28-Pin SSOP Package**
- **Industrial Temperature Qualified, T_A = –40°C to 85°C**
- **Programmable Edge Trigger on Clock**
- **Flow-Through Pinout for Easy PCB Layout**

SN65LV1023
Serializer



SN65LV1224
Deserializer



description

The SN65LV1023 serializer and SN65LV1224 deserializer comprise a 10-bit serdes chipset designed to transmit and receive serial data over LVDS differential backplanes at equivalent parallel word rates from 30 MHz to 66 MHz. Including overhead, this translates into a serial data rate between 360-Mbps and 792-Mbps payload encoded throughput.

Upon power up, the chipset link can be initialized via a synchronization mode with internally generated SYNC patterns, or the deserializer can be allowed to synchronize to random data. By using the synchronization mode, the deserializer establishes lock within specified, shorter time parameters.

The device can be entered into a power-down state when no data transfer is required. Alternatively, a mode is available to place the output pins in the high-impedance state without losing PLL lock.

The SN65LV1023 and SN65LV1224 are characterized for operation over ambient air temperature of –40°C to 85°C.

ORDERING INFORMATION

DEVICE	PART NUMBER
Serializer	SN65LV1023DB
Deserializer	SN65LV1224DB

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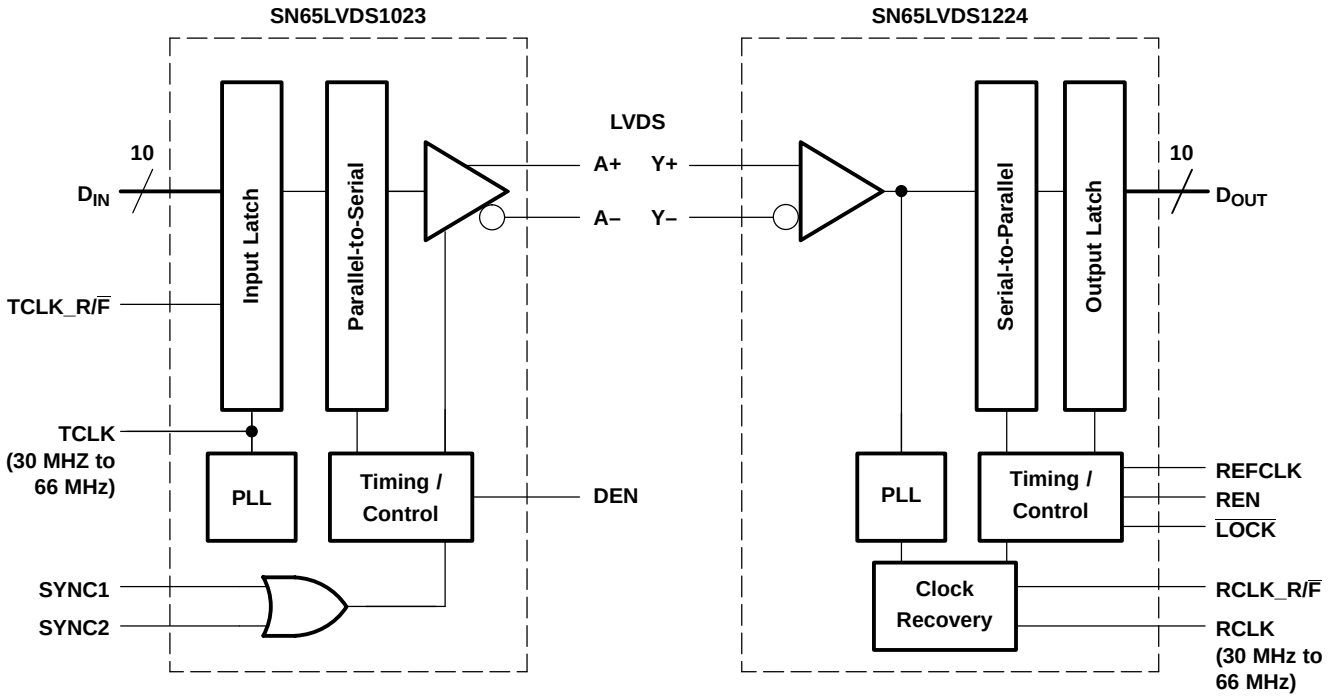
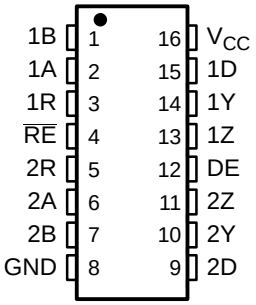
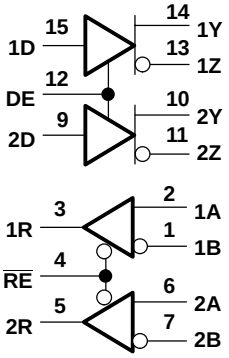
block diagrams



- **Typically Meets or Exceeds ANSI TIA/EIA-644-1995 Standard**
- **Operates From a Single 2.4-V to 3.6-V Supply**
- **Signaling Rates up to 400 Mbit/s**
- **Bus-Terminal ESD Exceeds 12 kV**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 285 mV and a 100 Ω Load**
- **Propagation Delay Times**
  - **Driver: 1.7 ns Typ**
  - **Receiver: 3.7 ns Typ**
- **Power Dissipation at 200 MHz**
  - **Driver: 25 mW Typical**
  - **Receiver: 60 mW Typical**
- **LVTTL Input Levels Are 5 V Tolerant**
- **Driver Is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Receiver Has Open-Circuit Fail Safe**
- **Available in Thin Shink Outline Packaging With 20-mil Lead Pitch**

SN65LVDS1050PW
(Marked as **DL1050** or **LDS1050**)
(TOP VIEW)





DRIVER FUNCTION TABLE

INPUTS		OUTPUTS	
D	**DE**	**Y**	**Z**
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

H = high level, L = low level, Z = high impedance,
X = don't care

description

The SN65LVDS1050 is similar to the SN65LVDS050 except that it is characterized for operation with a lower supply voltage range and packaged in the thin shrink outline package for portable battery-powered applications.

The differential line drivers and receivers use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The drivers provide a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 100-mV signals with up to 1 V of ground potential difference between a transmitter and receiver.

RECEIVER FUNCTION TABLE

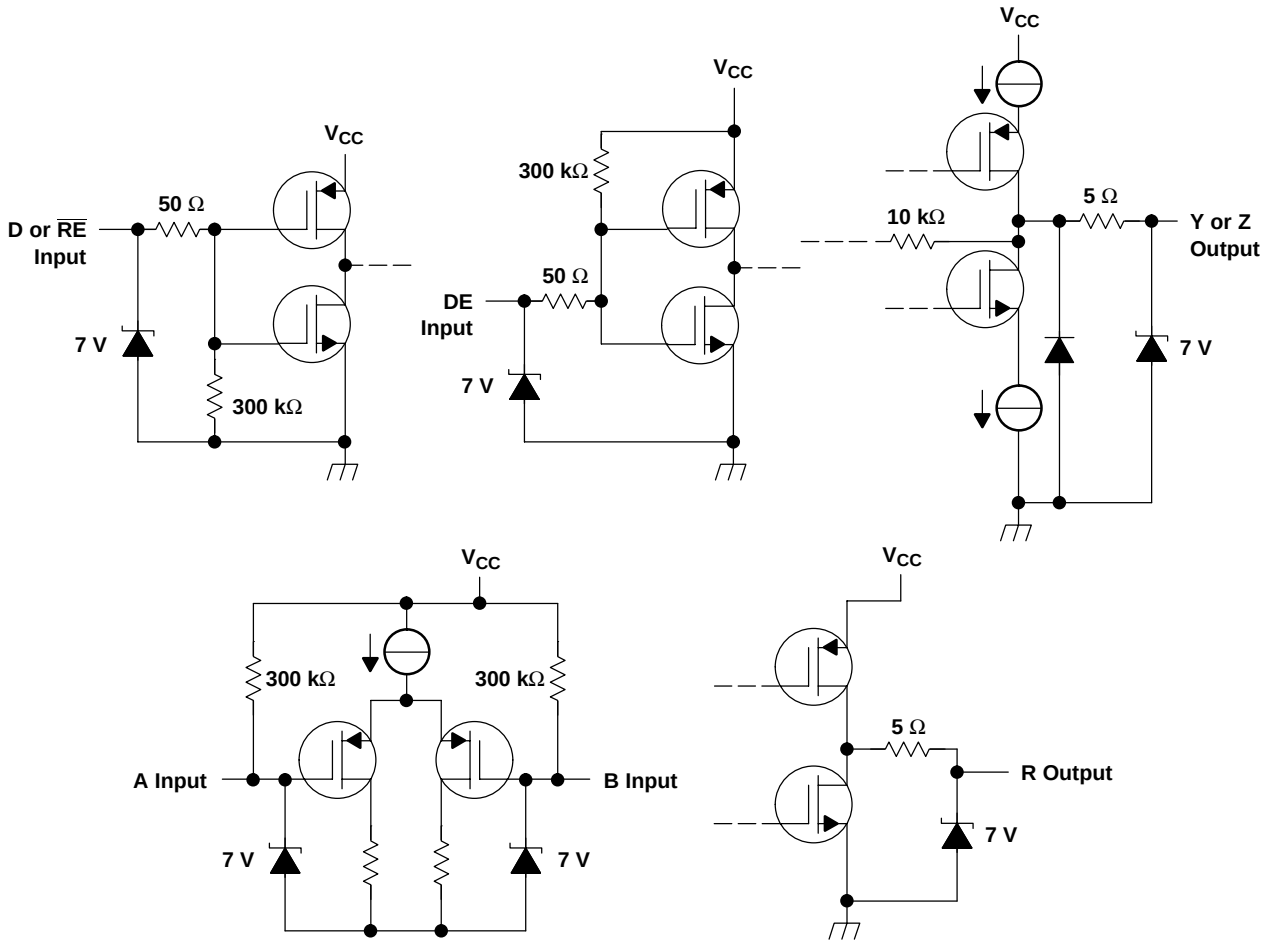
INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	**$\overline{RE}$**	**R**
$V_{ID} \geq 100$ mV	L	H
–100 MV < V_{ID} < 100 mV	L	?
$V_{ID} \leq -100$ mV	L	L
Open	L	H
X	H	Z

H = high level, L = low level, Z = high impedance,
X = don't care

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment and other application-specific characteristics.

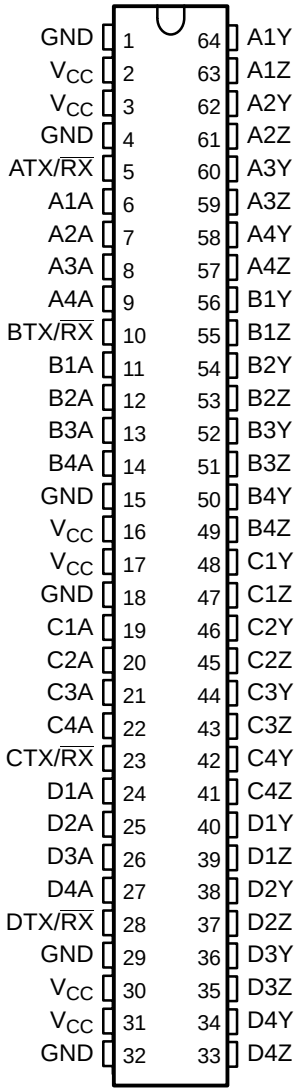
The SN65LVDS1050 is characterized for operation from –40°C to 85°C.

equivalent input and output schematic diagrams



- **Sixteen Low-Voltage Differential Transceivers Designed for Signaling Rates† Up to 630 Mbps**
- **Simplex (Point-to-Point) and Half-Duplex (Multipoint) Interface**
- **Typical Differential Output Voltage of 340 mV Into a 50-Ω Load**
- **Integrated 110-Ω Line Termination on ‘LVDM1677 Product**
- **Propagation Delay Time:**
  - **Driver: 2.5 ns Typ**
  - **Receiver: 3 ns Typ**
- **Recommended Maximum Transfer Rate:**
  - **Driver: 650 M-Transfers/s**
  - **Receiver: 350 M-Transfers/s**
- **Driver is High Impedance When Disabled or With V_{CC} < 1.5 V for Power Up/Down Glitch-Free Performance and Hot-Plugging Events**
- **Bus-Terminal ESD Protection Exceeds 12 kV**
- **Low-Voltage TTL (LVTTL) Logic Input Levels Are 5-V Tolerant**
- **Packaged in Thin Shrink Small-Outline Package With 20 mil Terminal Pitch**

SN65LVDM1676DGG (Marked as LVDM1676)
SN65LVDM1677DGG (Marked as LVDM1677)
(TOP VIEW)



description

The SN65LVDM1676 and SN65LVDM1677 (integrated termination) are sixteen differential line drivers and receivers configured as transceivers that use low-voltage differential signaling (LVDS) to achieve signaling rates in excess of 600 Mbps. These products are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts except that the output current of the drivers are doubled. This modification provides a minimum differential output voltage magnitude of 247 mV into a 50-Ω load and allows double-terminated lines and half-duplex operation. The receivers detect a voltage difference of 100 mV with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of transceivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

description (continued)

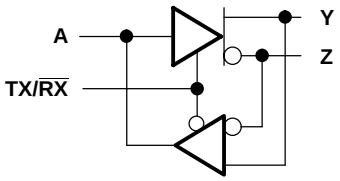
The SN65LVDM1676 and SN65LVDM1677 are characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS		
(Y – Z)	TX/$\overline{RX}$	A	Y	Z	A
$V_{ID} \geq 100$ mV	L	NA	Z	Z	H
–100 mV < V_{ID} < 100 mV	L	NA	Z	Z	?
$V_{ID} \leq$ –100 mV	L	NA	Z	Z	L
Open circuit	L	NA	Z	Z	H
NA	H	L	L	H	Z
NA	H	H	H	L	Z

H = high level, L= low level, Z= high impedance, ? = indeterminate

LVD Transceiver



- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard**
- **Signaling Rates up to 155 Mbps**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 100 Ω Load**
- **LVTTL Input Levels are 5 V Tolerant**
- **Driver is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Receiver has Open-Circuit Fail Safe**
- **Surface-Mount Packaging**
  - **D Package (SOIC)**
- **Characterized For Operation From 0°C to 70°C**

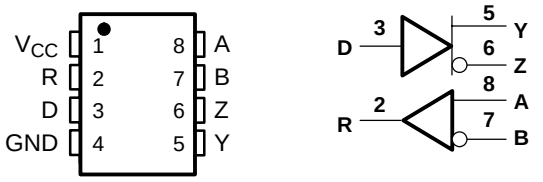
description

The SN75LVDS179, SN75LVDS180, SN75LVDS050, and SN75LVDS051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 155 Mbps. The TIA/EIA-644 standard compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100 Ω load and receipt of 100 mV signals with up to 1 V of ground potential difference between a transmitter and receiver.

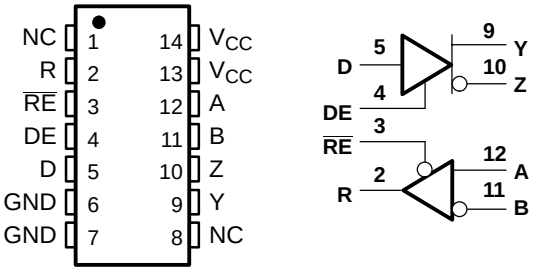
The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The SN75LVDS179, SN75LVDS180, SN75LVDS050, and SN75LVDS051 are characterized for operation from 0°C to 70°C.

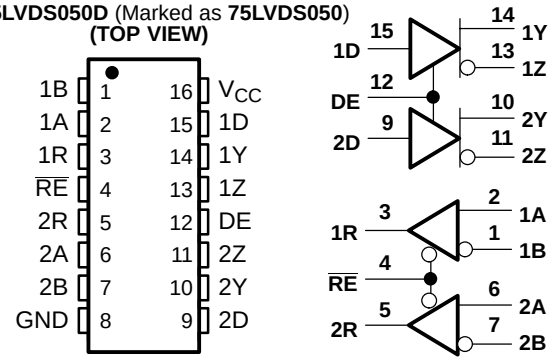
SN75LVDS179D (Marked as **DS179** or **7LS179**)
(TOP VIEW)



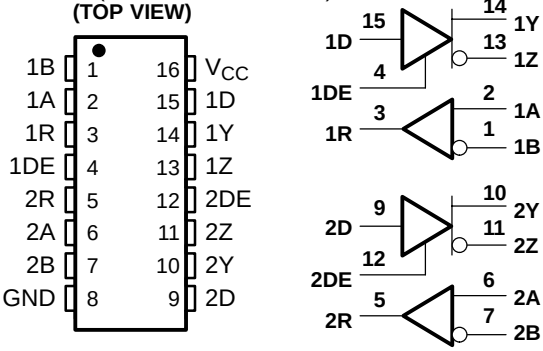
SN75LVDS180D (Marked as **7LVDS180**)
(TOP VIEW)



SN75LVDS050D (Marked as **75LVDS050**)
(TOP VIEW)



SN75LVDS051D (Marked as **75LVDS051**)
(TOP VIEW)



Function Tables

SN75LVDS179 RECEIVER

INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
–100 MV < V_{ID} < 100 mV	?
$V_{ID} \leq -100$ mV	L
Open	H

H = high level, L = low level, ? = indeterminate

SN75LVDS179 DRIVER

INPUT	OUTPUTS	
D	Y	Z
L	L	H
H	H	L
Open	L	H

H = high level, L = low level

SN75LVDS180, SN75LVDS050, and SN75LVDS051 RECEIVER

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 100$ mV	L	H
–100 MV < V_{ID} < 100 mV	L	?
$V_{ID} \leq -100$ mV	L	L
Open	L	H
X	H	Z

H = high level, L = low level, Z = high impedance, X = don't care

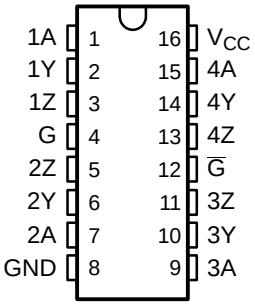
SN75LVDS180, SN75LVDS050, and SN75LVDS051 DRIVER

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

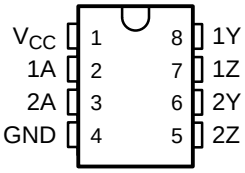
H = high level, L = low level, Z = high impedance, X = don't care

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Signaling Rates up to 155 Mbps**
- **Operates From a Single 3.3-V Supply**
- **Driver at High Impedance When Disabled or With V_{CC} = 0**
- **Low-Voltage TTL (LVTTL) Logic Input Levels**
- **Characterized For Operation From 0°C to 70°C**

SN75LVDS31D (Marked as **75LVDS31**)
SN75LVDS31PW (Marked as **DS31**)
(TOP VIEW)



SN75LVDS9638D (Marked as **DF638** or **7L9638**)
SN75LVDS9638DGK (Marked as **AXK)**
(TOP VIEW)



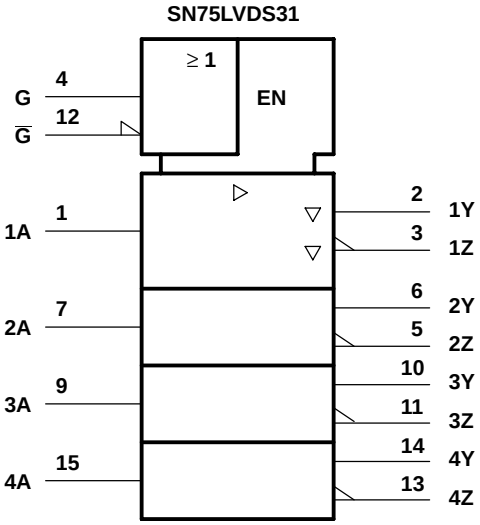
description

The SN75LVDS31 and SN75LVDS9638 are differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

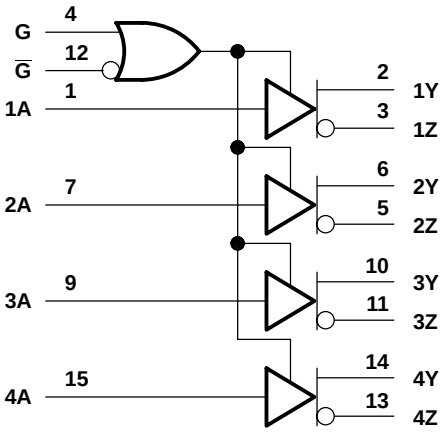
The SN75LVDS31 and SN75LVDS9638 are characterized for operation from 0°C to 70°C.

logic symbol†

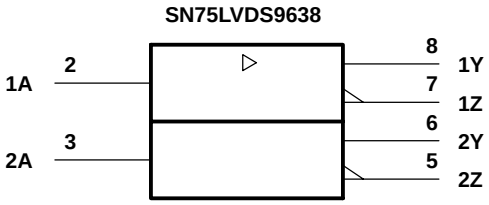


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

’LVDS31 logic diagram (positive logic)

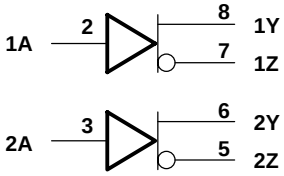


logic symbol†



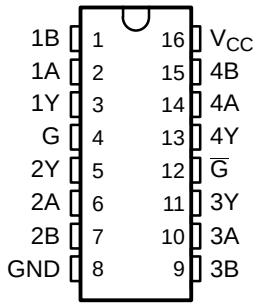
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

’LVDS9638 logic diagram (positive logic)

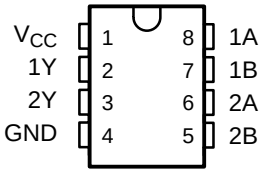


- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard**
- **Operates With a Single 3.3-V Supply**
- **Designed for Signaling Rate of up to 155 Mbps**
- **Differential Input Thresholds ±100 mV Max**
- **Low-Voltage TTL (LVTTL) Logic Output Levels**
- **Open-Circuit Fail Safe**
- **Characterized For Operation From 0°C to 70°C**

SN75LVDS32D (Marked as **75LVDS32**)
SN75LVDS32PW (Marked as **DS32**)
(TOP VIEW)



SN75LVDS9637D (Marked as **DF637** or **7L9637**)
SN75LVDS9637DGK (Marked as **AXI**)
(TOP VIEW)



description

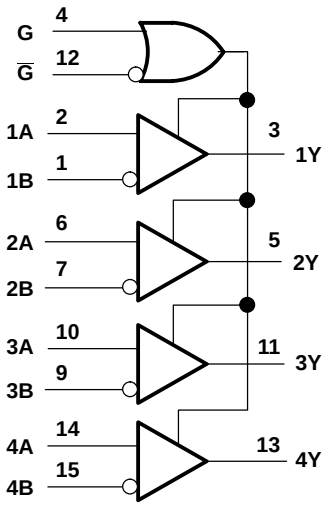
The SN75LVDS32 and SN75LVDS9637 are differential line receivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four differential receivers provides a valid logical output state with a ±100 mV allow operation with a differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

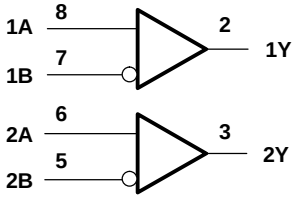
The SN75LVDS32 and SN75LVDS9637 are characterized for operation from 0°C to 70°C.

logic diagram

'LVDS32 logic diagram (positive logic)



'LVDS9637D logic diagram (positive logic)



Function Tables

SN75LVDS32			
DIFFERENTIAL INPUT	**ENABLES**		**OUTPUT**
A, B	**G**	**$\overline{G}$**	**Y**
$V_{ID} \geq 100$ mV	H X	X L	H H
-100 mV $< V_{ID} < 100$ mV	H X	X L	? ?
$V_{ID} \leq -100$ mV	H X	X L	L L
X	L	H	Z
Open	H X	X L	H H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

Chapter 6
Design Guidelines and Tools

This chapter introduces important concepts and design guidelines to help users realize the benefits of LVDS devices. Specifically, It offers advice on PCB design guidelines, bypass capacitors, transmission line termination, connectors, and cables. References are included to provide further guidance where appropriate.

Common Problems

Some of the common problems encountered in PCB design are discussed in the following subsections.

Electromagnetic Interference (EMI)

EMI is a process in which electromagnetic energy generated by one circuit disrupts another. Propagation modes for EMI are mostly through radiation; however, they can occur also through conduction. LVDS circuits generate low EMI due to the low voltage swing used to transmit signals and their differential mode of operation. EMI can occur both with single-ended or differential transmission; however it is mostly a concern when single-ended IOs (TTL/CMOS) are used. Most of these single-ended signals have fast transition times and higher voltage swings, making them more likely to emit radiation and interfere with neighboring circuits. EMI can occur intra- or inter-system. Intra-system interference can cause the equipment not to function as intended. Inter-system interference could create problems with the installation and/or electromagnetic compatibility (EMC) compliance requirements. Control of the interconnection between a driver and receiver can suppress EMI at the source. Controlling EMI at the source via the use of LVDS signaling results in significant improvements in overall system performance.

Crosstalk

One example of intrasystem interference is crosstalk that occurs between conductors that have significant mutual inductance and/or capacitance. LVDS circuits are exposed to crosstalk on the inputs and outputs as well as internally on the IC. Fast switching TTL/CMOS signals used for driver inputs or receiver outputs are the worst sources of crosstalk and must be isolated from sensitive circuits. Isolation is achieved by reducing the coupling between circuits and keeping signal paths as short as possible. The coupling between circuits, defined in terms of the mutual inductance and capacitance, is inversely proportional to the distance between two signal paths. Thus, minimizing crosstalk usually involves increasing the separation between two conductors to decrease the coupling. Table 6–1 explains different types of crosstalk.

Table 6–1. Types of Crosstalk

TYPES OF CROSSTALK	COMMENTS
Single-ended to single-ended	The most prominent case of crosstalk. It is usually minimized by increasing the spacing between two conductors, controlling the slew-rate, or reducing voltage swings.
Single-ended to LVDS	Coupling is mostly common-mode and the receiver rejects it. Differential noise coupling is not zero but is generally small. (Empirical results show values typically less than 50 mV in most layouts)
LVDS to single-ended	LVDS signaling has very little common-mode energy, so this case is rarely a concern.
LVDS to LVDS	Coupling minimized when circuits are well balanced. Since LVDS signaling is differential, uncancelled fringe fields are minimal; hence, this type of crosstalk is rarely a problem.

Ground Bounce

Ground bounce is crosstalk that occurs when there is a shift in the internal ground reference voltage due to output switching. This problem can result in erroneous state switching in ground-referenced (single-ended) gates. Essentially, transients on the ground disturb single-ended inputs that use the ground potential as a reference. During the output high-to-low transition, the sum of the output load current and all switching current through the internal gates of the device flows through the ground lead. The rate of change of this current (di/dt) develops a voltage drop across the ground lead inductance and causes a positive overshoot or ground bounce in an otherwise quiet ground. This positive ground bounce is normally followed by undershoot coincident with the voltage waveform on the output terminal. An output low-to-high transition also generates ground bounce.

The amplitudes of both positive and negative ground bounces are a function of the inductance to ground times the rate of change of current ($L_g \times di/dt$) and of the number of outputs switching simultaneously. As device speed goes up, the rate of change of current in the parasitic inductances increases and the related switching noise goes up. You cannot eliminate ground and V_{CC} bounce, but providing low impedance, low inductance paths from the ground leads of the chip to the PCB ground can minimize their effects. TI recommends connecting each ground pin on a device directly to the PCB ground plane. Tying pins together and connecting them to the ground plane tends to increase inductance to ground and worsen ground bounce problems.

Signal Reflection

Transmission lines are usually modeled using distributed-parameter networks, as opposed to lumping parameters together. When the rise time of the circuit is short relative to the propagation delay of the interconnect, the transmission line should be terminated to implement incident-wave switching and to minimize radiated emissions. LVDS transmission lines should have a nominal impedance of 100 Ω;, however, heavy loading in multidrop and multipoint applications can lower this figure. Ideally, the line termination should match the resulting transmission line impedance. If there is a mismatch, there is an increase in the reflected energy that disrupts the signal quality of the incoming waves and ultimately limits the speed of the link.

Printed-Circuit Board Guidelines

Microstrip vs Stripline Topologies

Today's printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 6–1.

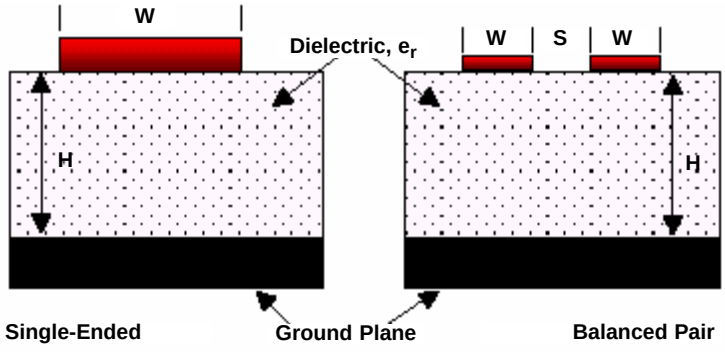


Figure 6–1. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems since the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_0 based on the overall noise budget and reflection allowances. References [1], [2], and [3] provide formulas for Z_0 and t_{PD} for differential and single-ended traces.

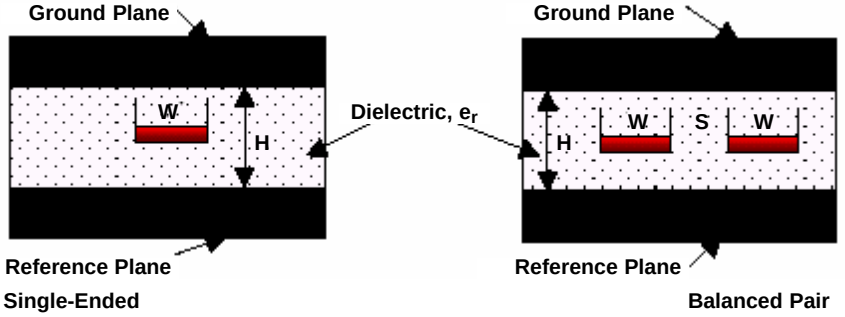


Figure 6–2. Stripline Topology

Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise and fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited.

Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 300 µin (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 6–3.

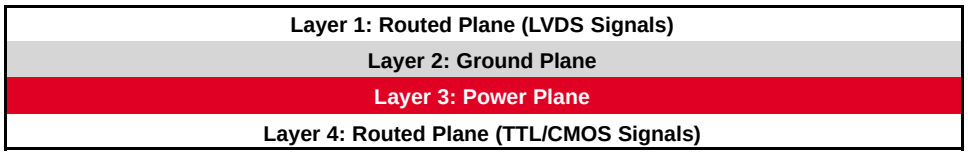


Figure 6–3. Four-Layer PCB Board

NOTE:
The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 6–4.

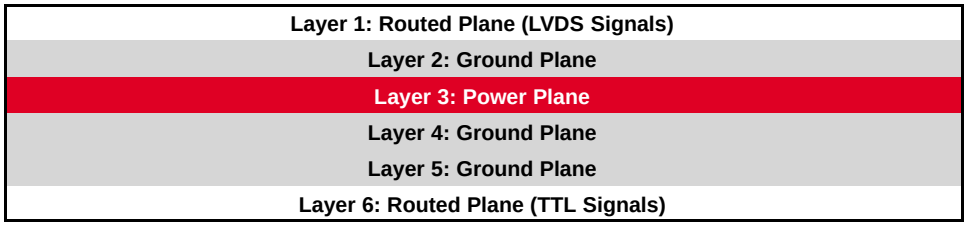


Figure 6–4. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plate. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, since it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broadside coupled.

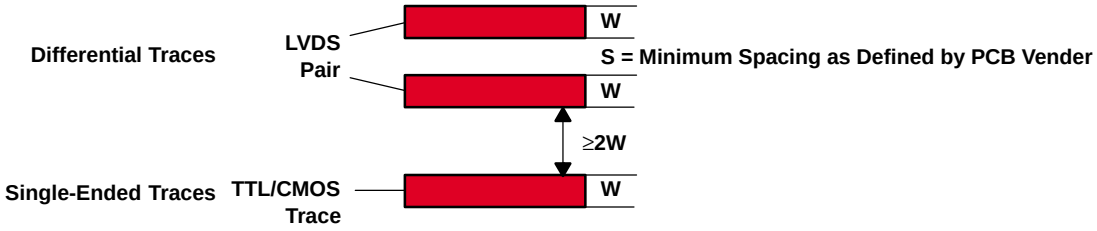


Figure 6–5. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, since they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns in order to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Since the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

Ground Plane Layout Tips

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise/fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 6–6.

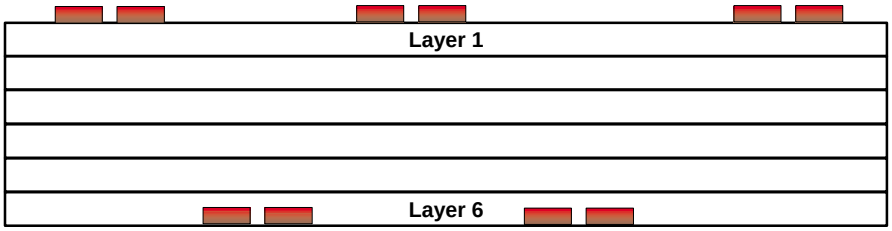


Figure 6–6. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 6–7. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

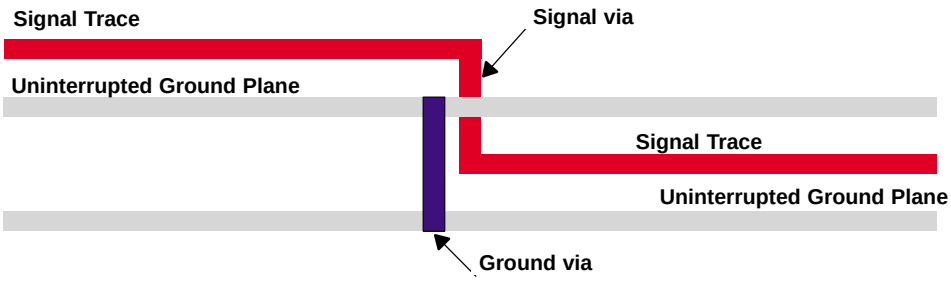


Figure 6–7. Ground Via Location (Side View)

Short and low-impedance connection of the device's ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (e.g., holes, slits, etc.) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

Powering LVDS Devices

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10–1000 μF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one must resort to the use of smaller capacitors (nF to μF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, since their lead inductance is about 1 nH. For comparison purposes, a typical leaded capacitor has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson [1], equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV; however, this figure varies depending on the noise budget available in your design.

$$C_{chip} = \left(\frac{\Delta I_{Maximum\_Step\_Change\_Suppy\_Current}}{\Delta V_{Maximum\_Power\_Suppy\_Noise}} \right) \times T_{Rise\_Time}$$

$$C_{LVDS} = \left(\frac{1A}{0.2\ V} \right) \times 200\ ps = 0.001\ \mu F$$

The following example lowers lead inductance and covers intermediate frequencies between the board level capacitor (>10 μF) and the value of capacitance found above (0.001 μF). You should place the smallest value of capacitance as close as possible to the chip.

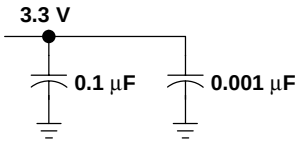


Figure 6–8. Recommended LVDS Bypass Capacitor Layout

Termination Techniques

Two important factors influencing the quality of a termination are the location of the resistor on the line and its value. Transmission lines that are not terminated properly, i.e. impedance matched, can cause reflection, ringing, and crosstalk. To prevent such phenomena, termination is suggested when exceeding one-third (1/3) of the critical length. The critical length is the effective length of a transmission line when the round trip propagation delay of the signal is equal to the rise or fall time. The following equations define critical lengths for striplines and microstrips: $l_c = \frac{ct_r}{2\sqrt{\epsilon_r}}$ for striplines and $l_c = \frac{ct_r}{2\sqrt{0.457\epsilon_r + 0.67}}$ for microstrips (c is the speed of light, t_r is the rise time, ε_r is the dielectric (constant). Thick-film leadless resistors (size 0603 or 0805) reduce stub lengths.

Texas Instruments offers a selection of on-chip terminations in LVDS receivers (LVDT devices). We offer the best termination available since the resistor goes on the chip, as close as possible to the end of the transmission line. Designers should consider LVDT devices for performance and board area considerations. The LVDS standard (TIA/EIA-644A) bounds termination resistor values between 90 Ω and 132 Ω.

Although most designers use LVDS drivers and receivers in point-to-point configurations, other topologies are possible. Here are recommendations for terminating point-to-point, multidrop, and multipoint topologies.

Point-to-Point

This architecture connects the driver directly to one receiver. You should terminate the transmission line at the end of the line opposite to the driver with a 100-Ω resistor tied across the differential inputs of the receiver within one third of the critical length. point-to-point connections offer the highest signal quality of a standard LVDS interface.

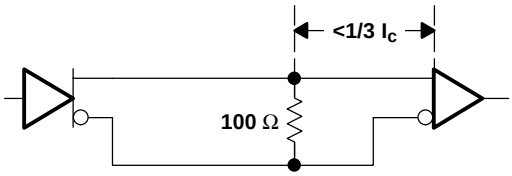


Figure 6–9. Point-to-Point Termination

Multidrop Busses

In the multidrop configuration, a driver is broadcasting data to multiple receivers. As in point-to-point connections, you must place the terminating resistor at the end of the transmission line. You may connect up to 32 TIA/EIA-644-A receivers to the transmission line. If desired, you can use an LVDT receiver at the end of the transmission line and nonterminated LVDS receivers elsewhere on the line. Note that stub lengths exceeding one third of the critical length can become transmission lines and induce impedance mismatch and reflections.

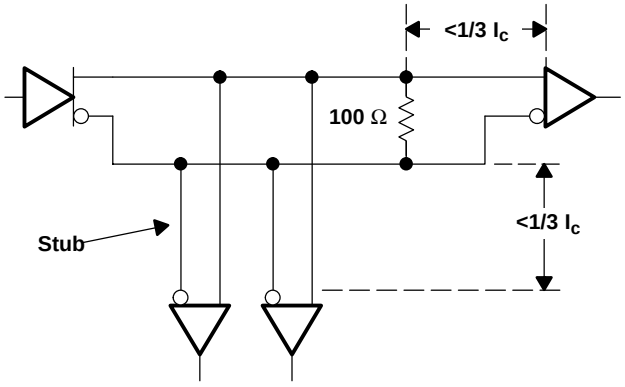


Figure 6–10. Multidrop Termination

Multipoint Termination

Multipoint circuits are those configured in a bus-type solution. Usually, you use transceivers in this circuit configuration, but a combination of drivers, receivers, and transceivers is also possible. Texas Instruments offers LVDM for two node multipoint and M-LVDS for multipoint applications with up to 32 nodes. You place terminating resistors at both ends of the bus, as shown in Figure 6–11. The transceivers should be within one third of a critical length of the bus.

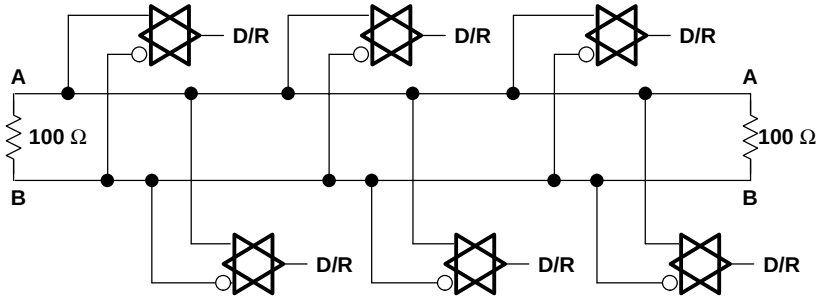


Figure 6–11. Multipoint Bus Termination

Effects of Loading on the Effective Characteristic Impedance

To a good approximation, the characteristic transmission line impedance seen into any cut point in the unloaded multipoint or multidrop bus is defined by $\sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. As capacitance is added to the bus in the form of devices and interconnections, the bus characteristic impedance is lowered. This may result in signal reflections from the impedance mismatch between the unloaded and loaded segments of the bus.

If the number of loads is constant and can be distributed evenly along the line, reflections can be reduced by changing the bus termination resistors to match the loaded characteristic impedance. Normally, the number of loads are not constant or distributed evenly and the reflections resulting from any mismatching must be accounted for in the noise budget.

Effects of Driving Non-Terminated Lines With LVDS

Several LVDS data transmission systems have a cable link between the receiver and driver. In such a system, the possibility exists that a driver could drive an unterminated line when a cable is disconnected. Empirical measurements with the SN65LVDM180 have shown that the effects of nontermination on an active transmission line are minimal. Operation of an unterminated data line does not cause a state change on an adjacent signal pair, indicating no significant increase in noise emissions. In addition, the resulting noise and fault voltage for both active simplex and half-duplex data links reveals that the maximum signal level at the output of an unterminated driver under any condition is equal to the supply rails. These voltages are within the absolute maximum ratings and thus do not damage LVDS devices.

Unused Pins

Leave unused LVDS driver pins open circuited, with the exception of enabling pins. Data sheet equivalent schematics show the operation of input and output pins. If the enable pins are not driven, you can tie them to ground or V_{CC}. Similarly, leave unused pins on the receiver open if not used, with the exception of enable pins. A fail-safe feature that assures a known output state for open inputs is available with some LVDS devices, as discussed in Chapter 3.

Connectors and Cables

It is important to consider the following factors when deciding which connector type to use:

- Impedance matching and conductivity
- Crosstalk
- Shielding
- Skew performance

When using LVDS for data transmission, you should maintain the impedance at any point between the driver and receiver within 90 Ω to 132 Ω. At typical speeds (>100 Mbps), shielded connectors with 100-Ω differential impedance play a key role in preserving signal integrity. The use of shielded connectors helps in reducing EMI. Trace lengths are important among signal pairs because a mismatch causes skew. Teradyne's HSD connectors address this issue by maintaining equal electrical lengths within signal pairs. In addition, shielding minimizes crosstalk. Figure 6–12 shows an example of a configuration that minimizes crosstalk between signal pairs.

S1+	**S1–**	**GND**	**S2+**	**S2–**	**GND**	**S3+**	**S3–**
GND	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
S4+	**S4–**	**GND**	**S5+**	**S5–**	**GND**	**S6+**	**S6–**

Figure 6–12. Connector Configuration Minimizing Crosstalk

Most of the factors discussed above are speed dependent. The following table shows examples of connector types suitable for LVDS applications within a particular speed range.

Table 6–2. LVDS Connector Selector

SPEED	CONNECTOR TYPE	EXAMPLE VENDOR PRODUCT
Low/Medium Trise > 500 ps	Board to board	3M board mounted socket and header
		3M board mounted socket
		Molex modular jack, RJ45
High Trise < 500 ps	Board to board	AMP MICTOR™ and ZPACK™ connectors
		Teradyne HSD™ connectors
		Delphi Gold Dot™ connection system
	Board to cable	Teradyne VHDM-HSD™ connectors with Gore Eye-Opener™ 6 products
		Panduit Giga-Channel™ minijack TX-6™ shielded modular jack
		AMP MICTOR™ connectors
		SMA connectors

The standard governing LVDS devices (TIA/EIA-644A) does not specify the balanced interconnecting media between driver and receiver. Therefore, you may use PCB traces, backplanes, or cables. If you choose cables, we recommended using polyethylene, or Teflon™ insulation in either round or flat cables and uniform distances between the conductors in a signal pair. Belden #9807 is an example of round cable and Belden #9V28010 is an example of flat cable. The twisting of signal pairs is suggested, but not mandatory. In addition, designers should address the following points:

- Design cables for differential transmission.
- Couple each pair of wires representing a signal path to each other, not to ground.
- The attenuation should be as low as possible for a given length.
- The characteristic impedance should be 100 Ω, differential, with allowable variation consistent with signal integrity requirements.

Design Tools

This section presents information on computer simulation models, evaluation modules (EVMs), and other support tools that are available to designers.

Computer Simulation

Accurate circuit models are a critical part of the design process of a high-speed digital system. As clock rates continue to increase, so does the importance of signal integrity (SI) simulation. With existing SI simulation technology, it is possible to simulate large systems with sufficient accuracy to prevent expensive prototypes and design reworks. One of the largest problems still facing SI simulation is the availability of quality device models. SPICE models are the favorite among designers for doing SI simulation but the obstacle with SPICE is largely twofold, 1) very slow run times and 2) contains proprietary information. To get around this headache and still achieve accurate simulations, a new standard has been formed. The industry established the IBIS (I/O Buffer Information Specification) standard (ANSI/EIA-656-A) as a nonproprietary method for providing necessary buffer simulation information.

This section discusses various aspects of IBIS including its history, advantages, input/output (IO) models, model generation flow, validation, and simulation.

IBIS is a fast and accurate behavioral method of modeling input/output buffers based on both VI curve data and transition voltages versus times. This data can be derived in one of two ways: full circuit simulation or measurement. It uses a standardized software-parsable format to create the behavioral information required to model analog characteristics of integrated circuits (ICs). Regardless of the source, the model must pass the parser test to ensure, syntactically, that the model meets the IBIS specification. It is worth noting that behavioral models mimic the behavior of a circuit rather than the behavior of individual transistors. Most analog simulators or electronic design automation (EDA) tool vendors support the IBIS standard today.

The originator of IBIS was Intel Corporation. Today, the IBIS forum drives the evolving standard with over 35 members consisting of EDA vendors, computer manufacturers, semiconductor vendors, and universities. The committee is continually refining the IBIS specifications. With the advances in technology, the standard adds various characteristics of the IO buffer behaviors.

The most important advantage the IBIS model offers is protection of proprietary information about the modeled circuit. The IBIS model provides pertinent information needed for SI simulation without disclosing process or circuit design information. IBIS models are accurate and account for the nonlinear aspects of IO structures in the model parameters.

Since IBIS is behavioral, the simulation time for an IBIS model can run upwards of 25 times faster than a structural model (SPICE). IBIS does not have the nonconvergence issues associated with SPICE. Due to the strong support from the various EDA vendors, IBIS can run on practically any EDA tool industry-wide. One of the most popular uses of IBIS is for signal integrity analysis on system boards.

Figure 6–13 is a behavioral block diagram of IBIS with the pieces required to create an Input and Output Model.

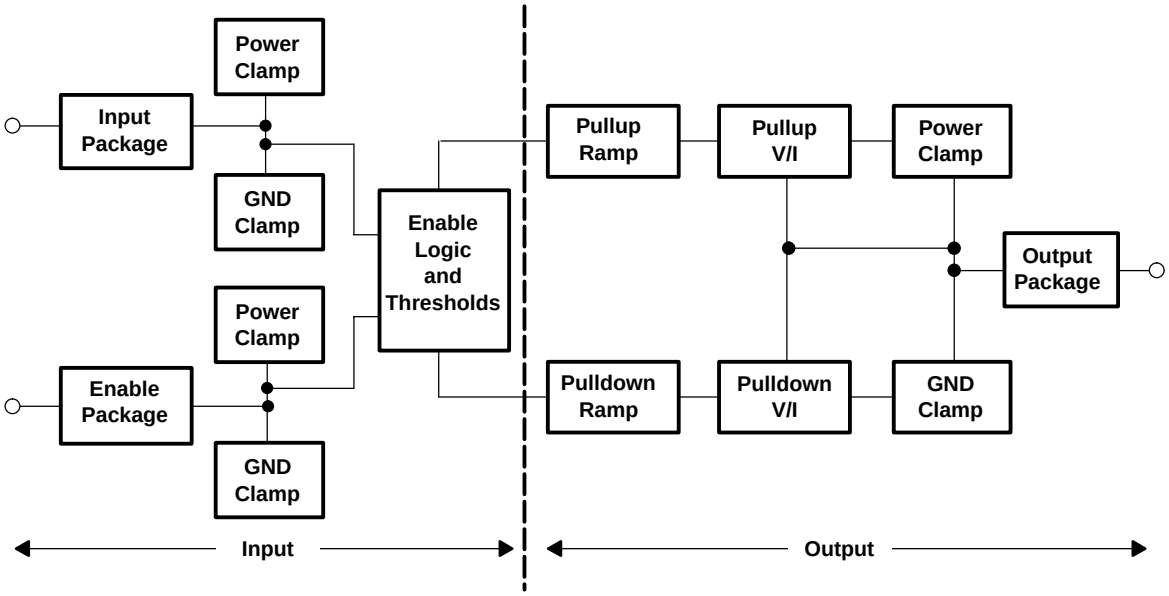


Figure 6–13. Input/Output Behavioral Model

Block 1 of Figure 6–14 and Figure 6–15 represents the pad and package parasitics seen by the buffer. C_comp is the total capacitance due to the pad, clamp diodes, and IO transistors. L_pkg, R_pkg, and C_pkg are the inductance, resistance, and capacitance of the bond wire and pin combination of the package. Pin-specific package parameter nomenclatures are L_pin, R_pin and C_pin.

Block 2 consists of steady-state VI tables representing the ESD or clamping diodes. These diodes can help clamp transmission line reflections. Blocks 3 and 4 show output transistors that are also modeled by steady-state VI curves. These curves describe the voltage vs. current performance of a given output structure at high, low, and high-impedance states. The curves define the voltage and current relationship of the device through the extended operating range. This can be tricky because it is necessary to measure the device beyond the normal operating range in order to determine the effects of overshoot protection diodes—an important effect in SI simulation.

Block 5 represents the transition time of the output as it switches from one logic state to the other. Rise and fall times are represented a couple of ways, either through ratios of transition voltage to times: dV/dt or the more preferred method of the actual data through a table of transition voltage versus time.

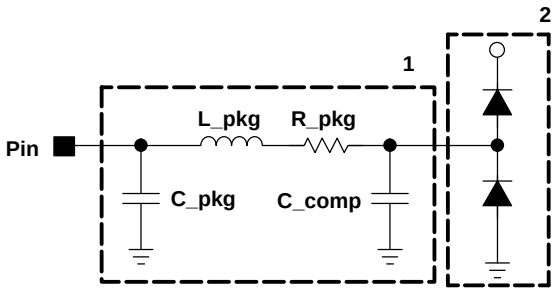


Figure 6–14. Input/Enable Model

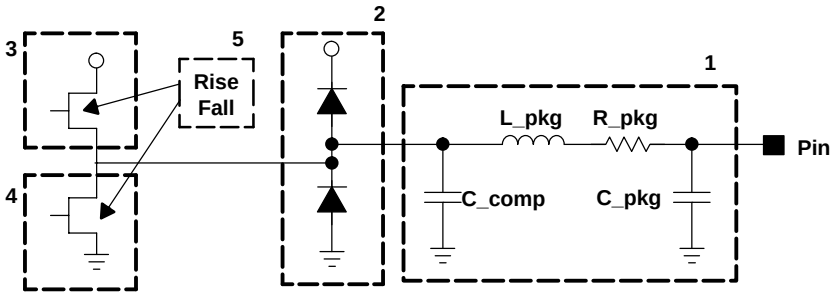


Figure 6–15. Output Model

The following are the steps used in generating an IBIS model.

1. All required data needs to be collected through simulation or measured on the bench.
2. Once the data is collected, we generate an IBIS ASCII file following the format defined in the IBIS standard.
3. To verify that the model is IBIS compliant, it is then checked using the *Golden Parser*. This software-parser validates the ASCII model file for syntax and confirms the data format meets the IBIS specification.
4. Once we correct all syntax errors, the model is imported into a simulator and validated for accuracy.

Data with abrupt discontinuities is suspicious and, even if it is valid, probably will not simulate correctly. One alternative is to truncate the data at the discontinuity. Most behavioral simulators linearly extrapolate the data points based on the last two data points. Therefore, we still assure reasonable simulation with truncated data.

Check the model for any regions that could have nonmonotonic data. Nonmonotonic refers to a negative resistance region. While not inherent in LVDS circuits, this can occur (other circuit designs) in the clamp region where the pull-up current is swamped by the power clamp, leaving a net positive resistance. In those rare cases where we find a non-monotonicity in the active area of operation, convergence could be a problem resulting in oscillations under certain loading.

IBIS gives some latitude when it comes to setting up the loads for rise and fall times. Some of the loads capture actual simulation characteristics, but the data itself does not yield a model that gives a good simulation. As a rule, capacitive and inductive loads and fixture package parameters should be avoided. Additionally, to avoid warnings, IBIS requires the beginning and ending values of waveforms to converge to their final values.

Once we review the model thoroughly and make any corrections, it is ready for the model review committee. The committee is comprised of various EDA vendors who review the model and provide helpful feedback.

TI Data Transmission generates IBIS models and uses Innoveda's LineSim simulator for model validation. LineSim can simulate a system board by using different transmission elements with different characteristics and connecting them together. These transmission elements can be microstrip, buried microstrip, stripline, or cables, just to name a few. The transmission line chosen in Figure 6–16 is Innoveda's microstrip.

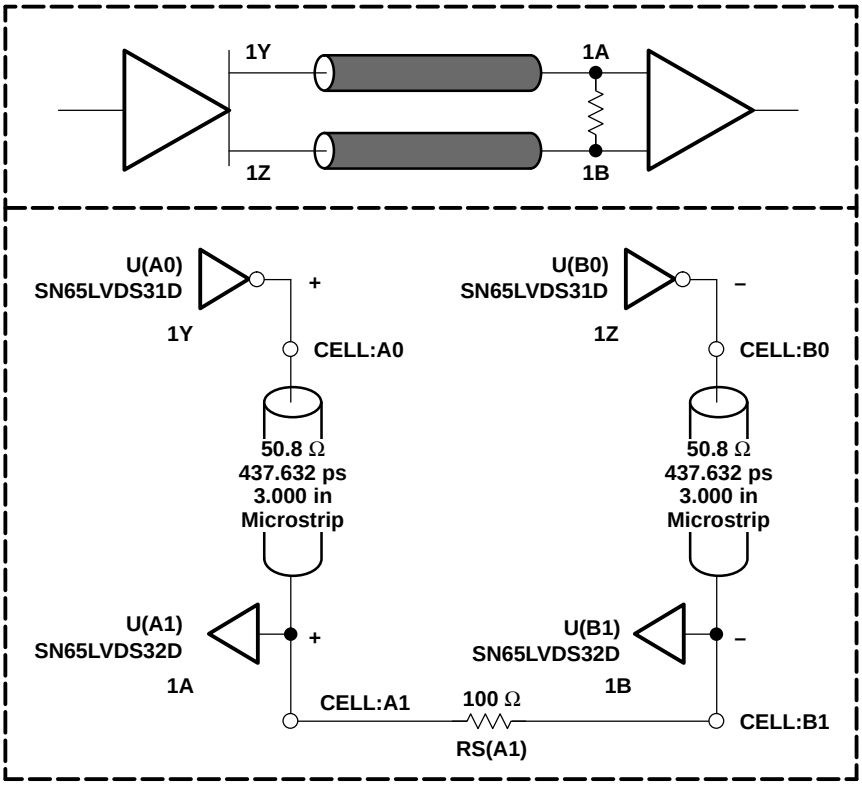


Figure 6–16. Schematic Drawing and Schematic Editor of LineSim

In the example, we are using TI's low voltage differential signaling (LVDS) SN65LVDS31 differential driver driving a balanced transmission line and terminating with a 100-Ω resistor across the inputs of the SN65LVDS32 receiver. The example has both the schematic drawing and schematic editor as shown by LineSim.

The waveforms shown in Figure 6–17 are the differential output of the SN65LVDS31 driver (solid line) and the differential input to the SN65LVDS32 (dashed line) receiver using the IBIS model. The stimulus is a 200-MHz oscillator driving the input to the SN65LVDS31. The scope picture shows a nice controlled differential output with minimal reflection when properly terminated.

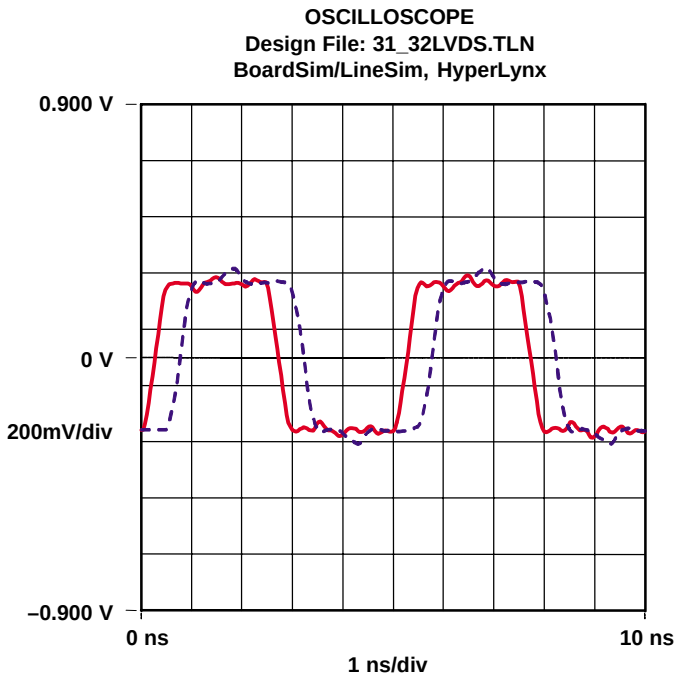


Figure 6–17. Differential Output Simulation With a Termination of 100 Ω

In the scope picture shown in Figure 6–18, we used the same transmission line properties with a mismatched termination resistor of 60 Ω. The impedance of the media is 100 Ω so this should demonstrate a negative reflection, as it does.

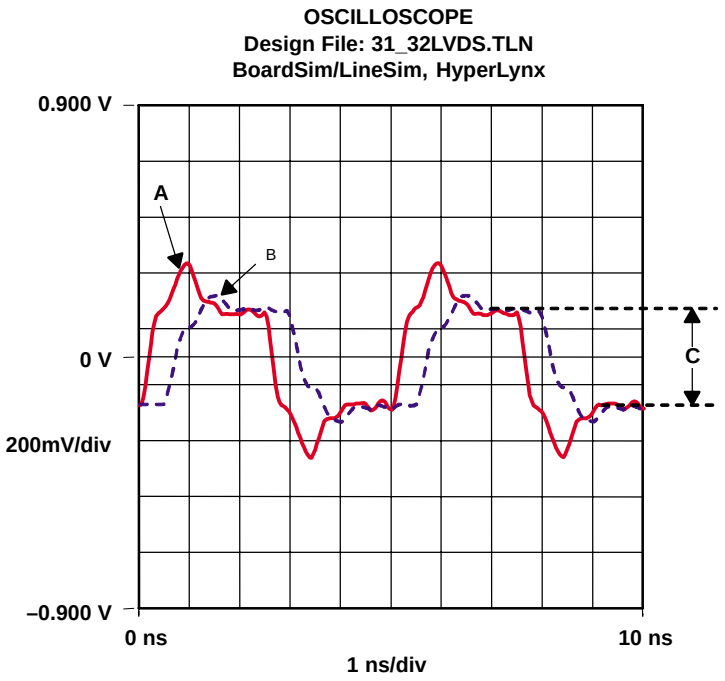


Figure 6–18. Differential Output Simulation With a Mismatched Termination of 60 Ω

The source (solid line) has an inflection at one τ (delay of the line, 0.438 ns) and hits its peak and overshoot at 2 τ (point A on the graph). The receiver (dashed line) mirrors this behavior delayed by τ and is reduced in amplitude (point B). The impedance mismatch reflects energy back to the source thus lowering the overall differential signal present at the receiver's input. On the properly terminated transmission line (Figure 6–17), the power transfer is optimized providing maximum transfer of signal. In the second case, the lower termination value reduces the final differential signal roughly by one-half (point C).

TI offers IBIS models for nearly all LVDS products with the goal to provide good accurate models to designers. TI is an active participant in the IBIS forum meetings, helping guide future enhancements to provide a better comprehensive standard.

The IBIS community provides various kinds of free tools from its website (http://www.eigroup.org/ibis/ibis.htm):

- s2ibis2: This shareware from North Carolina State University (NCSU) translates SPICE models to IBIS. Various commercial and noncommercial SPICE engines are supported.
- S2iplt: This is another utility provided with the s2ibis2 tool from NCSU. This Perl script uses GNUplot to graphically plot the V/I and V/t table.
- Visual IBIS Editor: HyperLynx (Innoveda) provides a shareware that can help develop and test IBIS models on a PC platform. Graphical viewer, parser test and other functions are available
- spi_tran: Cadence provides this shareware which is a Java based GUI for easy input of all the SPICE-to-IBIS parameters required for s2ibis2 translation.
- Parser: The IBIS parser (ibischk3) is available for free download from the IBIS website and supports multiple operating systems and computing platforms
- IBIS Cookbook: Detailed descriptions of IBIS model development with all sorts of tips.
- Model Review Committee: A committee comprising of various EDA vendors can review IBIS models and provide confidential feedback to developers. This support is free and available only to model developers.

- IBIS2SPICE: Intusoft provides a shareware that can take an IBIS model and translate it back to SPICE.
- IBIS Librarian: The official EIA IBIS Librarian can create a link to the IBIS model's website from the EIA IBIS web page.

IBIS modeling is an accurate and useful tool for signal integrity simulation. The formation of IBIS (ANSI/EIA-656-A) has been a great vehicle to get around the bottleneck of proprietary information contained within SPICE models and the long simulation run times that go with them. TI is making a very strong effort in supplying IBIS models for many products. The overall goal is to provide a good modeling tool so designers can run their simulations with confidence.

EVMs

Evaluation modules or EVMs have become very popular because they allow a designer to evaluate interface designs or device performance and catch simple mistakes before building a prototype. Knowing the design will work is a big benefit, but not the only one. EVMs come with a detailed manual, which contains not only electrical schematics but also, in most cases, detailed layout and trace routing information that an engineer can use as design guidelines.

TI currently offers eleven EVMs designed for evaluation of the electrical characteristics of LVDS, LVDM, and M-LVDS products. Each EVM contains a representative device of a family of devices. The EVM user can verify data sheet parameters, evaluate the interoperability of driver and receivers, and analyze unique system performance. Table 6–3 lists the EVMs currently available.

Table 6–3. LVD EVMs

TOOL NAME	PART NUMBER	GENERATION	RELATED DEVICES
100–400 MHz, 10-bit LVDS serializer/deserializer EVM	SN65LV1021EVM	Low speed LVDS SERDES (<85 MHz)	SN65LV1021
300–660 MHz, 10-bit LVDS serializer/deserializer EVM	SN65LV1023EVM	Low speed LVDS SERDES (<85 MHz)	SN65LV1023
MuxIt-EVM evaluation module	MUXIT-EVM	Low speed LVDS SERDES (<85 MHz)	SN65LVDS150, SN65LVDS151, SN65LVDS152
NLK48EVM KIT-MSDS	NLK48EVM	Low speed LVDS SERDES (<85 MHz)	SN65LVDS96, SN65LVDS95
16-channel LVDS driver evaluation module	SN65LVDS387EVM	LVDS	SN65LVDS387, SN65LVDS389
16-channel LVDS receiver evaluation module	SN65LVDS386EVM	LVDS	SN65LVDS386, SN65LVDS388A
Evaluation module for SN65LVDS31 and SN65LVDS33	SN65LVDS31-33EVM	LVDS	SN65LVDS31, SN65LVDS33
M-LVDS evaluation module	MLVD20XEVM	LVDS	SN65MLVD200, SN65MLVD201, SN65MLVD202, SN65MLVD203, SN65MLVD204, SN65MLVD205
SN65LVDM31-32BEVM evaluation module	SN65LVDM31-32BEVM	LVDS	SN65LVDM31, SN65LVDS32B
SN65LVDS31-32BEVM evaluation module for LVDS31 and LVDS32B	SN65LVDS31-32BEVM	LVDS	SN65LVDS31, SN65LVDS32B
SN65LVDS31-32EVM evaluation module for LVDS31 and LVDS32	SN65LVDS31-32EVM	LVDS	SN65LVDS31, SN65LVDS32

The list of available EVMs is always growing. To keep pace with new products and features, check www.ti.com/evms for the most complete and up-to-date information. To order any of the EVM kits listed here, please call our toll free order desk at 1-800-477-8924, ext. 5800 in North America. To order in Europe, Asia, and other regions contact the TI Product Information Center or contact your local TI distributor.

Other Design Help

- www.ti.com—data sheets, application notes, reference designs, EVM manuals, TI's Analog Applications Journal, and Knowledge Base (a natural language search engine to point to answers to frequently asked questions).

- TI's Product Information Center (PIC)—Technical assistance is available by contacting at 1-972-644-5580, or by email at http://www–k.ext.ti.com/sc/technical_support/email_tech_support.asp?AAP
- Product samples—Available free from TI in quantities less than 10. To order LVDS samples, simply complete your device search at www.ti.com by landing in a device product folder, select the *Check Stock or Order* link under the column labeled *Availability/Samples* and submit all required information. TI processes sample requests immediately upon receipt, and usually deliver (U.S.) within 48 hours. Overseas delivery usually takes 10 days. You may also contact your local sales office or authorized TI distributor to place an order.
- Purchase small quantities—Less than 40 units for preproduction verification. DigiKey provides this service (1-800-344-4539).
- **Field Sales**—You may obtain sales support by contacting any of the TI field sales offices or local distributor. This Handbook lists TI's field sales offices at the back. You can find distributors for TI products through the TI home page by entering the TI device part number and clicking on *search*, or by visiting www.ti.com/sc/docs/general/distr.htm for distributor listings.

Conclusion

Successful designs of LVDS circuits start with good planning of power and noise budgets, careful signal layout, adequate power supplies, proper transmission line termination, and connectors and cables that preserve signal integrity. Designing LVDS parts with the guidelines presented in this chapter is very rewarding in the quality and robustness of the design.

References

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5. Texas Instruments, The Bypass Capacitor in High-Speed Environments, literature number SCBA007A.
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7. Texas Instruments, Interface Circuits for TIA/EIA-644A (LVDS) Design Notes, literature number SLLA038A.
8. Texas Instruments, Performance of LVDS with Different Cables, literature number SLLA053.
9. Texas Instruments, Powering an LVDS Com-Link in a 5-V System, literature number SLLA059.
10. Texas Instruments, Terminating LVDS transmission, literature number SLLA066.
11. Texas Instruments, Driving Unterminated Lines with LVDM, literature number SLLA074.
12. Texas Instruments, Transmission at 200 Mbps in VME Card Cage Using LVDM, literature number SLLA088.
13. Texas Instruments, PCB Design Guidelines For Reduced EMI, literature number SZZA009.

Chapter 7
Testing Guidelines

Introduction

The LVDS design techniques, discussed in Chapter 6, maximize signal integrity and system performance. Some testing is necessary in order to validate these good design practices. Different tests utilize different metrics as a standard or reference to measure against. These metrics can be either industry standards or application specific system requirements. These requirements dictate the types of measurements needed and consequently the type of test equipment required.

Test equipment and peripheral devices impact system evaluation and should not be neglected. Proper use of test equipment should lead to measurements that have a high degree of confidence. From these measurements, the designer can further investigate (troubleshoot) if test results are not as expected.

Requirements such as percent jitter, an eye mask, or bit error rate (BER), all specify the signal quality of the device and system under test (DUT) outputs for a particular signaling rate at the inputs. In addition to signal quality, LVDS systems have to comply with electromagnetic interference (EMI) requirements. Although not a measure of performance, EMI can affect other systems and therefore the overall product.

Using the Eye Pattern

The eye pattern is a useful tool to measure the overall signal quality at the end of a transmission line. It includes all of the effects of systemic and random distortion, and shows the time during which the signal may be considered valid. Figure 7–1 illustrates the significant attributes of the eye pattern.

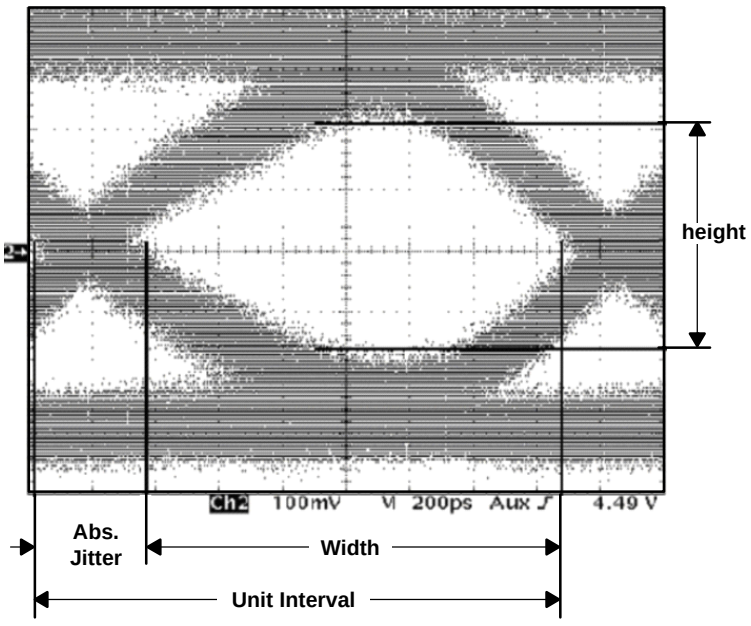

Figure 7–1. Typical Eye Pattern

Evaluators use eye patterns for both jitter measurements and eye mask criteria. The example eye pattern, shown in Figure 7–1, consists of several superimposed transitions. Figure 7–2 shows how the combination of several transitions can make an eye pattern.

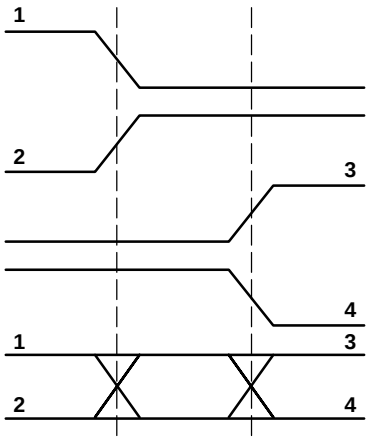

Figure 7–2. Sample Components of Eye Pattern

In order to generate an eye pattern, the signal source must provide the different transitions. A pseudorandom bit sequence (PRBS) can provide the transitions needed to generate an eye pattern. In order to display the eye pattern, the observation device needs to be in a mode which displays several transitions. The eye pattern in Figure 7–1 used the digital phosphorus mode of the Tektronix TDS784D digitizing oscilloscope. Another important part of displaying eye patterns is the triggering. A clock or external trigger from the source needs to provide the horizontal trigger to the oscilloscope rather than the data pattern. Triggering the scope from the displayed pattern removes one of the transitions from the eye pattern. For example, triggering on the falling edge removes the rising edge of the eye pattern at the trigger.

Jitter Measurements

Although several standard definitions clearly describe various skews and jitters, no single definition can clarify the origins and contents of jitter in a measurement. The JEDEC Standard No. 65 (EIA/JESD65) defines skew as the magnitude of the time difference between two events that ideally would occur simultaneously, and explains jitter as the time deviation of a controlled edge from its nominal position. IEEE and the International Telecommunications Union reinforce this time variation definition with similar discussions. Jitter can best be defined as the total sum of skews, reflections, pattern-dependant interference, propagation delays, and coupled noises that degrade signal quality. It represents the portion of the unit interval (UI) in Figure 7–1 during which a receiver cannot determine a logic state.

Jitter is typically measured at the differential voltage zero crossing during the logic state transition of a signal. Note that jitter present at the nonzero receiver threshold voltage measures the worst-case jitter of the signal, and most consider it a more conservative representation of the jitter applied to the input of a receiver. The jitter may be given either as an absolute number or as a percentage of the unit interval (UI). This UI or bit duration equals the reciprocal value of the signaling rate, and the time during which a logic state is valid is just the UI minus the jitter. Percent jitter (the jitter time divided by the UI times l00) is more commonly used and it represents the portion of UI during which the logic state is indeterminate. A percent jitter of 25% or less is acceptable in most systems that do not provide any type of data recovery or equalization.

Users can use the cursor functions of most oscilloscopes to determine the jitter and the UI of an eye pattern. An example of using the display cursors of an oscilloscope to measure percent jitter is available in application report SLLA064, *Measuring Crosstalk in LVDS Systems*. In addition, some scopes provide histogram measurements, indicating the distribution of the jitter in an eye pattern. Some histogram measurements provide standard deviation and peak-to-peak jitter information based on the total jitter, which is statistically inaccurate (*A New Method for Jitter Decomposition Through Its Distribution Tail Fitting*; Li, Wilstrup, Jessen, and Petrich; Wavecrest Corp.). Software upgrades to oscilloscope are available that specifically measure jitter and provide more information beyond that of the histogram measurements. An example of this software is the TDSJIT1 software from Tektronix. More advanced measurements with Wavecrest Software (VISI™ 6.0) separate the deterministic and random jitter components. The separation of deterministic and random jitter allows proper allocation of standard deviation to the unbounded random components and the peak-to-peak value to the bounded deterministic components. This separation also can provide greater insight into the causes of the observed jitter. Jitter can be measured manually in a relatively simple way, or it can be automated by software and become a very detailed and complex measurement of signal integrity.

Eye Mask

An eye mask defines the acceptable region or zone about an anticipated eye pattern. The eye mask can take on many shapes and is not limited to the hexagon shape of the example in Figure 7–3. Signal excursions into the masked area are potential errors. One advantage of an eye mask over a percent jitter measurement is that the eye mask is a requirement placed upon the whole eye pattern and not just the width at the zero differential voltage crossing. The eye mask also accounts for signal overshoot and undershoot.

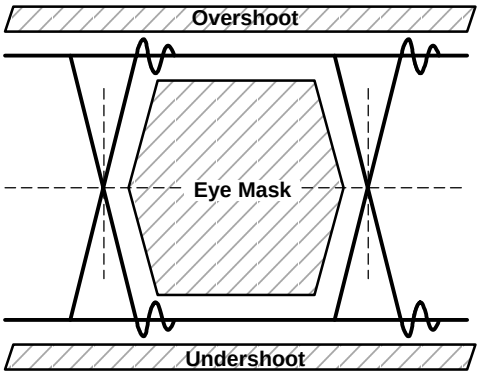

Figure 7–3. Eye Mask

The eye mask is common and, like the jitter measurements, often realized with an oscilloscope. The eye mask requires more equipment preparation than a percent jitter measurement; however, specific eye mask software is available to automate the measurements. An example of eye mask software is the WaveStar™ software family from Tektronix.

Test equipment can influence both the percent jitter and eye mask measurements. The sampling rate of the digital sampling scopes used to observe the eye pattern limit both. The scope can miss large transients that happen infrequently and not at the same time of the scope sample. In the case of an eye mask, this would prevent error detection, and in the case of percent jitter, it would prevent an accurate measurement. The bandwidth of the oscilloscope and the probes can also limit measurement accuracy. Faster signal rise times require more bandwidth to see the signal. If the scope is blind to the high frequency components of the signal due to a lack of bandwidth, then the displayed signal has a larger rise time than the actual signal. The increase in the 10% to 90% rise time can be calculated using equation 1 given the 3-dB bandwidth. If the bandwidth is given in RMS values, equation 2 calculates the increase in rise time. This increase in rise time is a combination of the bandwidth limitations of the probe, the oscilloscope, and the actual rise time of the signal. The combination is the square root of the sum of the squares, as shown in equation 3.

VISI is a trademark of Wavecrest Corporation
WaveStar is a trademark of Tektronix, Inc.

$$T_{10–90} = \frac{0.338}{F_{3\ dB}} \quad (1)$$

$$T_{10–90} = \frac{0.361}{F_{RMS}} \quad (2)$$

$$T_{displayed} = \sqrt{\left(T_{Rscope}{}^{2} + T_{Rprobe}{}^{2} + T_{Rsignal}{}^{2}\right)} \quad (3)$$

Equations 1, 2, and 3 are taken from *High-Speed Digital Design, A Handbook of Black Magic* by H. Johnson and M. Graham. The approximations of equations 1 and 2 assume a Gaussian frequency response.

The signal generator is also an important part of evaluating signal integrity for two reasons. First, the signal generator has some amount of jitter and eye mask criteria may be impossible to meet if the signal source already violates the mask. In the case of a percent jitter measurement, subtract the known peak-to-peak jitter from the signal source from the total to determine the jitter induced by the DUT (approximated by truncating the shape of the jitter to the peak-to-peak values and then applying the width property of the convolution of two waveforms). Second, the signal quality in a system is data dependent. TI calls this dependence intersymbol interference (ISI). ISI is a leading cause of signal degradation. Typically referred to as pattern dependant skew, these one-to-zero and zero-to-one voltage attenuation and propagation delays are only one of the several jitter sources associated with a circuit component's frequency-dependant impedance. These differing patterns present varied frequency components that attenuate differently and propagate at different speeds, creating signal dispersion. Line resistance, capacitance (mutual and ground), conductance, and inductance (series and mutual) interplay with a signal and adjacent signals at different frequencies depending on matters like slew rate, electrical environment, board layout, board composition, and connector and cable quality. Balanced transmissions like clock signals or data with balanced coding (like 8b10b) usually suffer less from ISI than random sequences that contain long sequences of 1s and 0s. Most use PRBS that contain nearly all possible sequences and the resulting ISI for transmission line measurements. This ensures performance under worst-case conditions and may not be applicable to systems that transmit clock-encoded signals.

Bit-Error-Rate Test (BERT)

A shortcoming of percent jitter and eye mask measurements is that, even though the eye pattern may be open, errors may result from propagation delay and skew within the LVDS components when data is *clocked in*. Another way of saying this is that, regardless of the data quality, the data is erroneous if sampled at the wrong time. This is especially true in serializer-deserializer (SERDES) functions. This type of measurement not only ensures data quality, but also an accurate timing relationship between clock and data. The number of errors detected within a period determines the bit-error rate (BER) of the DUT.

Application report SLLA088 is an example of using BER for system evaluation. Section 2.1.2 of SLLA088 specifically addresses the propagation delay and clock considerations in order to perform the BER testing of the LVDS transmission in the VME card cage. At signaling rates in the range of hundreds of megabits per second, the propagation time on the transmission media is an important factor. Because the bit duration is lower than the VME backplane propagation delay, correct timing of the readout at the receiver is essential. There are two important factors at work in the VME example. First, the delay increases with the physical distance between the driver and the receiver. Second, the capacitance increases with increased backplane loading (more cards in the chassis), which increases the propagation delay, i.e., it slows down the backplane even more. Therefore, TI recommends an approach in which users send a data-clocking signal with the data so that the receiver can trigger on a separate clock line. Embedding the clock into the data stream offers another solution.

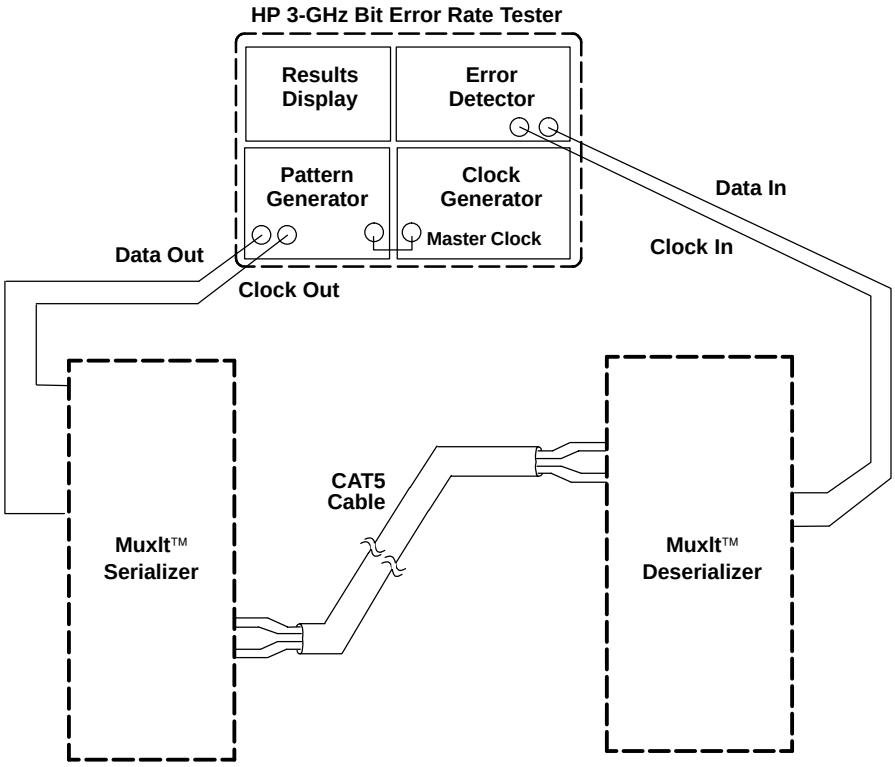

Figure 7–4. Example BER Test Setup With MuxIt™ EVM

A BER tester compares inputs and outputs of the DUT to determine if an error has occurred. Figure 7–4 shows a BER test set up where the DUT is the MuxIt™ EVM. For accurate comparison of the inputs of the serializer with the outputs of the deserializer, the BERT uses an alignment feature to compensate for the propagation delay through the DUT. After running the alignment, the BERT is ready to analyze the outputs of the DUT. We used this particular test setup to determine the BER for different cable lengths between the serializer and deserializer.

BER measurements can take large amounts of time depending upon the transmission rate and the desired BER to verify. For example, in order to verify a BER of $1x10^{-14}$ (1 error for every 10^{14} bits sent) with a signaling rate of 400 Mbps (UI is 2.5 ns), one would have to wait at least 69.4 hours (until 10^{14} bits were transmitted).

Cables, power splitters, and connectors used to carry signals from the DUT to the measuring device can influence the integrity of the signal. Cables need to be impedance matched with the DUT and the measurement device. Any discontinuities can result in reflections and poor measurements. Most cables and measurement terminations have an impedance of 50 Ω. Also, any capacitive attributes can limit the bandwidth of the cable and impact the displayed rise times in the same manner as a probe.

Electromagnetic Compatibility Testing

Three major standards define EMI compliance. These standards are FCC Title 47; part 15; Subpart B, EEC CISPR 22, and MIL-STD 461. MIL-STD 461 is the most inclusive, containing requirements for radiated emissions, radiated susceptibility, conducted emissions, and conducted susceptibility. The FCC and EEC commercial product standards for EMI are very similar and only address emissions.

The difficult part of EMI evaluation is finding or creating an open area test site that is electromagnetically isolated and still provides the physical dimensions specified by the standards. CISPR 22 specifies 30 m (Class A) and 10 m (Class B), while the FCC specifies 10 m (Class A) and 3 m (Class B). Users can replace expensive 30-m anechoic chambers by smaller enclosures that measure the spectral content (usually along multiple axes) and scale the measurements to the appropriate test configuration. Conversely, the measurement equipment can take the emission standard and scale the intensities to the smaller chamber environment.

MuxIt is a trademark of Texas Instruments.

Just as it is important to prevent test equipment from influencing test measurements, it is also important to control any external interference when testing. Radiated and conducted emissions are the most notable type of interference in commercial systems. Whether it is preventing the exposure to emissions by shielding or using a chamber, or grounding schemes to prevent conducted emissions, users need to consider both of these external factors even outside of EMI testing.

Troubleshooting

Results obtained from high confidence measurements are not always as expected. Failure to meet standards or system requirements usually requires further analysis, especially in the prototype and developing stages of a product. The remainder of this chapter intends to provide some examples of problems and some direction on how to troubleshoot problems in LVDS systems.

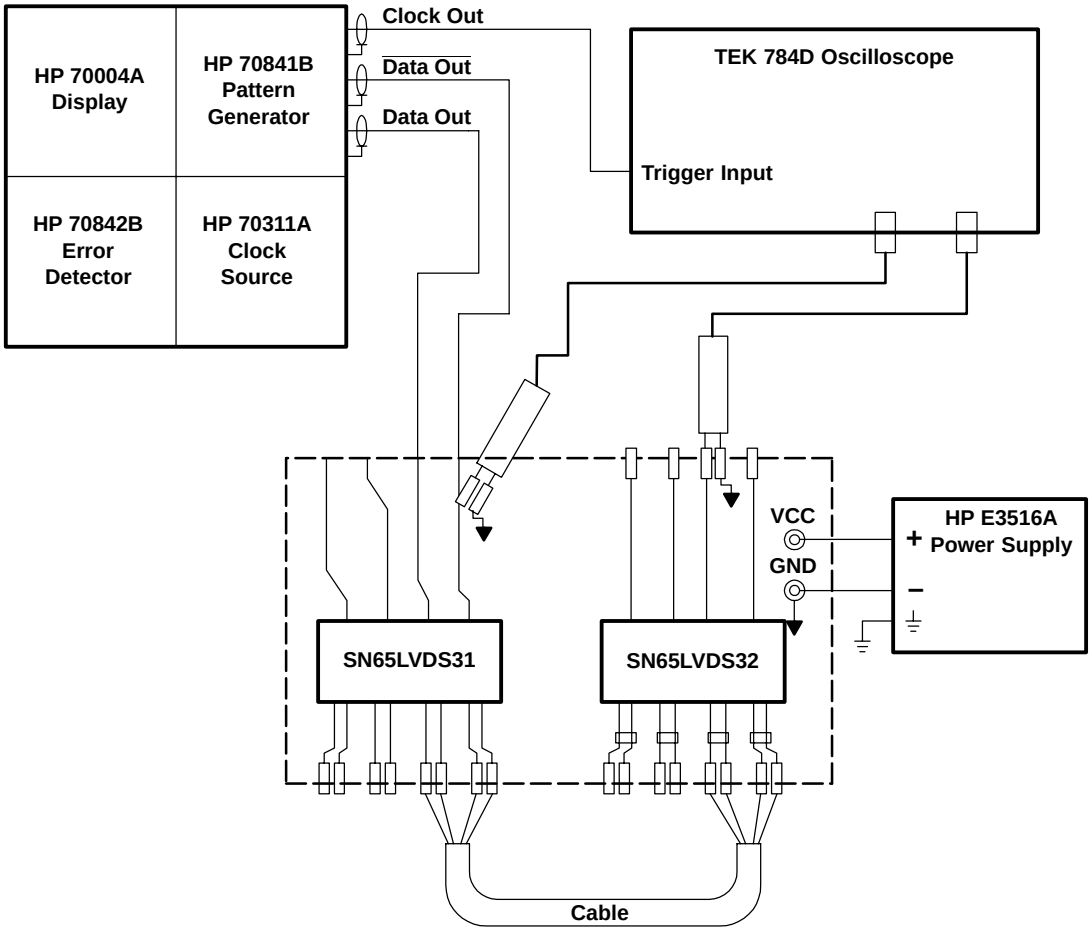

Figure 7–5. Test Setup for Trouble Shooting Section

Common LVDS Problems

Nonterminated outputs: All of the Texas Instruments LVDS product line requires proper termination. Leaving the LVDS outputs open results in the outputs swinging from rail to rail (0 V to 3.3 V) instead of the low-voltage swing of 400 mV.

The *Flying A* and *Flying V*: The most common reason for a *flying A* or *flying V* is that the non-LVDS inputs to the LVDS device are not symmetrical about the transition threshold. In Figure 7–6, the input to the SN65LVDS31 (CH2) varies from 0 V to 1.6 V, which does not meet the input specification of this device. The result is the flying *A* at the output (CH3) of the SN65LVDS32B receiver.

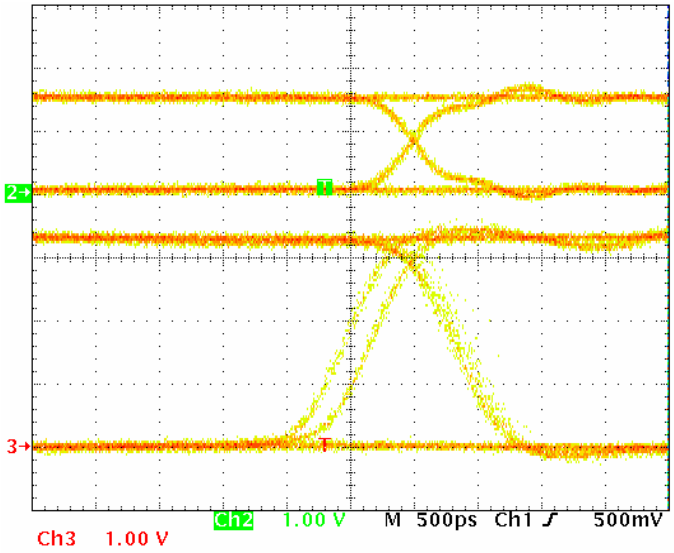

Figure 7–6. Flying *A*

A Flying A or *V* can also occur if the Vcc or GND of the device is not at the specified value, which can affect the input threshold of the device. One of the benefits of the LVDS current drivers from Texas Instruments is the immunity to variances in trace lengths within differential pairs. Since the current through the resistor determines the voltage at the receiver, there is no possibility for the voltage to change on one side of the termination and not the other. While this is a benefit at low speeds, other factors such as impedance matching and cross talk become more evident if the traces are not the same.

Noisy rails are the result of either noisy Vcc or GND. A lack of decoupling capacitors or ground bounce can cause noise to appear on the top or bottom of the eye pattern.

Signal Integrity

When one of the aforementioned situations does not distort the transmission waveform, signal quality becomes the focus of possible causes of error. This is usually associated with an eye pattern where the jitter measurement is greater than 25 percent of the UI. This measurement of percentage jitter or peak-to-peak jitter provides an indication of the quality of the transmitted signal, but not the causes of the jitter. In addition to knowledge of the system, the distribution of the jitter can provide some insight into the factors which contribute to overall jitter of the peak-to-peak measurement. Both the distribution and the peak-to-peak values can give a test engineer an idea of the deterministic and random components of jitter.

Random Jitter

Random jitter is the result of any random fluctuations, which include movement of electrons in conductors and thermal variations. There is purely random jitter in theory and not in real applications. Jitter is always a combination of deterministic and random components. Figure 7–7 is an example of jitter with a minimal amount of deterministic contribution. The distribution at the top of the scope picture is somewhat Gaussian or bell shaped, demonstrating the major influence of the random jitter. In Figure 7–7, channel 3 is the input and channel two is the output of a simple balanced waveform.

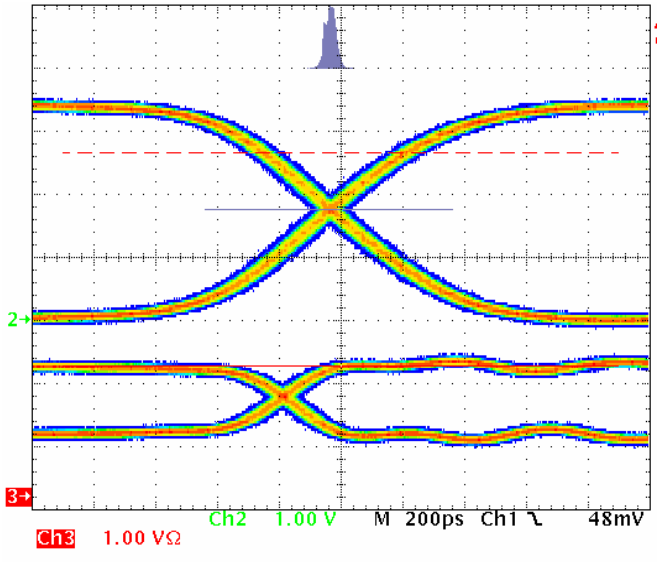

Figure 7–7. Input and Output Eye-Crossing With 100-MHz Clock Signal

Deterministic Jitter

Sources of deterministic jitter can include cross talk, skew, and ISI. While there are other sources of deterministic jitter, these are the most common and are the focus of discussion. Figure 7–8 is an example of how deterministic jitter affects the distribution. The only difference between the tests that generated Figure 7–7 and Figure 7–8 is the type of data transmitted by the system. Figure 7–7 uses balanced data and Figure 7–8 uses a PRBS (10^{23} –1). The use of balanced data reduces any pattern-dependent skew created from ISI, while the PBRS data is a worst-case data type to generate the most skew from ISI. The distribution still has the presence of random components, as evidenced by the Gaussian shapes; however, the presence of multiple peaks reveals a more prominent deterministic component. The significance of this observation is simple. When the jitter is random, the problem lies in either the thermal or the molecular properties of the devices and or interconnects. When the distribution displays a very deterministic effect, such factors like skew, cross talk, or EMI are affecting the signal integrity. By controlling the test, users can conclude that the degradation in signal integrity is due to ISI.

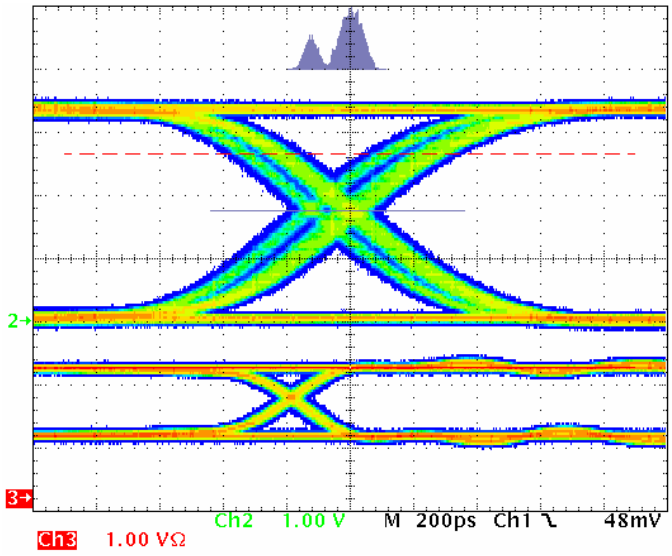

Figure 7–8. Input and Output Eye-Crossing With PRBS Data at 200 Mbps

Figure 7–9 is the same measurement as in Figure 7–7 but in the presence of another active channel. The input to both channels is a balanced signal transmitting at a rate of 200 Mbps. The jitter does not increase significantly by adding a nearby channel, indicating that effects, like cross talk, are minimal. However, Figure 7–8 and Figure 7–10 show a significant increase in jitter by adding a second channel. This is particularly interesting because crosstalk now appears to be contributing to the jitter while there was no significant increase with the dc-balanced examples. Crosstalk is jitter coupled and inducted from the magnetic fields generated by nearby signals that produce impedance changes in components, connectors, and transmission lines. Adjacent synchronous and in-phase signals may amplify these frequency-dependent effects. There appears to be energy coupled from the ISI from channel to channel (crosstalk), thus increasing the jitter of the LVDS devices.

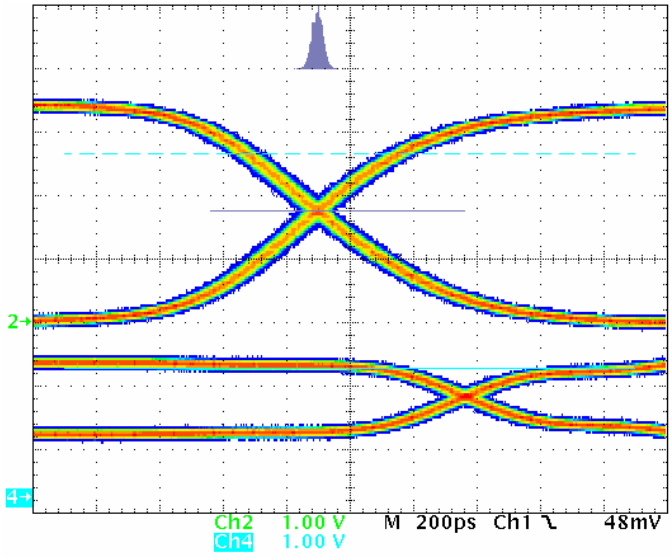

Figure 7–9. Jitter With Adjacent Channel In Operation and Clock Signal

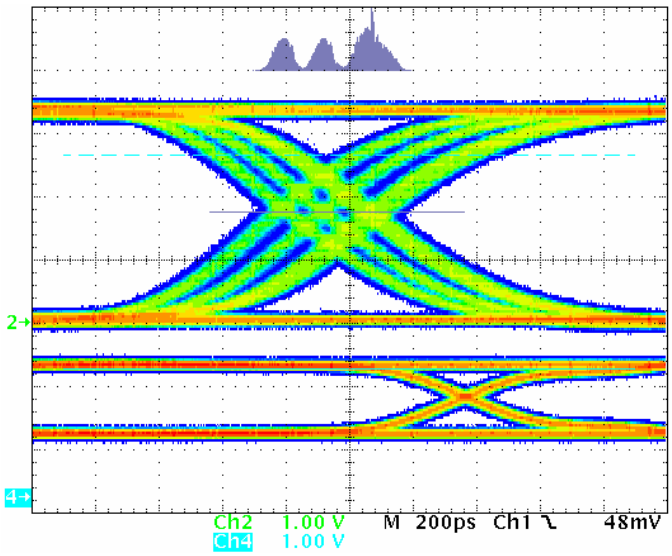

Figure 7–10. Jitter With Adjacent Channel and PBRS Data

Time Domain Reflectometry (TDR)

TDR can also be a great troubleshooting tool to locate transmission line problems. TDR is not a true signal integrity measurement, but provides great insight into the continuity and characteristics of a transmission line which affect signal integrity. The premise of TDR is to launch a wave down a transmission line and observe the reflections. You can make a simple TDR measurement with a function generator and a high-speed oscilloscope, see Figure 7–11 for test setup. The waveform on the display provides information about the number of discontinuities (number of reflections), the distance to the reflections (calculated by the time delay and the velocity of propagation of the media), the characteristics of the continuities (inductive, capacitive, or resistive components), and the cable loss. Again, these are not true signal integrity measurements, but these reflections give an indication of the quality of the transmission line. Figure 7–11 is taken from *Time Domain Reflectometry Theory*, Application Note 1304-2 of Agilent Technologies, which also provides examples of different types of reflections and how to make related calculations.

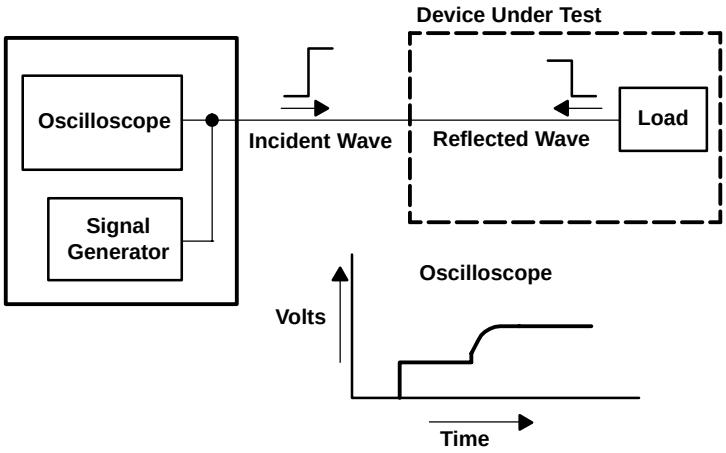

Figure 7–11. TDR Setup

You can also use spectrum and network analyzers to make TDR measurements. However, for correlation with other time domain measurements, the analyzer must be able to utilize the fast Fourier transform (FFT). The main reason for moving to TDR and away from spectrum and network analyzers is the presentation of information in the time domain.

Conclusion

The testing of LVDS systems involves understanding of the requirements and standards, selecting of measurement devices, compensating for the impact of measurement devices, minimizing external influences, and planning to deal with systems that fail the requirements.

References

1. *A New Method for Jitter Decomposition Through Its Distribution Tail Fitting*; Li, Wilstrup, Jessen, and Petrich; Wavecrest Corp.
2. *High-Speed Digital Design, A Handbook of Black Magic*; by H. Johnson and M. Graham

Glossary

1596.3 or IEEE-1596.3—IEEE physical layer specification, suitable for use with the IEEE 1596 Scalable Coherent Interface. Low-voltage swing, differential-signaling techniques are specified for the electrical characteristics. Electrical characteristics differ from TIA/EIA-644 in some areas.

644 or TIA/EIA-644—TIA/EIA standard defining an electrical layer signaling technology utilizing low-voltage differential signaling (LVDS). Defines the electrical characteristics for most LVDS vendors.

644-A or TIA/EIA-644A—TIA/EIA standard building on TIA/EIA-644, and incorporating additional specifications to support multidrop operation.

Balanced signaling—A description of two circuits that have identical electrical properties such that when driven with signals of equal magnitude but in opposite directions there is little ac common-mode energy in the two circuits.

BER—Bit error rate. The probability of a single transmitted data bit being incorrectly detected by a receiver due to noise and/or timing errors.

Bus—A bus is a common electrical connection between multiple devices.

CAT-5 —Category 5 cabling. 100-Ω nominal, unshielded twisted-pair cable. Electrical transmission characteristics are specified by TIA/EIA-568A.

Characteristic impedance or Zo—The ratio of the voltage to current at any point on a transmission line. For a lossless transmission line Zo=sqrt (Lo/Co), where Lo is the inductance per unit length, and Co is the capacitance per unit length.

Common-mode voltage—The common-mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. The common-mode voltage at a receiver input is the sum of ground potential difference, driver common-mode output voltage (driver offset voltage), and longitudinally coupled noise.

Common-mode voltage range—The range of common-mode voltages over which a receiver can correctly detect the logic level at its input.

Current mode—A drive circuit that relies on an output-stage current source to set the drive current delivered to the load.

Deterministic jitter—The component of the total jitter present in a system that is bounded in magnitude, and is traceable to specific causes such as transmitted data patterns (ISI), pulse skew, simultaneous switching noise, etc.

Differential mode—A signaling mode that uses one of a driven signal pair as the zero-potential reference.

ECL—Emitter-coupled logic. A class of high-speed interface circuits that consist of a current-switching differential amplifier followed by emitter followers in output stages. The choice of supply voltages determines the subclass of negative ECL (NECL), positive ECL (PECL), or low-voltage positive ECL (LVPECL).

Effective Length—Used to characterize a system as distributed or lumped with regards to some electrical feature. Equal to the electrical feature time (e.g., rise time) divided by the propagation delay per unit length.

Embedded Clock—A data encoding approach where data and clock signals are combined into a single signal stream to eliminate data-to-clock skew issues, maintain dc balancing, and reduce interconnect requirements.

EMC—Electromagnetic compatibility. A term used to describe the absence of conducted and radiated emissions that exceed specified limits, and the capability of a system to operate in its electromagnetic environment without performance degradation.

EMI—Electromagnetic interference. A term used to describe conducted and radiated emissions which are above specified limits or cause system performance degradation.

ESD—Electrostatic discharge. ESD is the transfer of electrostatic charge between bodies that are at different electrostatic potential. Three ESD tests are standardized: Human body model (HBM), machine model (MM), and charged device model (CDM).

Eye pattern—A measure of the data signal transmission path quality using an overlay pattern of random data signal transitions.

Failsafe—Refers to the deterministic response of receivers when an invalid input condition exists at the receiver pins.

Full duplex—A data transmission system that allows for simultaneous bidirectional data transfer.

Ground shift—The difference between the signal ground potential between the active driver and a receiver of an interchange circuit.

Half duplex—A data transmission system that allows for bidirectional data transfer, but is limited to single direction data transfer at any instant in time.

Hysteresis—The difference between the positive and negative going receiver input voltage thresholds. Incorporated into receivers to reduce output oscillations in response to input signal noise.

Idle line—An idle line is a point-to-point, multidrop, or multipoint line with all drivers disabled.

Idle-line failsafe—Used to designate receivers that provide a deterministic response when an idle line condition is present.

Insertion/removal—The ability to attach and remove devices while the system is in operation.

Intersymbol interference (ISI)—Intersymbol interference is the time displacement of a state transition due to a new wave (subsequent signal) arriving at the receiver site before the previous wave has reached its final value.

Jitter—The variation, over time, of the instant a binary signal crosses a threshold (state transition) from the ideal occurrence.

LVDM—Low voltage differential signaling for multipoint. A TI LVDS designation for drivers that provide high output current to drive multipoint buses, increase noise margin, etc.

LVDT—A TI LVDS designation for receivers that provide integrated line termination resistors.

M-LVDS or TIA/EIA-899—Multipoint low-voltage differential signaling. TIA/EIA standard that specifies the driver and receiver characteristics for low-voltage differential signaling interface circuits operating in a multipoint environment.

Multidrop—A data bus structure that has one transmitting and two or more receiving connections.

Multipoint—A data bus structure that has two or more transmitting and any number of receiving connections.

Offset—Used to refer to the common-mode voltage at the output of a driver circuit.

Open-line failsafe—Used to designate receivers that provide a deterministic response when the input to the receiver is disconnected, and no line termination is present across the receiver inputs.

Output skew—Unintentional misalignment of the edges of two or more parallel outputs of a device

Point-to-point—Point-to-point refers to a communications line that provides a unidirectional path from a single driver to a single receiver.

Power up/down glitch free—A feature of line circuits that assures monotonic transitions of output or inputs during power cycling.

Propagation velocity or v—The speed at which a traveling wave propagates through a transmission line. For a lossless transmission line $v = 1/\sqrt{L_O C_O}$ where Lo is the inductance per unit length, and Co is the capacitance per unit length.

Pulse skew—Unintentional differences between the high-to-low propagation time for a device and the low-to-high propagation time for a device. Will result in changes to the duty cycle for a clock input signal.

Random jitter—The component of total jitter characterized by a Gaussian statistics and arising thermal vibrations, process imperfections, etc.

SERDES—Serializer-deserializer. Used to refer to a class of devices that convert parallel input data to a serial format to take advantage of transmission efficiencies, followed by a conversion back to a parallel format at the receiving link end.

Shorted-line failsafe—Used to designate receivers that provide a deterministic response when the differential input signal is 0 V due to a shorted transmission line.

Signaling rate—The number of transitions that are made per second, for a single circuit, expressed in units of bits per second. Equal to $1/t_{UI}$, where UI is the unit interval.

Simplex—A data transmission system that allows for data transmission in only one direction.

Stubs—Short traces, branching from the main transmission line or bus.

Terminated line failsafe—Used to designate receivers that provide a deterministic response when no drivers are connected to the transmission line but a path to a termination resistor exists.

Total jitter—The peak to peak jitter observed in a transmission system arising from the combined effects of random and deterministic jitter. Usually reported with an associated BER metric.

Transfer rate—The number of parallel data transfers per second, accounting for the timing considerations due to parallel channel differences.

Transition time—The transition time is the 20%-to-80% rise or fall time of a binary signal.

Type 1—A class of receivers, specified by the M-LVDS standard, that have their thresholds centered about 0 volts.

Type 2—A class of receivers, specified by the M-LVDS standard, that have their thresholds offset from 0 volts.

Unit interval—The unit interval (UI or t_{UI}) is the mathematical inverse of the signaling rate.

Voltage mode—A drive circuit that relies on output-stage and load circuit impedance to set the drive current delivered to the load.