Application Brief

TPLD In-System Developing

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TPLD™ devices need a serial peripheral interface (SPI) or inter-integrated circuit (I2C) interface to be configured temporary or permanently. Moreover, TPLD801 and TPLD1201 devices need a general purpose input (GPI) line as well, which means that five general-purpose input/output (GPIO) total (IO5, IO4, IO2, IO1 and GPI) must be used for configuration. In some cases, the user prefers to install the TPLD device in one's own system specially in the development phase of a given project.

Because the number of general purpose input/outputs (GPIOs) are limited, a method to temporarily program the device using SPI can be possible by installing tri-state buffers in the lines that are going to be used for temporary programming and also used as GPIOs in the system. In this way, isolation can be generated when the programming lines are needed to update the TPLD functionality. Figure 1 illustrates this concept.

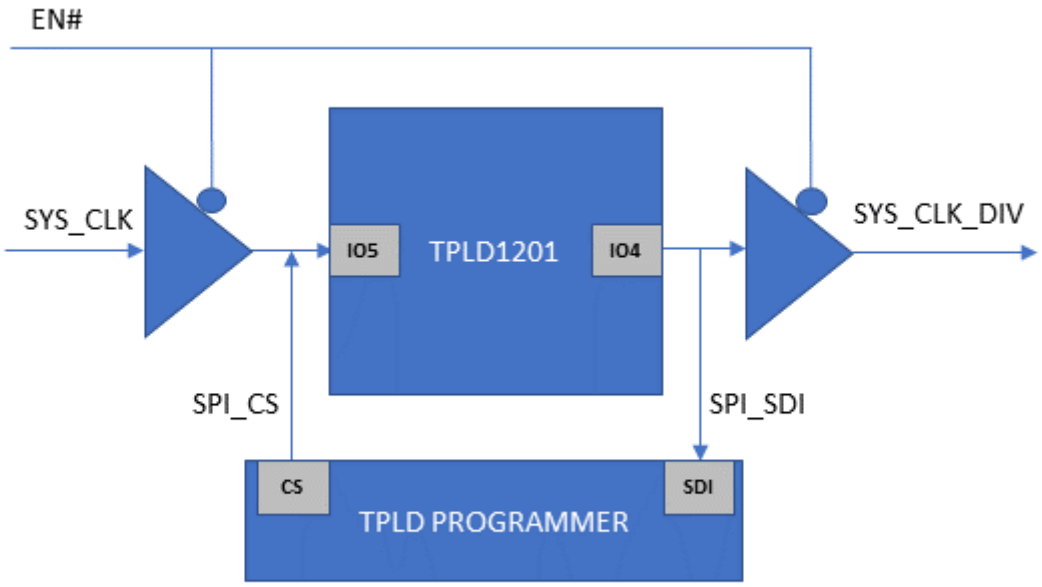

Figure 1. TPLD In-system Developing Block Diagram

Testing the Prototype

Figure 2 shows a developing system including some TI SN74LVC1G125 tri-state buffers (top), the TPLD1201 (middle), a jumper and a programming port (bottom). The jumper is going to be used to select either the programmer lines or the external signals that are being used by the TPLD GPIOs in the current system. To reach the TPLD pins that are needed to program the device, the customer must install pin headers or a double-row connectors, for instance, to provide the configuration signals that are coming from the programmer.

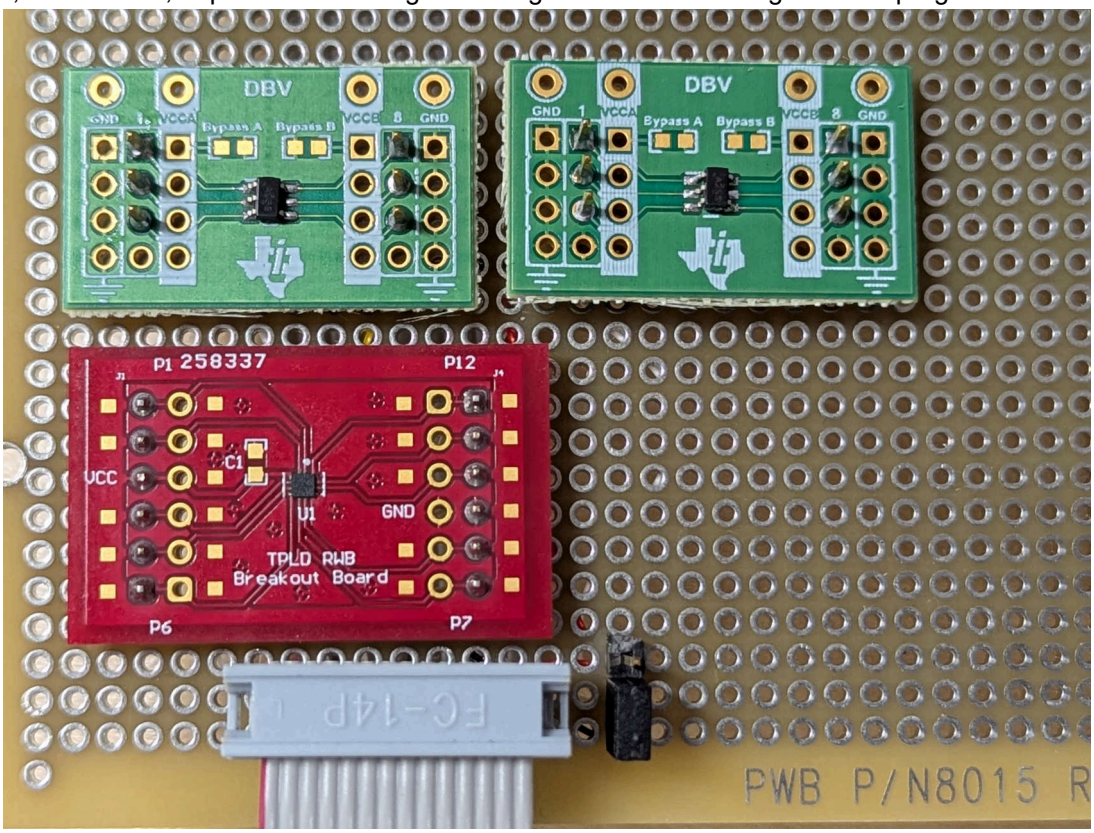

Figure 2. TPLD In-System Developing Prototype Example

Suppose the TPLD is going to divide by two an input frequency. In this case, the input signal SYS_CLK is active all the time and attached to a tri-state buffer input. Meanwhile TPLD GPIO5 is tied to the tri-state buffer output. Figure 3 shows that SYS_CLK is running all the time but is not able to reach GPIO5 because the tri-state enable (OE#) is deasserted high.

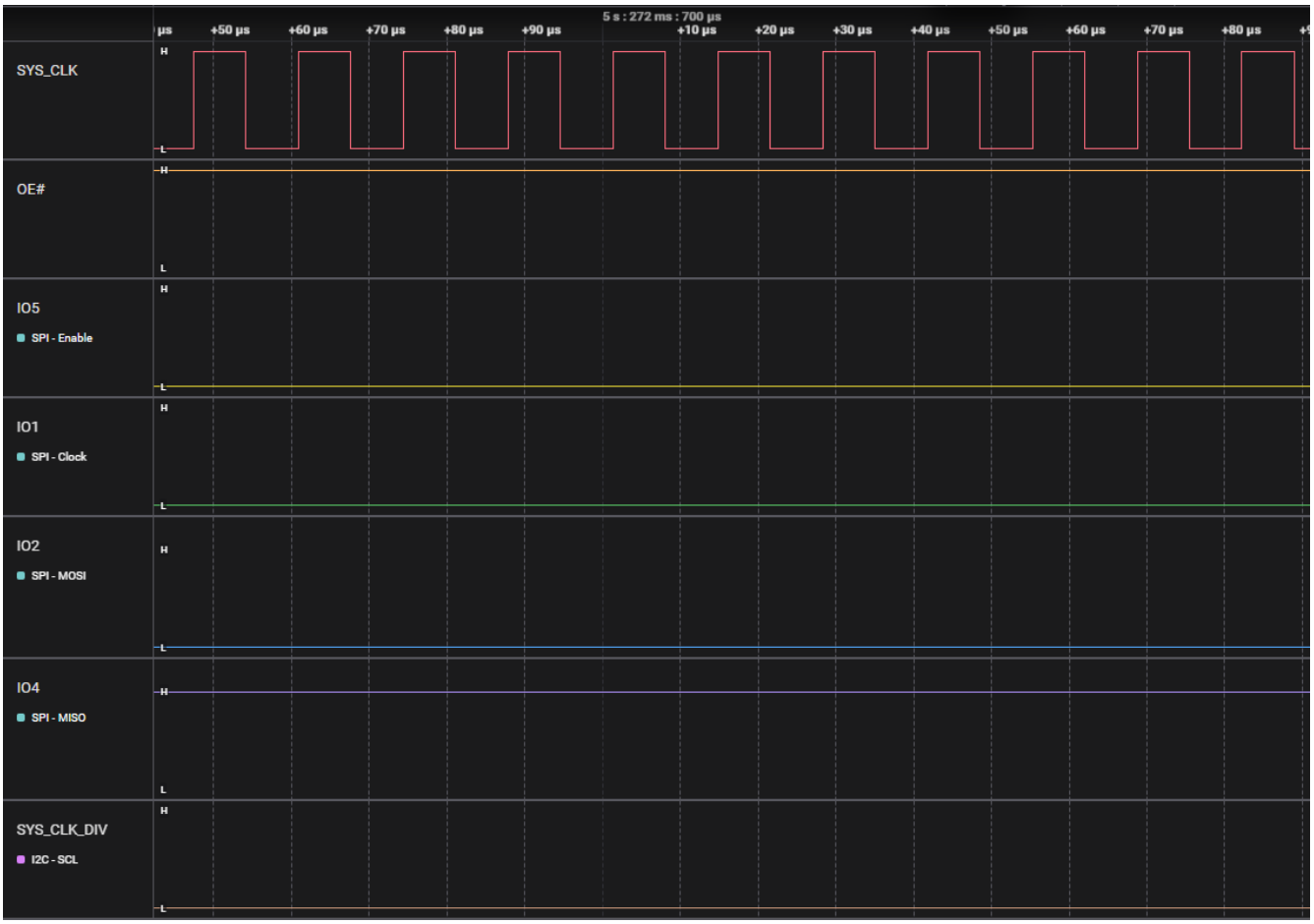

Figure 3. TPLD Unprogrammed

Figure 4 shows that the TPLD is being programmed through the SPI interface using the same OE# configuration. The SYS_CLK signal is active but isolated from GPIO5, but the SPI CS line.

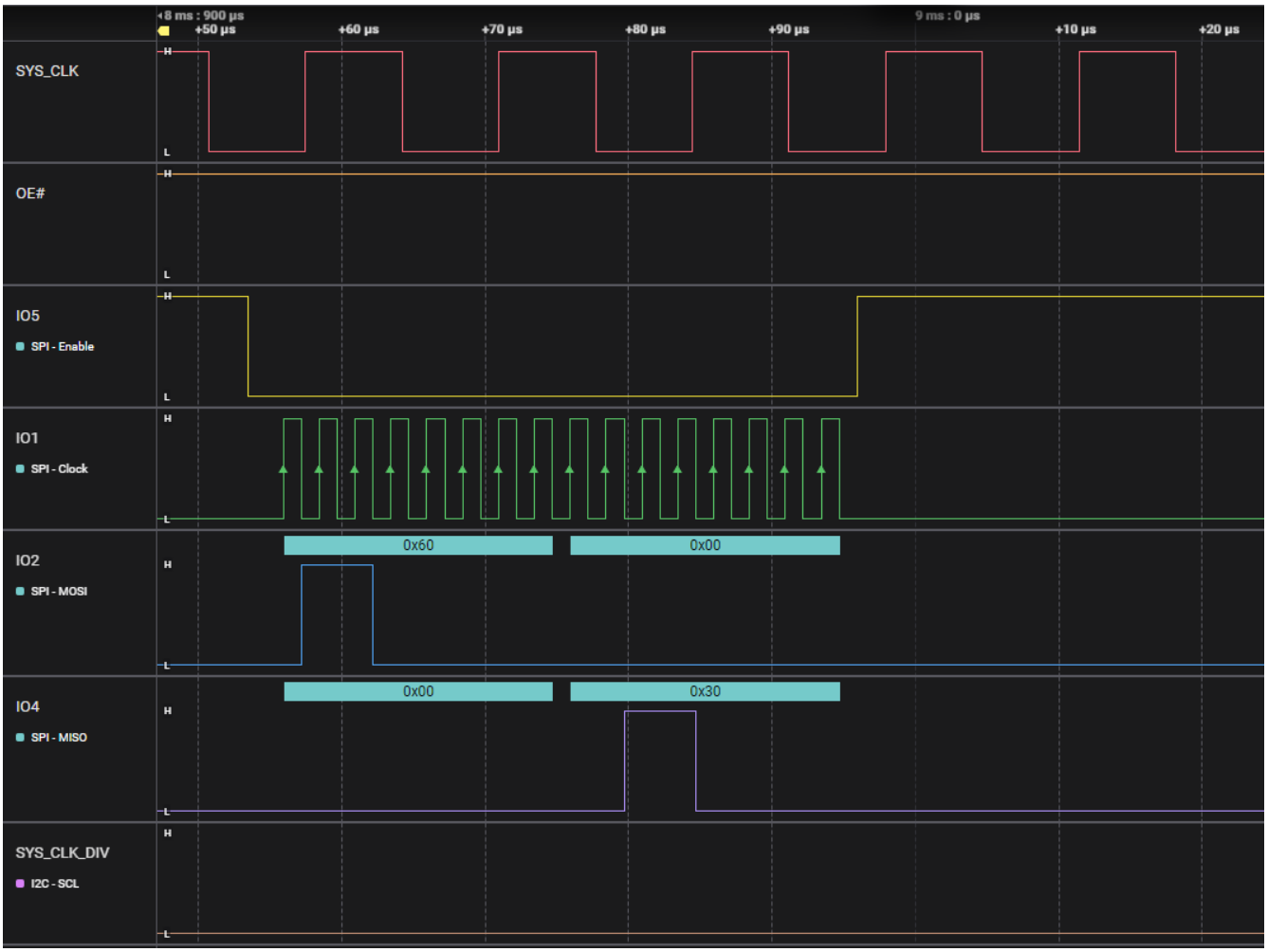

Figure 4. TPLD During Programming

Once the device is programmed, OE# can be grounded to activate the tri-state buffers so the external clock is reaching IO5 and the clock output (CLK_SYS divided by 2) is present in IO4 and also at the output tri-state buffer as shown in Figure 5.

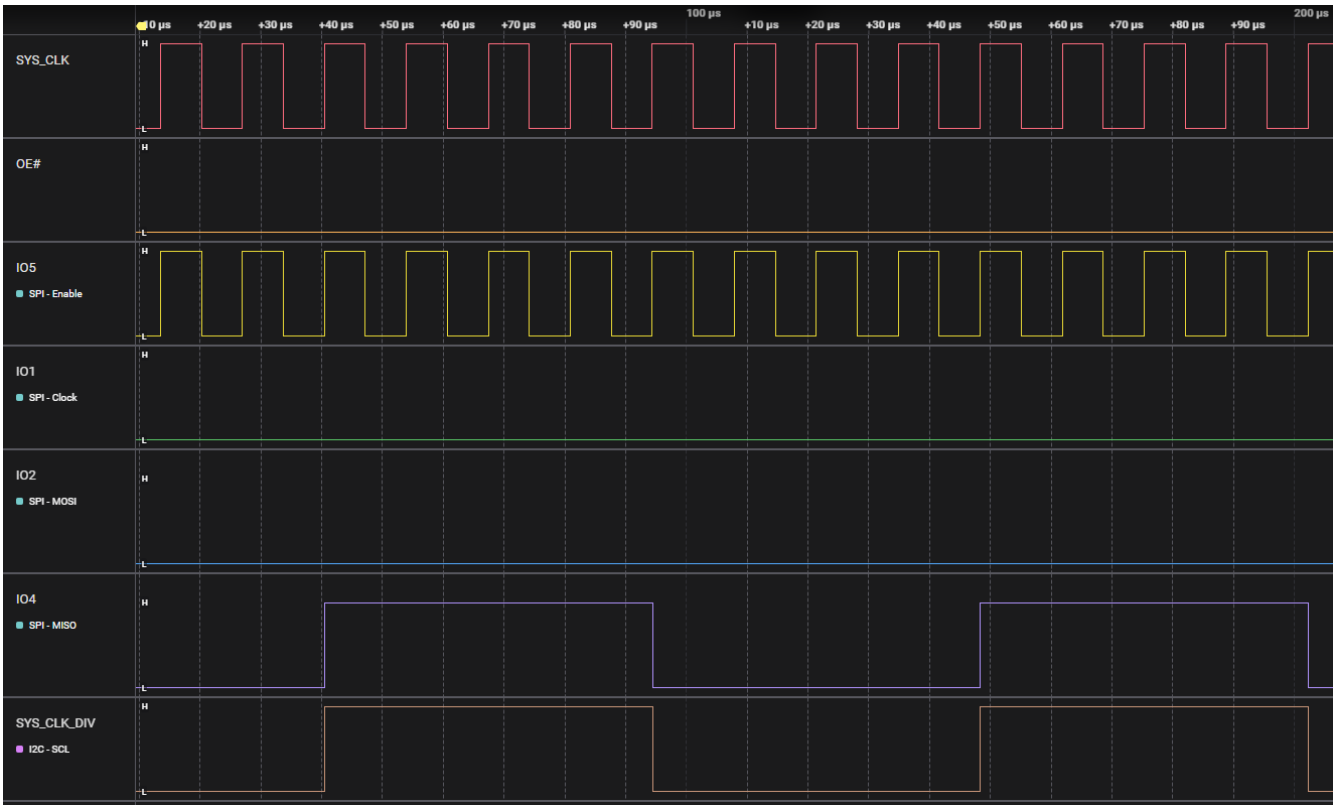

Figure 5. TPLD After Programming

Conclusion

It is possible to make changes to or add features to a system with TPLD devices using external tri-states buffers to isolate the device during the upgrade of its internal configuration. The number of such buffers depends on how many GPIOs must be used both as GPIO and as configuration pins as well. Finally, it is important to remember that the method described above can not be applied to GPI because it also has an alternative function as +8V VPP, a voltage that is at the top of the maximum 5V typically accepted by tri-state buffers.

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