

How to Configure the TUSB1044 Using SigCon Architect



ABSTRACT

This Falcon SigCon Architect document explains how to configure your TUSB1044 redriver using the user-friendly GUI.

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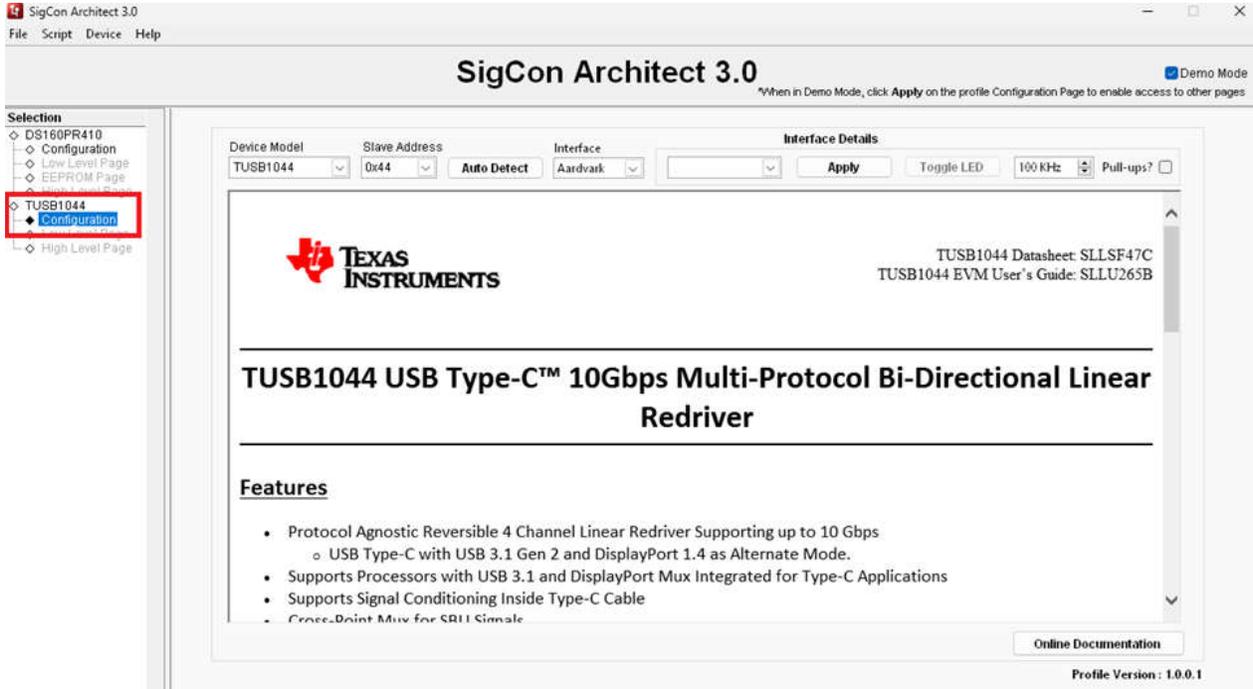
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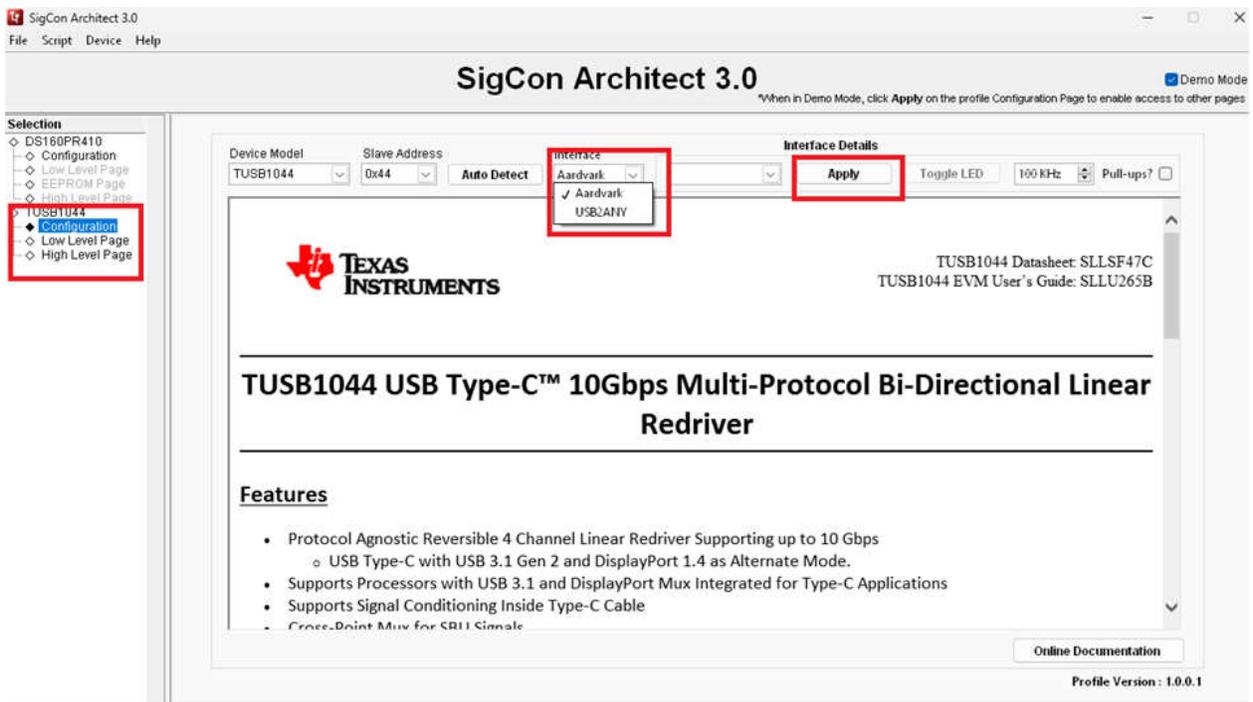
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1 Getting Started

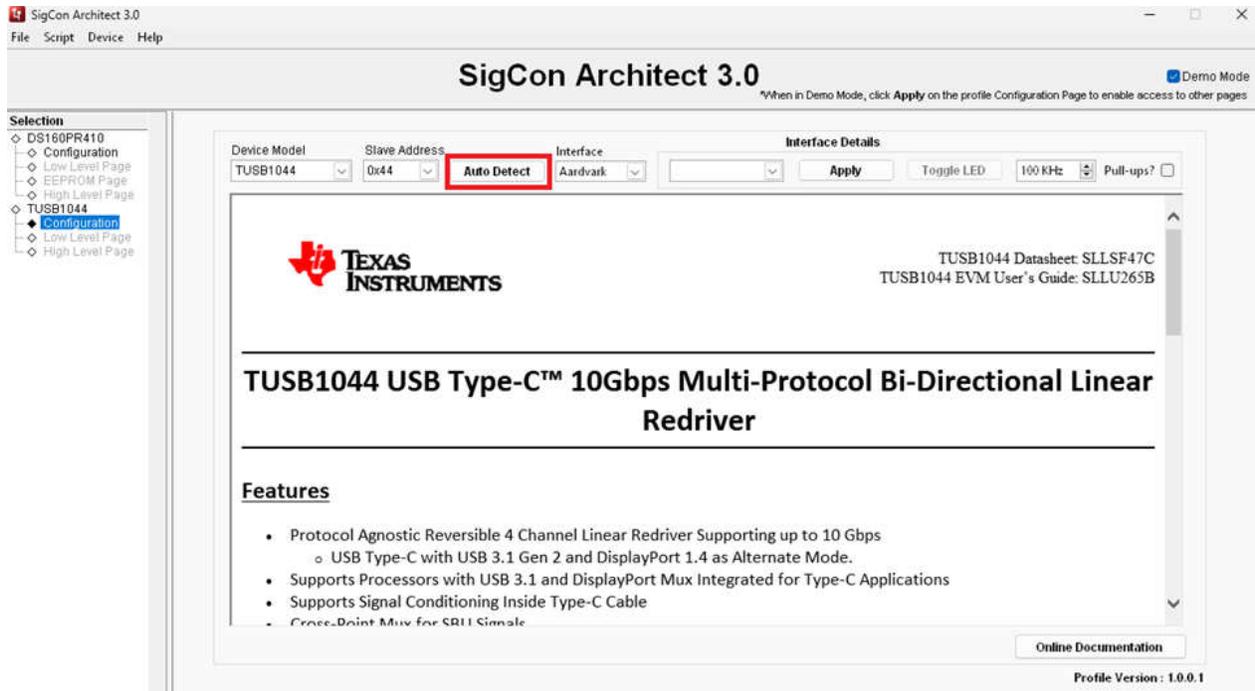
1. Download and install SigCon Architect. Follow the steps in the [SigCon Architect: Installation and Starter's Guide](#) for detailed instructions.
2. Download and install the TUSB1044 Profile Updater.
3. Connect a USB2ANY Interface Adapter or Aardvark I²C Host Adapter to the desired TUSB1044 and PC.
4. Open SigCon Architect and click the *Configuration* tab below the TUSB1044 profile on the left, as shown below.



5. Ensure the correct interface adapter is selected below the interface drop-down menu (USB2ANY or Aardvark), then click **Apply** to activate the other tabs under the TUSB1044 profile. Click the desired tab to begin programming the device.



6. Click the **Auto Detect** button to detect the device and I²C bus addresses.

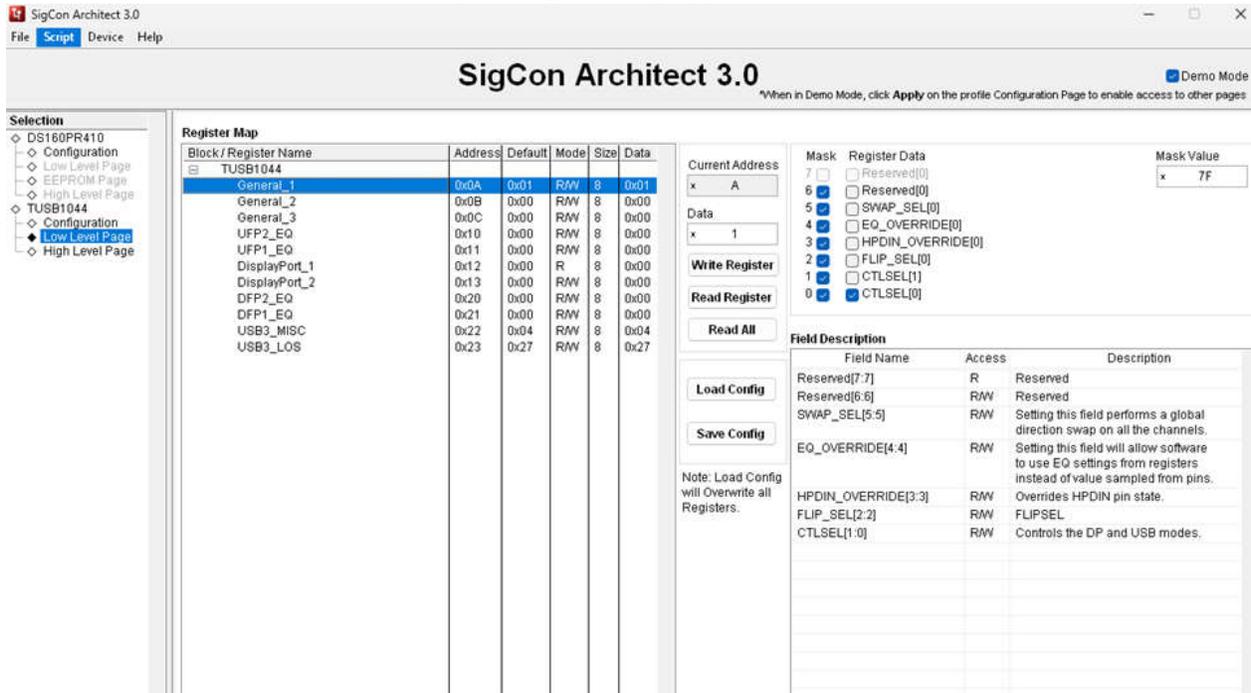


7. Descriptions of each tab is listed below:

- Low Level Page: Individual register access to the lowest level of the device. Can be used to change specific settings, or to verify changes from the high-level page have taken effect.
- High Level Page: Main page used to change EQ settings of the device and to see the active status of each channel

2 Low Level Page

- When the device is selected, the complete register map appears in the table below.



SigCon Architect 3.0 Demo Mode

*When in Demo Mode, click **Apply** on the profile Configuration Page to enable access to other pages.

Selection

- DS160PR410
 - Configuration
 - Low Level Page
 - EEPROM Page
 - High Level Page
- TUSB1044
 - Configuration
 - Low Level Page**
 - High Level Page

Register Map

Block / Register Name	Address	Default	Mode	Size	Data
TUSB1044					
General_1	0x0A	0x01	RAW	8	0x01
General_2	0x0B	0x00	RAW	8	0x00
General_3	0x0C	0x00	RAW	8	0x00
UFP2_EQ	0x10	0x00	RAW	8	0x00
UFP1_EQ	0x11	0x00	RAW	8	0x00
DisplayPort_1	0x12	0x00	R	8	0x00
DisplayPort_2	0x13	0x00	RAW	8	0x00
DFP2_EQ	0x20	0x00	RAW	8	0x00
DFP1_EQ	0x21	0x00	RAW	8	0x00
USB3_MISC	0x22	0x04	RAW	8	0x04
USB3_LOS	0x23	0x27	RAW	8	0x27

Current Address
x A

Data
x 1

Write Register

Read Register

Read All

Load Config

Save Config

Note: Load Config will Overwrite all Registers.

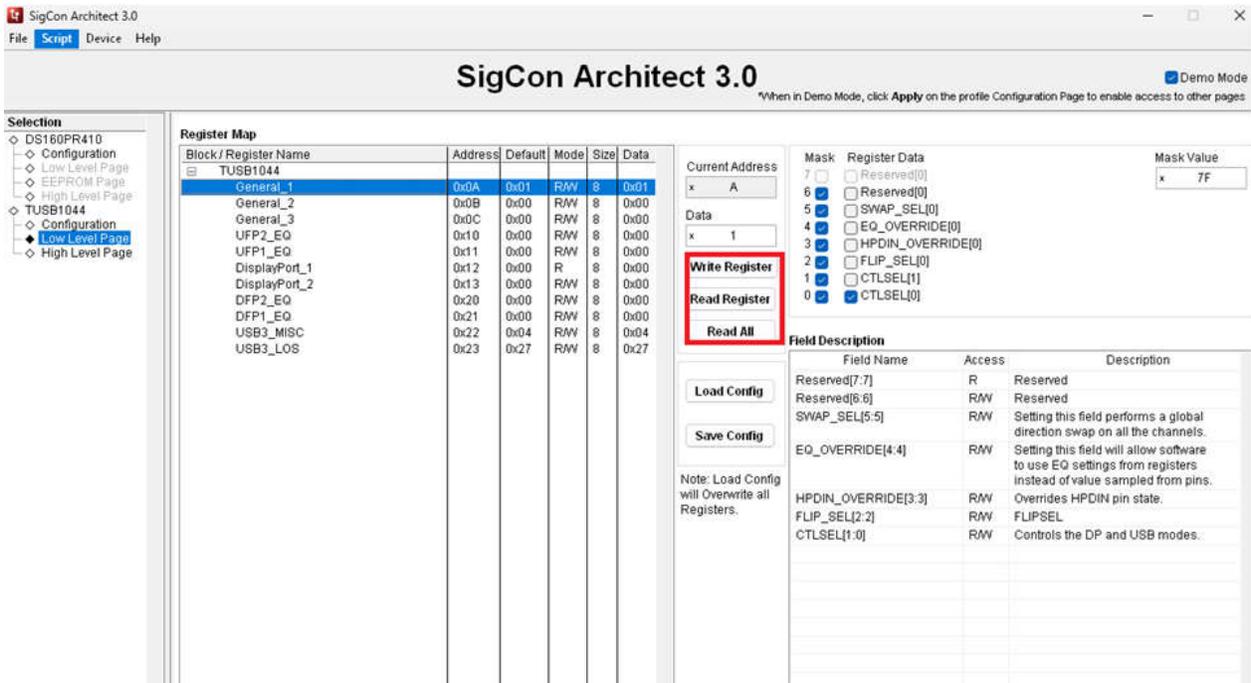
Mask Register Data Mask Value

Mask	Register Data	Mask Value
7	<input type="checkbox"/> Reserved[0]	x 7F
6	<input type="checkbox"/> Reserved[0]	
5	<input type="checkbox"/> SWAP_SEL[0]	
4	<input type="checkbox"/> EQ_OVERRIDE[0]	
3	<input type="checkbox"/> HPDIN_OVERRIDE[0]	
2	<input type="checkbox"/> FLIP_SEL[0]	
1	<input type="checkbox"/> CTLSEL[1]	
0	<input checked="" type="checkbox"/> CTLSEL[0]	

Field Description

Field Name	Access	Description
Reserved[7:7]	R	Reserved
Reserved[6:6]	RAW	Reserved
SWAP_SEL[5:5]	RAW	Setting this field performs a global direction swap on all the channels.
EQ_OVERRIDE[4:4]	RAW	Setting this field will allow software to use EQ settings from registers instead of value sampled from pins.
HPDIN_OVERRIDE[3:3]	RAW	Overrides HPDIN pin state.
FLIP_SEL[2:2]	RAW	FLIPSEL
CTLSEL[1:0]	RAW	Controls the DP and USB modes.

- Click the **Read All** button to read the configuration of the entire device. Alternately, select a specific register and click the **Read Register** button to update the target register quicker. The current address field automatically updates with the highlighted register.



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UFP2_EQ	0x10	0x00	RAW	8	0x00
UFP1_EQ	0x11	0x00	RAW	8	0x00
DisplayPort_1	0x12	0x00	R	8	0x00
DisplayPort_2	0x13	0x00	RAW	8	0x00
DFP2_EQ	0x20	0x00	RAW	8	0x00
DFP1_EQ	0x21	0x00	RAW	8	0x00
USB3_MISC	0x22	0x04	RAW	8	0x04
USB3_LOS	0x23	0x27	RAW	8	0x27

Current Address
x A

Data
x 1

Write Register

Read Register

Read All

Load Config

Save Config

Note: Load Config will Overwrite all Registers.

Mask Register Data Mask Value

Mask	Register Data	Mask Value
7	<input type="checkbox"/> Reserved[0]	x 7F
6	<input type="checkbox"/> Reserved[0]	
5	<input type="checkbox"/> SWAP_SEL[0]	
4	<input type="checkbox"/> EQ_OVERRIDE[0]	
3	<input type="checkbox"/> HPDIN_OVERRIDE[0]	
2	<input type="checkbox"/> FLIP_SEL[0]	
1	<input type="checkbox"/> CTLSEL[1]	
0	<input checked="" type="checkbox"/> CTLSEL[0]	

Field Description

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Reserved[7:7]	R	Reserved
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HPDIN_OVERRIDE[3:3]	RAW	Overrides HPDIN pin state.
FLIP_SEL[2:2]	RAW	FLIPSEL
CTLSEL[1:0]	RAW	Controls the DP and USB modes.

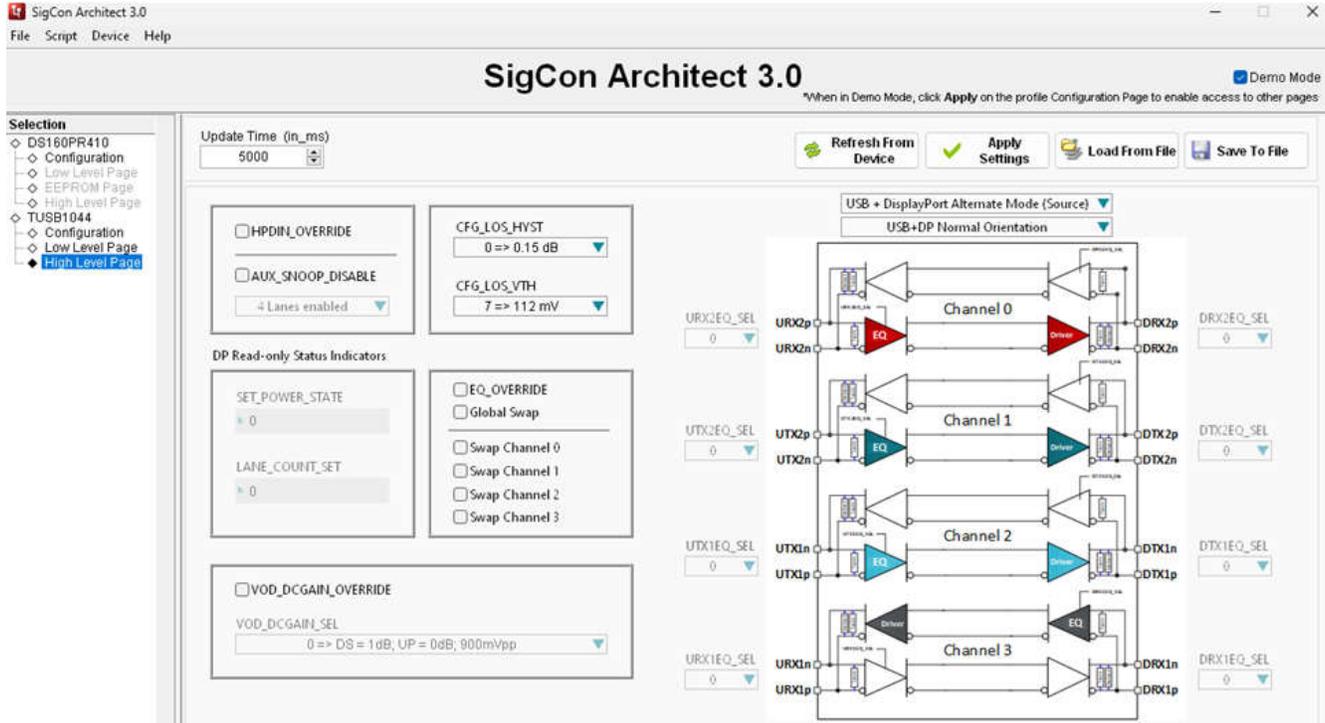
- To write to the selected register, check or deselect the boxes in the Register Data field. You can also manually enter a hex value into the Data field. Click the **Write Register** button to complete the update, then click the **Read Register** button to verify that the change was made. Note the Field Description table describes the function of each bit in the highlighted register
- Use the Save Config and Load Config buttons to save the current configuration in a .cfg file, and load the file back as needed. Click the **Reset Device** button to reset every setting to the default.

3 High Level Page

The TUSB1044 redriver features a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of a passive channel.

This page is used to quickly and easily adjust the EQ settings as needed for your specific application. A further description of this feature is described in the data sheet.

The High Level page also contains a device status page which shows which channels are detecting a signal.



The screenshot displays the SigCon Architect 3.0 software interface. On the left, a 'Selection' tree shows the navigation path: DS160PR410 > Configuration > Low Level Page > EEPROM Page > High Level Page > TUSB1044 > Configuration > Low Level Page > High Level Page. The main configuration area is titled 'USB + DisplayPort Alternate Mode (Source)' and 'USB+DP Normal Orientation'. It features several control panels:

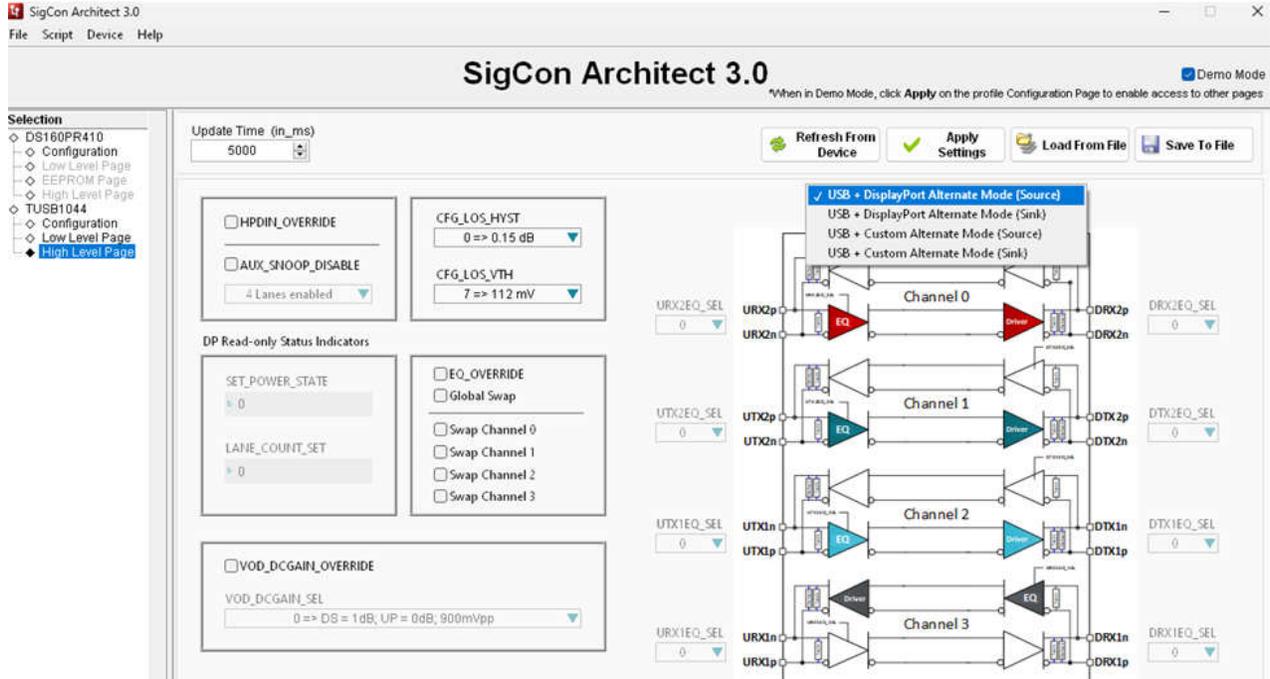
- Update Time (in_ms):** Set to 5000.
- HPDIN_OVERRIDE:** A checkbox.
- AUX_SNOOP_DISABLE:** A checkbox with a dropdown set to '-4 Lanes enabled'.
- CFG_LOS_HYST:** A dropdown set to '0 => 0.15 dB'.
- CFG_LOS_VTH:** A dropdown set to '7 => 112 mV'.
- DP Read-only Status Indicators:** Includes 'SET_POWER_STATE' (0), 'LANE_COUNT_SET' (0), and 'EQ_OVERRIDE' (checkboxes for Global Swap and Swap Channel 0-3).
- VOD_DCGAIN_OVERRIDE:** A dropdown set to '0 => DS = 1 dB, UP = 0dB, 900mVpp'.

 The right side shows a schematic diagram of four channels (Channel 0-3). Each channel has an input (URX2p/n, UTX2p/n, UTX1e/n/p, URX1e/n/p) and an output (DRX2p/n, DTX2p/n, DTX1e/n/p, DRX1e/n/p). Each channel contains an 'EQ' block and a 'Driver' block. The EQ blocks are color-coded: Channel 0 (red), Channel 1 (teal), Channel 2 (blue), and Channel 3 (grey). Each channel also has an 'EQ_SEL' dropdown menu on the right side.

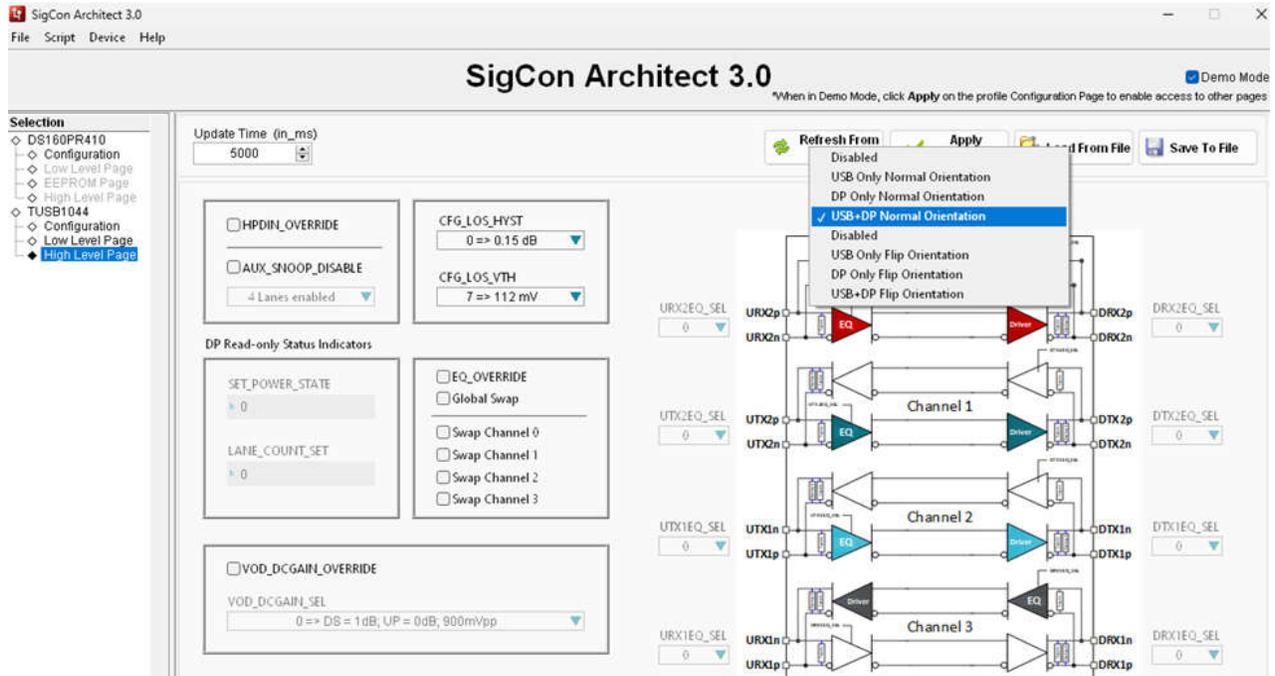
1. Select the right application mode form the menu.

There are four modes to select:

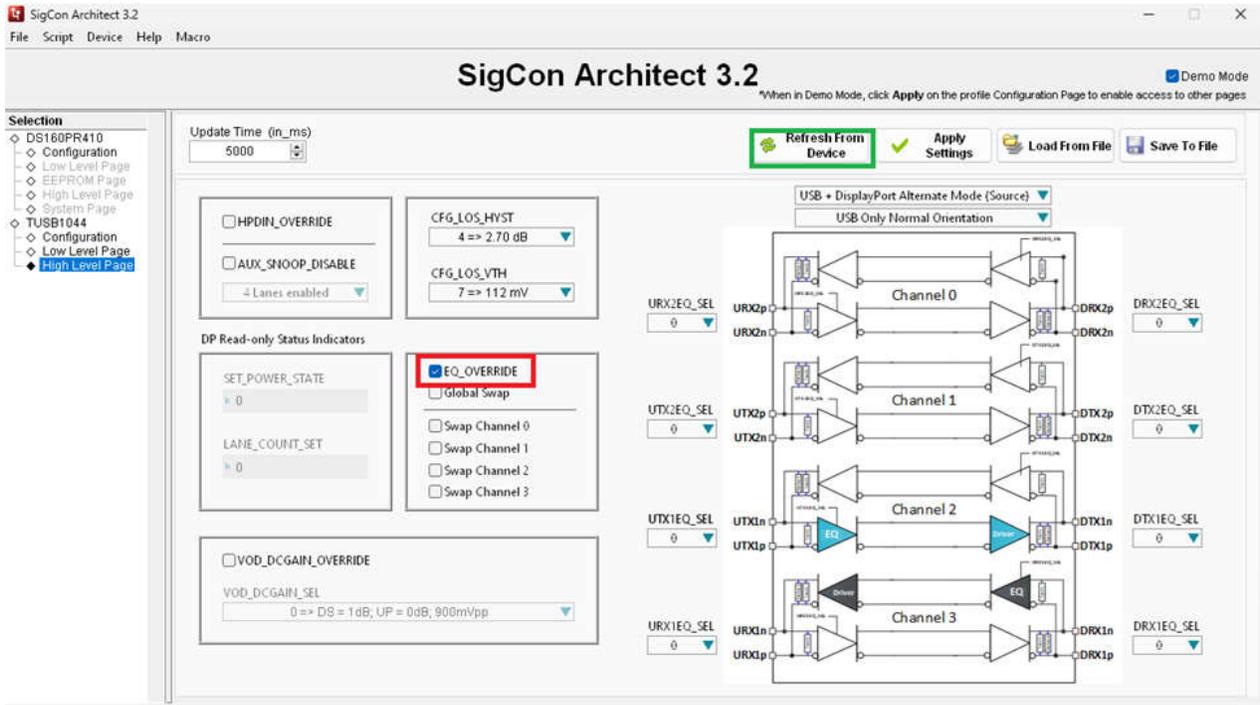
- USB + DisplayPort Alternate mode for Source
- USB + DisplayPort Alternate mode for Sink
- USB + Custom Alternate mode for Source
- USB + Custom Alternate mode for Sink



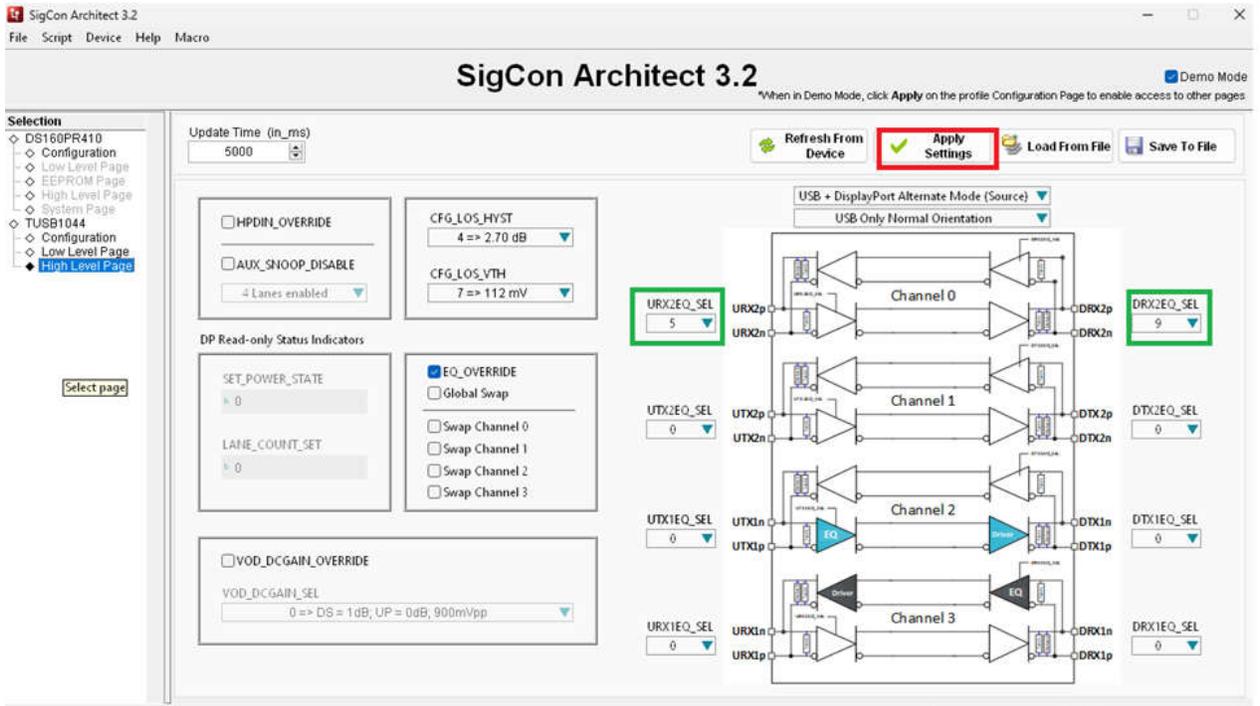
2. Select either the normal orientation or flip orientation.



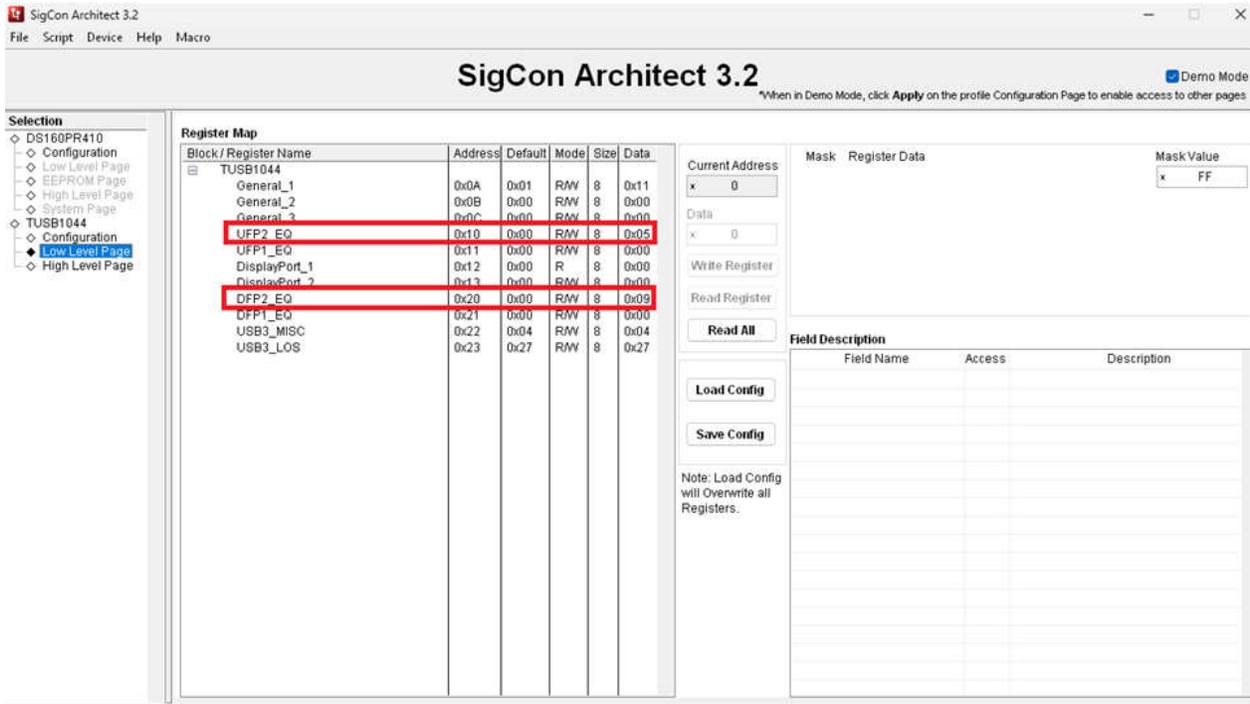
- Select the EQ_OVERRIDE checkbox and click the **Refresh From Device** button. You can then change the EQ setting for your desired channel.



- After the EQ setting change, click the **Apply Setting** button to update the EQ setting to the register.



- Go back to Low Level page to see the updated register.



SigCon Architect 3.2 *When in Demo Mode, click **Apply** on the profile Configuration Page to enable access to other pages

Selection

- DS160PR410
 - Configuration
 - Low Level Page
 - EEPROM Page
 - High Level Page
 - TUSB1044
 - Configuration
 - Low Level Page**
 - High Level Page

Register Map

Block / Register Name	Address	Default	Mode	Size	Data
TUSB1044					
General_1	0x0A	0x01	R/W	8	0x11
General_2	0x0B	0x00	R/W	8	0x00
General_3	0x0C	0x00	R/W	8	0x00
UFP2_EQ	0x10	0x00	R/W	8	0x05
UFP1_EQ	0x11	0x00	R/W	8	0x00
DisplayPort_1	0x12	0x00	R	8	0x00
DisplayPort_2	0x13	0x00	R/W	8	0x00
DFP2_EQ	0x20	0x00	R/W	8	0x09
DFP1_EQ	0x21	0x00	R/W	8	0x00
USB3_MISC	0x22	0x04	R/W	8	0x04
USB3_LOS	0x23	0x27	R/W	8	0x27

Current Address: x 0
Mask: x FF
Register Data: x 0

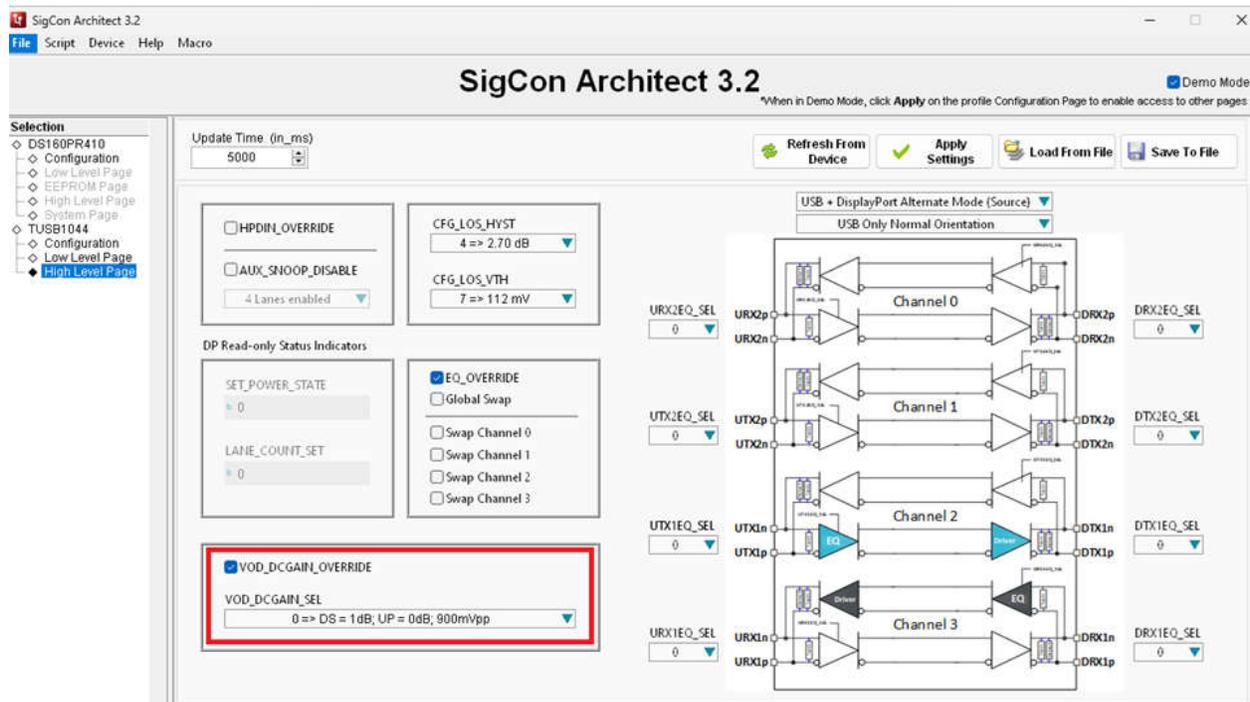
Field Description

Field Name	Access	Description

Buttons: Read All, Load Config, Save Config

Note: Load Config will Overwrite all Registers.

- Select the VOD_DCGAIN_OVERRIDE checkbox and select a DC gain setting in the drop-down list.



SigCon Architect 3.2 *When in Demo Mode, click **Apply** on the profile Configuration Page to enable access to other pages

Selection

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 - Configuration
 - Low Level Page
 - EEPROM Page
 - High Level Page
 - TUSB1044
 - Configuration
 - Low Level Page
 - High Level Page**

Update Time (in_ms): 5000

Buttons: Refresh From Device, Apply Settings, Load From File, Save To File

Configuration:

- HYPDIN_OVERRIDE
- AUX_SNOOP_DISABLE
- 4 Lanes enabled
- CFG_LOS_HYST: 4 => 2.70 dB
- CFG_LOS_VTH: 7 => 112 mV
- DP Read-only Status Indicators: SET_POWER_STATE: 0, LANE_COUNT_SET: 0
- VOD_DCGAIN_OVERRIDE**
- EQ_OVERRIDE
- Global Swap
- Swap Channel 0, Swap Channel 1, Swap Channel 2, Swap Channel 3
- VOD_DCGAIN_SEL: 0 => DS = 1dB; UP = 0dB; 900mVpp

Block Diagram: USB + DisplayPort Alternate Mode (Source) - USB Only Normal Orientation. Shows Channel 0, Channel 1, Channel 2, and Channel 3 with various signal paths and EQ blocks.

4 References

- Texas Instruments, [TUSB1044 USB TYPE-C™ 10Gbps Multi-Protocol Bidirectional Linear Redriver data sheet](#)

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