Application Brief

TUSB564-Q1 Configuration Guidelines

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Introduction

The TUSB564-Q1 is an automotive USB 3.1 5-Gbps Alt-mode redriver designed to enable DisplayPort Alt-mode over USB-C. This device multiplexes between USB and DisplayPort signals sent over the USB-C interface in a DisplayPort sink application. USB and DisplayPort signal amplitudes attenuate through a typical FR4 channel, placing limitations on system trace length at 5Gbps and higher data rates. A longer channel with large attenuation results in signal integrity issues at a USB or DisplayPort receiver. The TUSB564-Q1 is used to eliminate or minimize the attenuation effects of the channel to produce a compatible eye at the device receiver. Attenuation is minimized by applying receiver equalization to compensate for cable and board loss due to intersymbol interference (ISI) and insertion loss. The TUSB564-Q1 is configurable with 16 receiver equalization settings for USB signals and 16 equalization settings for Displayport signals.

Device Features

Equalization Selection

The TUSB564-Q1 used in a device application enables the system to pass USB 3.1 Gen 1 transmitter and receiver compliance, as well as DisplayPort receiver compliance. The TUSB564-Q1 recovers incoming data by applying equalization that compensates for channel loss, typical FR4 channel loss is provided in Table 1. Base the equalization on the amount of insertion loss of the channel before the TUSB564-Q1 receiver (Pre-Channel). The EQ values of the USB TX, USB RX, and DisplayPort RX are set independently. The equalization selection is configured through the EQ, SSEQ, and DPEQ pins. The USB equalization values available for the TUSB564-Q1 are listed in Table 2.

Table 1. Example FR4 Trace Loss

FR4 PCB Trace Length (inches)	Loss at 2.5GHz (dB)
1	0.5
2	1
3	1.5
4	2
5	2.5
6	2.9
7	3.4
8	3.9
9	4.4
10	4.9
11	5.4
12	5.9
13	6.4
14	6.9

Table 2. USB 3.1 Equalization Settings

EQ Setting #	USB 3.1 Upstream Facing Ports			USB 3.1 Downstream Facing Ports		
	EQ1	EQ0	EQ Gain at 2.5GHz (dB)	SSEQ1	SSEQ0	EQ Gain at 2.5GHz (dB)
0	0	0	-0.7	0	0	-0.9
1	0	R	1.8	0	R	0.2
2	0	F	2.7	0	F	1.1
3	0	1	3.7	0	1	2.2
4	R	0	4.6	R	0	3.0
5	R	R	5.5	R	R	4.0
6	R	F	6.3	R	F	4.8
7	R	1	7.0	R	1	5.6
8	F	0	7.8	F	0	6.4
9	F	R	8.5	F	R	7.0
10	F	F	9.1	F	F	7.6
11	F	1	9.7	F	1	8.2
12	1	0	10.1	1	0	8.7
13	1	R	10.7	1	R	9.2
14	1	F	11.1	1	F	9.7
15	1	1	11.6	1	1	10.2

AUX Snoop

For DisplayPort Alt-mode applications, the TUSB564-Q1 snoops the AUX lines by default to determine lane count when passing video signals. AUX snooping helps to conserve power when not all four data lanes are used for DisplayPort data. Deactivate AUX snooping when the TUSB564-Q1 is in I2C mode by writing a "1" in the AUX_SNOOP_DISABLE register. While AUX snooping is inactive, manually enable the DisplayPort lanes through the DPx_DISABLE registers where x = 0, 1, 2, or 3.

TUSB564-Q1 Placement

Following the layout guidelines listed in this document enables the TUSB564-Q1 to recover a signal from a USB device up to a typical 14-inch FR4 trace. In addition, the FR4 trace from the TUSB564-Q1 to the USB connector can be up to 5 inches. These recommended maximum trace lengths assumes the device provides -3 dB of de-emphasis and has a compliant receiver that recovers the 20dB loss budgeted by the USBIF for a Type-C cable and the host or device. Maximum trace lengths are extendable by adjusting the equalization, de-emphasis, and VOD settings of a device; best settings are determined in conjunction by the user and the device manufacturer. Conversely, if a device is unable to recover the signal with the amount of budgeted loss set by the USBIF, then concessions are required in the system design, such as placement of the device.

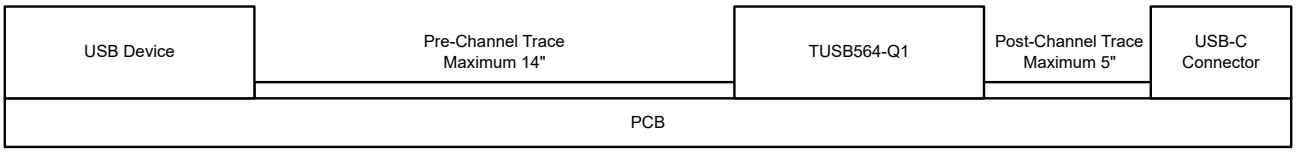

Figure 1. TUSB564-Q1 Maximum USB Trace Length Placement Example

TUSB564-Q1 Configuration Example

Figure 2 provides an example configuration of a device system using a USB3.1 Gen 1 device operating at 5Gbps and a DisplayPort 1.4 sink operating at 8.1Gbps with the TUSB564-Q1.

Using the given trace lengths in this example, the method to select the equalization values for SSTX and RX1/2 is to select the closest EQ gain available to match the trace loss and additional loss through the connector, components, and device package:

- USB device to TUSB564-Q1 SSTX = 10 inches (-4.9dB) + typical loss in Device package + capacitor (-1.5dB) = total loss of -6.4 dB. TUSB564-Q1 SSEQ setting used = Setting #8 (6.4dB).
- Type-C connector to TUSB564-Q1 RX1/RX2 = 5 inches (-2.5dB) + typical connector loss + component (-2dB) = total loss of -4.5 dB. TUSB564-Q1 EQ setting used = Setting #4 (4.6dB), TUSB564-Q1 DPEQ setting used = Setting #2 (4.4dB).

Please note that other factors such as the layout quality, device transmitter and receiver quality require adjusting the EQ settings for best performance. Use the above method to select the initial configuration values based on system board trace lengths.

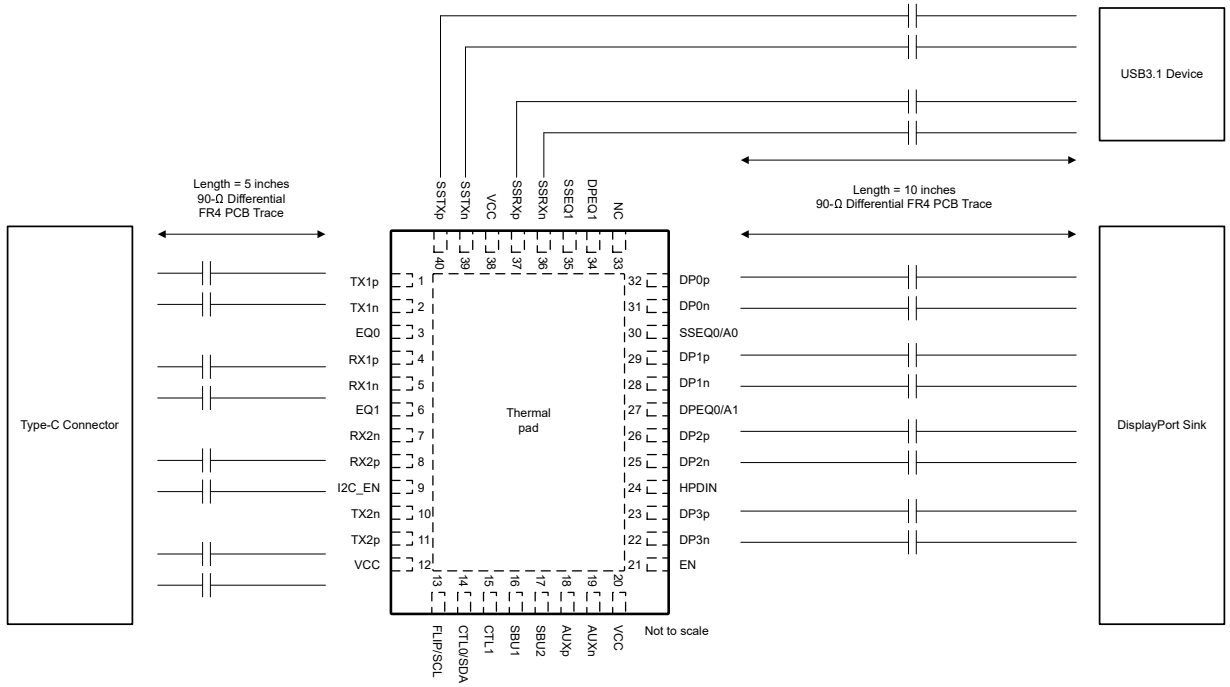

Figure 2. Device System Example

Layout Guidelines

Use the following layout guidelines in routing the high-speed USB signals to and from the TUSB564-Q1.

- Route the RXP/N and TXP/N pairs with a controlled 90-Ω differential impedance (±15%).
- Keep differential pairs away from other high-speed signals.
- Keep intra-pair routing to within 2 mils.
- Locate the differential pair length matching near the mismatch.
- Separate each pair by at least 3 times the signal trace width.
- Minimize the use of bends in differential traces. When bends are used, make the number of left and right bends as equal as possible and the angle of the bend is ≥135º. Bending the trace this way minimizes any length mismatch caused by the bends and minimize the impact bends have on the EMI.
- Route all differential pairs on the same layer.
- Minimize the number of vias to two or less.
- Keep differential traces on layers adjacent to a ground plane.
- Do not route differential pairs over any split plane.
- If using a through-hole connector, route the high-speed signals on opposite side of the connector so that the connector pin does not create a stub in the transmission line.

GND Stitching

The entirety of any high-speed signal trace must maintain the same GND reference plane from origination to termination. If the same GND reference plane is not maintained, via-stitch the GND planes together to establish continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200-mils (center-to-center, closer is better) of the signal transition vias. See Figure 3 below for an example of GND stitching vias.

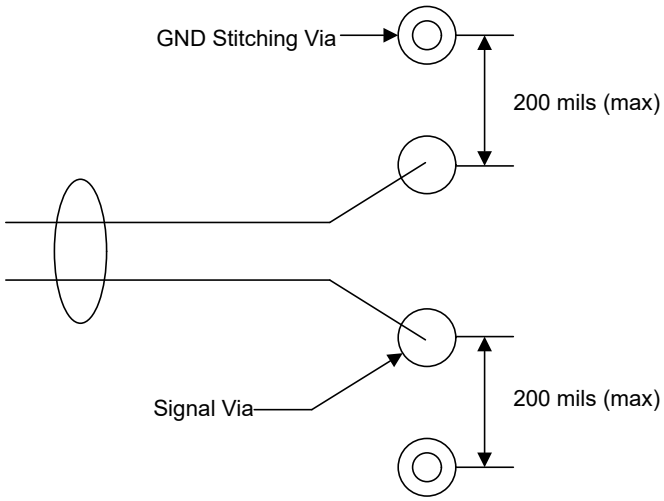

Figure 3. GND Stitching Via Example

AC Coupling and Resistor Placement

When placing AC-Coupling capacitors, the maximum component size is 0402 . During layout, on the host or device channel, place the AC-Coupling capacitors equidistant to the device and the TUSB564-Q1. On the connector to TUSB564-Q1 channel, place the AC Coupling caps close to the TUSB564-Q1 with symmetrical placement to establish top signal quality and to minimize reflections. Place the optional pull-down resistors so that the pad of the resistor shares the high-speed trace to minimize the presence of a stub. See Figure 4 for an example of the optimal AC Coupling capacitor layout symmetry.

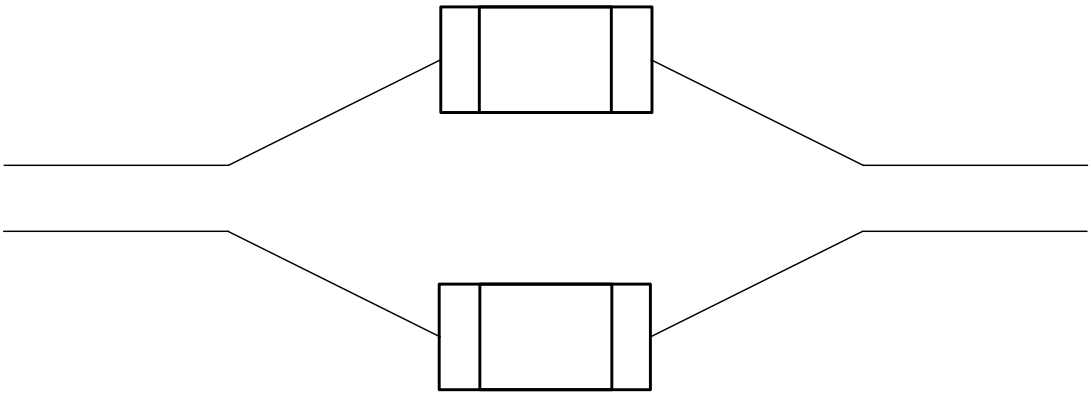

Figure 4. AC Coupling Layout Symmetry

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