Application Note

How to Dynamically Switch Between Serial and Parallel Modes Using ISO1228

Prakhar Agarwal, Andrew Jackiw

ABSTRACT

Further information on device operation is available in the *ISO1228 Eight-Channel Isolated Digital Input with Current Limit and Diagnostics*, data sheet and *ISO1228DFBEVM* EVM. This guide is used to explain the performance benefits of serial and parallel mode and how to switch dynamically between modes for the best functionality.

24V digital input systems have a growing need to support higher channel density and to integrate various features (*Space-Saving Design Techniques for Multichannel High- Voltage Digital Input Modules*). The ISO1228 address both needs as an eight-channel isolated 24V digital input receiver that can use a serial (SPI) or a parallel digital output mode to control various integrated digital features such as: wire-break detection, in-built glitch filters, field-side supply monitoring and built-in CRC across the isolation barrier. Additionally, designers can use the serial mode to monitor the inputs over SPI and reduce the number of pins in an MCU. The isolated logic side can range from 1.71V to 5.5V, supporting 1.8V, 2.5V, 3.3V, and 5V controllers. The field side supply voltage can range from 8.5V to 36V in sink mode and 13V to 36V in source mode. ISO1228 supports data rates up to 1.5Mbps, and can pass a minimum pulse width of 667ns for high-speed operation.

The ISO1228 is designed to comply with the IEC 61131-2 standard for digital inputs and supports eight channels with IEC 61131-2 Type 1, and 3 characteristics or four channels with Type 2 characteristics. The ISO1228 also includes integrated resistor-programmable current limiting and field side, input-current-powered LED indication to reduce the system's power dissipation and board temperature. ISO1228 can be configured for either sourcing or sinking type digital inputs with minimal hardware changes. The ISO1228 also supports IEC ESD and surge protection to achieve a robust design.

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1 ISO1228 - Relevant Device Information

The following ISO1228 data sheet tables and pinout are provided for reference.

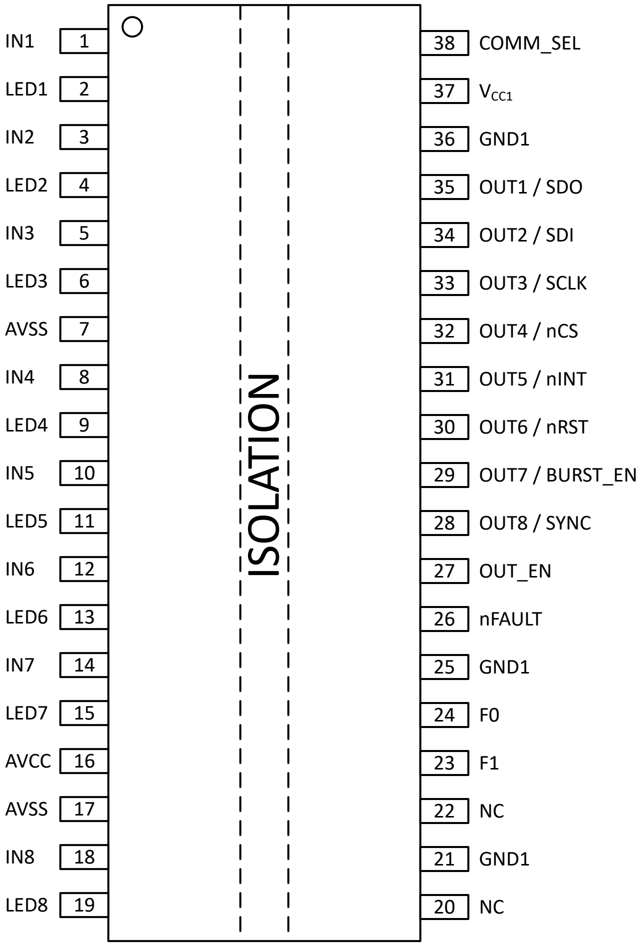

Figure 1-1. ISO1228 Pinout

Table 1-1. ISO1228 Pin Descriptions

PIN		I/O	Description
NO.	NAME		
1	IN1	I/O	Field Input, Channel 1
2	LED1	I/O	LED Indication Pin, Channel 1
3	IN2	I/O	Field Input, Channel 2
4	LED2	I/O	LED Indication Pin, Channel 2
5	IN3	I/O	Field Input, Channel 3
6	LED3	I/O	LED Indication Pin, Channel 3
7	AVSS	—	Field Side Negative Supply
8	IN4	I/O	Field Input, Channel 4
9	LED4	I/O	LED Indication Pin, Channel 4
10	IN5	I/O	Field Input, Channel 5
11	LED5	I/O	LED Indication Pin, Channel 5
12	IN6	I/O	Field Input, Channel 6
13	LED6	I/O	LED Indication Pin, Channel 6
14	IN7	I/O	Field Input, Channel 7
15	LED7	I/O	LED Indication Pin, Channel 7

Table 1-1. ISO1228 Pin Descriptions (continued)

PIN		I/O	Description
NO.	NAME		
16	AVCC	—	Field Side Power Supply
17	AVSS	—	Field Side Negative Supply
18	IN8	I/O	Field Input, Channel 8
19	LED8	I/O	LED Indication Pin, Channel 8
20	NC	—	Leave unconnected
21	GND1	—	Logic Ground
22	NC	—	Leave unconnected
23	F1	I	Digital Filter Setting
24	F0	I	Digital Filter Setting
25	GND1	—	Logic Ground
26	nFAULT	O	Open Drain Ouput. Connect 4.7 kΩ pull-up to V_{CC1}
27	OUT_EN	I	Ouput Enable. Output pins OUT1 through OUT8 are tri-stated if OUT_EN=0 or FLOAT
28	OUT8/SYNC	O	Synchronize data in Burst Mode(COMM_SEL=V_{CC1}) Data Output, Channel 8, in Parallel Interface Mode (COMM_SEL=0)
29	OUT7/BURST_EN	I/O	Burst Mode in Serial Interface Mode (COMM_SEL=V_{CC1}) Data Output, Channel 7, in Parallel Interface Mode (COMM_SEL=0)
30	OUT6/nRST	I/O	Active Low SPI Reset in Serial Interface Mode (COMM_SEL=V_{CC1}) Data Output, Channel 6, in Parallel Interface Mode (COMM_SEL=0)
31	OUT5/nINT	O	Active Low SPI Interrupt in Serial Interface Mode (COMM_SEL=V_{CC1}) Data Output, Channel 5, in Parallel Interface Mode (COMM_SEL=0)
32	OUT4/nCS	I/O	SPI Chip Seltect in Serial Interface Mode (COMM_SEL=V_{CC1}) Data Output, Channel 4, in Parallel Interface Mode (COMM_SEL=0)
33	OUT3/SCLK	I/O	SPI Clock in Serial Interface Mode (COMM_SEL=V_{CC1}) Data Output, Channel 3, in Parallel Interface Mode (COMM_SEL=0)
34	OUT2/SDI	I/O	SPI Input Data in Serial Interface Mode (COMM_SEL=V_{CC1}) Data Output, Channel 2, in Parallel Interface Mode (COMM_SEL=0)
35	OUT1/SDO	O	SPI Output Data in Serial Interface Mode (COMM_SEL=V_{CC1}) Data Output, Channel 1, in Parallel Interface Mode (COMM_SEL=0)
36	GND1	—	Logic Ground
37	VCC1	—	Logic Supply
38	COMM_SEL	I	Serial vs. Parallel Interface selection Serial Interface Mode if COMM_SEL=V_{CC1} Parallel Interface Mode if COMM_SEL=0 or Floating

Table 1-2. ISO1228 Register Map

Address	NAME	R/W	DESCRIPTION
00h	Input Data	R	Data Information: <7> = IN8 <6> = IN7 . . <0> = IN1
01h	Wire Break	R	Wire Break Information: <7> = WB8 <6> = WB7 <5> = WB6 . . <0> = WB1
02h	Fault	R	Provides the details of the faults in the design: <7> = WB (Any channel shows WB) <6> = OT (Over-temperature threshold is crossed) <5> = Reserved <4> = CRC (Inter-die CRC is in error) <3> = Reserved <2> = Field Side Power Loss <1> = Reserved <0> = UVLO (MCU Side)
03h	Filter Ch 1 and Ch 2	R/W	<7> = Filt Enable, Ch 1 <6:4> = Filter Settings, Ch 1 <3> = Filt Enable, Ch 2 <2:0> = Filter Settings, Ch 2
04h	Filter Ch 3 and Ch 4	R/W	<7> = Filt Enable, Ch 3 <6:4> = Filter Settings, Ch 3 <3> = Filt Enable, Ch 4 <2:0> = Filter Settings, Ch 4
05h	Filter Ch 5 and Ch 6	R/W	<7> = Filt Enable, Ch 5 <6:4> = Filter Settings, Ch 5 <3> = Filt Enable, Ch 6 <2:0> = Filter Settings, Ch 6
06h	Filter Ch 7 and Ch 8	R/W	<7> = Filt Enable, Ch 7 <6:4> = Filter Settings, Ch 7 <3> = Filt Enable, Ch 8 <2:0> = Filter Settings, Ch 8

2 Parallel and Serial Output Modes

ISO1228 can be configured in either serial or parallel mode to communicate with an MCU or controller. The COMM_SEL pin (pin 38) selects either serial or parallel mode as shown in the Table 2-1:

Parallel communication mode provides the fastest throughput since each input channel is directly available at the corresponding logic output (pins 35 to 28). However, the serial communication mode enables additional control features of ISO1228, such as reading device inputs, setting digital filters for individual inputs and identifying and clearing system faults (field power loss, wire-break detection, CRC errors, and so on). The MCU can access the digital control registers through SPI read and write commands.

Table 2-1. COMM_SEL (Pin 38) - Communication Mode Selection Table

COMM_SEL = Logic High	ISO1228 in serial communication mode using SPI
COMM_SEL = Logic Low	ISO1228 in parallel communication mode

Some applications can choose to switch between operational modes to take advantage of the higher throughput of parallel mode and the fault detection and control features of serial mode for a more robust system. A system example can use the following sequence:

1. Start in serial mode (COMM_SEL = 1) to configure input registers on power-up
2. Configure individual filters for each channel by writing to register addresses 03h to 06h
3. Change to parallel mode for higher throughput and less prop delay on OUTx (COMM_SEL=0)
4. Monitor the nFAULT pin’s state for any fault condition (nFAULT = 0 when a fault occurs)
5. Change to serial mode if a fault is detected (COMM_SEL=1)
6. Read fault register (02h) and wire break register (01h) to identify the fault condition. Reading the fault register can clear the nFAULT flag if the cause of the fault is no longer present
7. Return to parallel mode once faults are cleared (COMM_SEL = 0)

The following sections explains the proper timing needed to switch between modes and make glitch-free transitions.

3 Switching Communication Modes During Operation

3.1 Parallel to Serial

A parallel to serial mode transition needs to be executed as shown in the following when starting in parallel mode (COMM_SEL = 0):

1. Make sure that all MCU pins connected to the output pins of the ISO1228 (pins 35 to 28) are tristated.
2. Switch COMM_SEL = 1 to transition from parallel to serial mode. The ISO1228 can also tristate the OUTx pins needed for SPI (pins 35 to 32) until the mode switch is complete.
3. Wait for a minimum of 30ns to allow IO buffers to change from output mode to serial mode glitch-free
4. Drive nRST=0 (pin 30) for a minimum of 35ns to allow a full reset of the SPI logic inside ISO1228
5. Release nRST = 1 and wait for a minimum of 200ns
6. ISO1228 is now in serial mode.
7. Start a SPI transaction by pulling nCS = 0 (pin 32)

ISO1228 can be switched from parallel to serial mode in less than 300ns. The state of OUTx pins in this window needs to be ignored. Figure 3-1 shows the typical timing waveform for the previous steps.

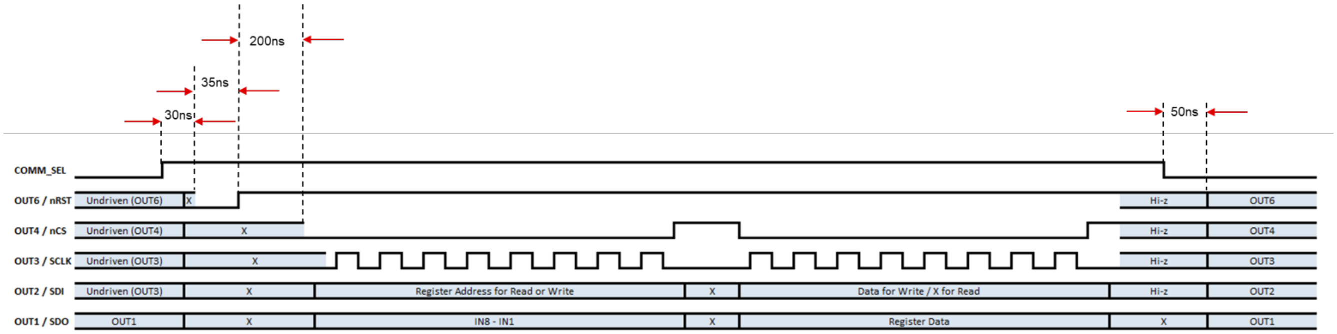

Figure 3-1. Parallel to Serial Transition Timing

3.2 Serial to Parallel

A serial to parallel mode transition needs to be executed as shown in the following when starting in serial mode (COMM_SEL = 1):

1. Make sure that all MCU pins connected to the output pins of the ISO1228 (pins 35 to 28) are tristated.
2. Set COMM_SEL = 0 to transition to parallel mode.
3. Wait for minimum 50ns to allow I/O buffers to change from SPI mode to parallel output mode cleanly
4. ISO1228 is now in parallel mode

The state of OUTx pins are undetermined during the 50ns transition period and need to be ignored. Any register configuration done while in serial mode is retained when switching to parallel mode until the device is power cycled.

4 SPI Functional Modes

The ISO1228 can operate the SPI pins in two modes controlled by BURST_EN (pin 29): Normal and Burst mode. The SYNC (pin 28) can be used for easy synchronization to the MCU which is covered in the subsequent sections.

4.1 Normal Mode

In normal SPI mode (BURST_EN = 0), ISO1228 expects 8 bits each of clock (SCLK) and data (SDI) in address phase followed by another 8 bits of SCLK and SDI in the data phase. Figure 4-1 shows the typical timing waveform for a SPI transaction on ISO1228:

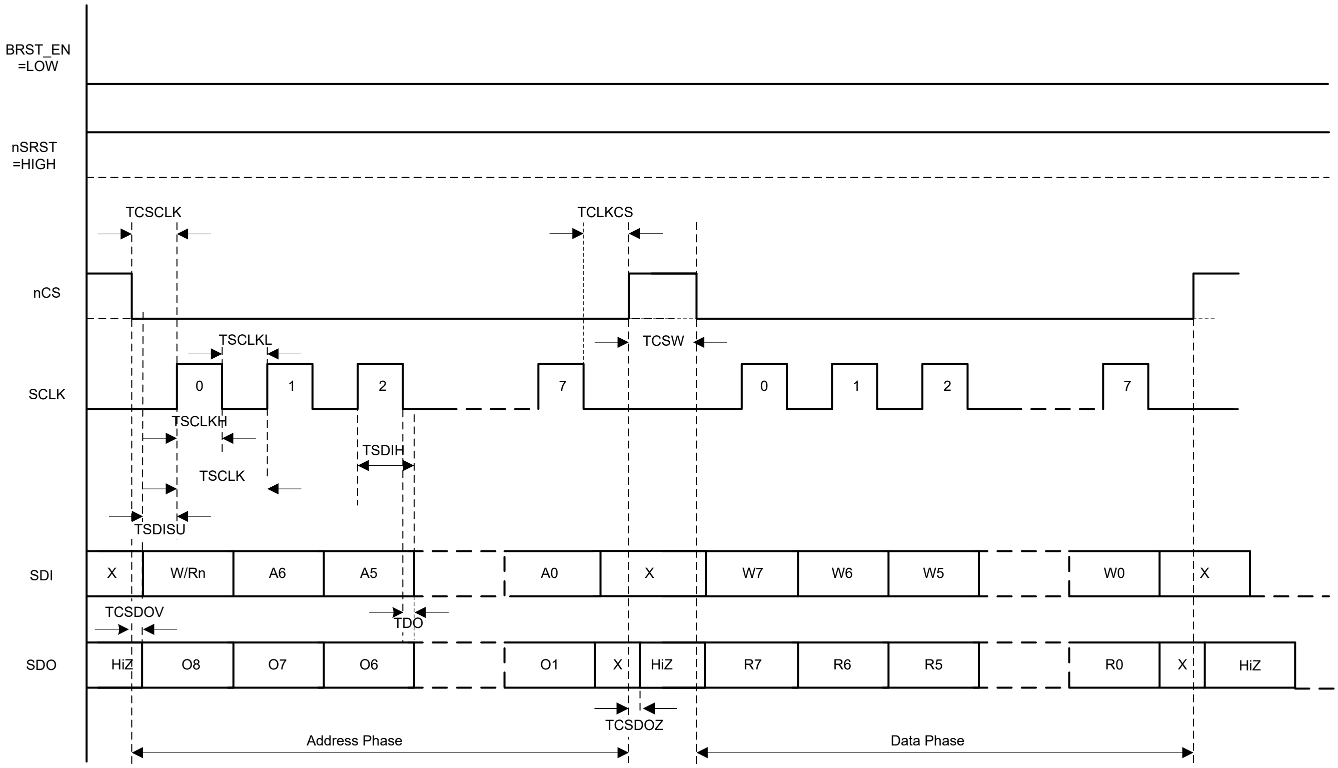

Figure 4-1. SPI Timing in Normal Mode

Due to noise or any other fault, the ISO1228 can become desynchronized from the MCU. For example, the MCU is sending bits for the data phase while ISO1228 is still in the address phase (or vice versa).

To solve this problem, the SYNC pin can be used to synchronize the MCU to ISO1228. The SYNC pin (pin 28) can change states to indicate the current phase of the ISO1228.

- When SYNC = 1, ISO1228 is in the address frame
- When SYNC = 0, ISO1228 is in the data frame and sending or receiving data bits

If the MCU detects that the MCU is out of sync with ISO1228, the MCU can read the SYNC pin and then assert low at nRST to clear ISO1228's internal registers and start a new transaction.

4.1.1 Normal Mode - Read IN8-IN1 Continuously

During the address phase of any transaction, O8-O1 is output on SDO.

If SDI is continuously held at Low (0), the device can treat this as a Read operation from Address 0. Address 0 holds the state on IN8-IN1, so in this special case of Read operation the SDO output can be IN8-IN1 in both Address and Read Phases. For applications that are only interested in the state of the digital inputs, and do not want to access other registers for Read/Write, this option can result in a simpler implementation.

Toggles are needed only on nCS and SCLK for reading the state of input pins.

4.2 Burst Mode

ISO1228 device supports Burst mode SPI operation when the BURST_EN = 1. In this mode, the outputs of the three SPI read-only registers Reg0, Reg1 and Reg2 are shifted out continuously in a circular manner on every CS toggle. The timing for this mode is shown in Figure 4-2.

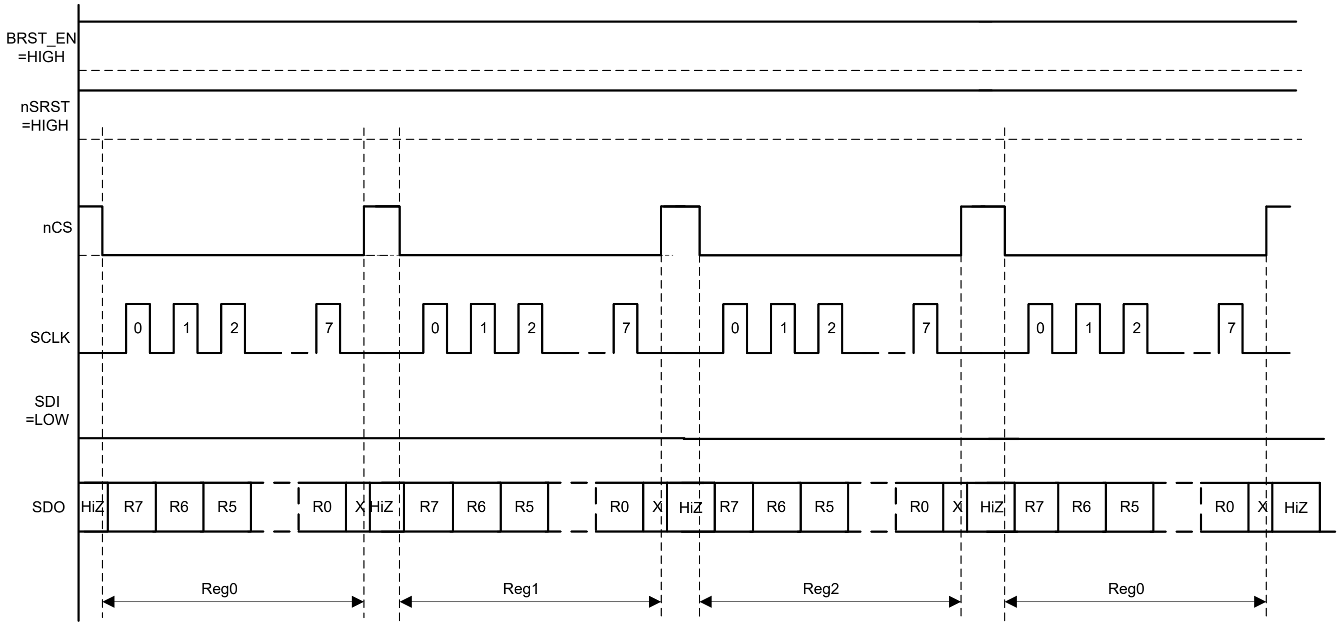

Figure 4-2. Burst Mode

This mode is an excellent choice for applications that do not want to provide address information through SDI, but want to read out information from Reg0, Reg1 and Reg2. The SYNC pin is HIGH when contents of Reg0 are being read out on SDO and LOW for Reg1 and Reg2 contents.

5 Maximum Data Throughput in Serial Mode

As described in the previous section, ISO1228 can read out two different input packets in a single SPI transaction (one during the address phase and another during the data frame).

The maximum SCLK frequency that ISO1228 supports is 25MHz (when VCC = 2.5V to 5.5V). The maximum data rate of IN8-IN1 that can be read in SPI mode without any loss of information can be calculated using the data sheet timing parameters.

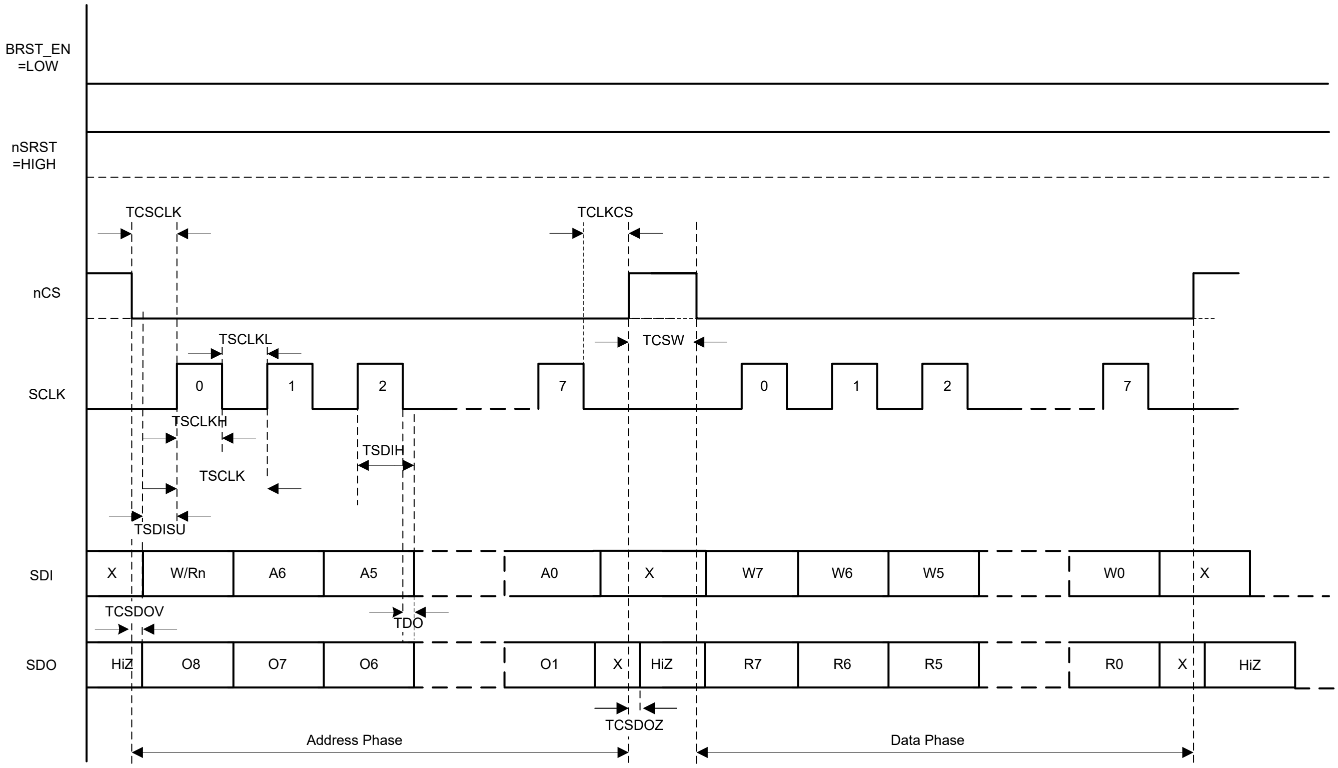

Figure 5-1. Normal mode - timing parameters

Given the data sheet specs:

- T_{CSCLK} = 20ns; the time from nCS low to SCLK first rising edge.
- T_{CLKCS} = 10ns; the time from SCLK last falling edge to nCS high.
- T_{CSW} = 250ns; Chip Select *High* Pulse Width

The time for a single frame (either address or data) can be calculated using T_{frame} = 8-SCLKbits × $T_{min\ pulse}$ = 8 × 40ns = 320ns, where $T_{min\ pulse}$ = 40ns; Minimum pulse width of SCLK at 25MHz.

The total time for one frame is **Total** = T_{CSCLK} +T_{CLKCS} + T_{CSW}+ T_{frame} = **600ns**, and the minimum pulse width on INx that can be passed through ISO1228 (T_{ui}) is 660ns. Therefore, there is not any packet loss when reading out input data using SPI.

6 Digital Low Pass Filtering of Outputs

The ISO1228 supports in-built digital low pass filters on the INx and WBx data paths. The filter value for each OUTx channel can be set individually by writing to the addresses indicated in the SPI programmable REGMAP. Alternatively a universal filter for all channels can be set using the F0/F1 device pins (pins 23 and 24). However, the filter setting in the register has the higher priority.

Filtering can be applied to OUTx data as well as wire-break data, however the filters for OUTx are programmable, while the wire-break filter value is fixed and is always ON.

If filtering is enabled (MSB = 1) on any one or more channels in the SPI registers, then register filter settings take priority. If all channels have filters disabled in the register (MSB=0), then F0/F1 takes priority. If F0/F1 = 0/0, then the filters are globally disabled.

The digital low-pass filter averaging time (TFILT) determines the averaging window for the inputs. Filters in ISO1228 are low pass filters and can be set to nine allowed levels.

Table 6-1. Low-Pass Filter Levels

F1 state	F0 state	Filter Register Setting	TFILT	Unit
F1=low	F0=low	0xxx	0	ns
F1=low	F0=float	1000	1	μs
F1=low	F0=high	1001	8	μs
F1=float	F0=low	1010	200	μs
F1=float	F0=float	1011	1	ms
F1=float	F0=high	1100	2.5	ms
F1=high	F0=low	1101	10	ms
F1=high	F0=float	1110	30	ms
F1=high	F0=high	1111	100	ms

Each filter is a saturating 3-bit counter with no resets/clears running on an internal clock. The clock period for any filter is the filter delay value divided by 8.

The counter can count the ON duration (value = 1) or OFF duration (value = 0) of each bit in OUTx across packets and assess if the duration surpasses the corresponding filter value. If this does, then only the new value can be stored into the REGMAP and communicated to the MCU. However, unlike a typical glitch filter a pulse shorter than the filter value is not completely rejected. Instead the glitch is attenuated and summed into the signal creating a low-pass response.

The clock period running a filter can be derived as FILTER_TIME/8, for example, in the previous diagram, FILTER_VALUE = 8us, for example, each pulse duration of OUTx has to exceed a min duration of 8us to be communicated to the MCU, and hence FILTER_CLK = 1MHz.

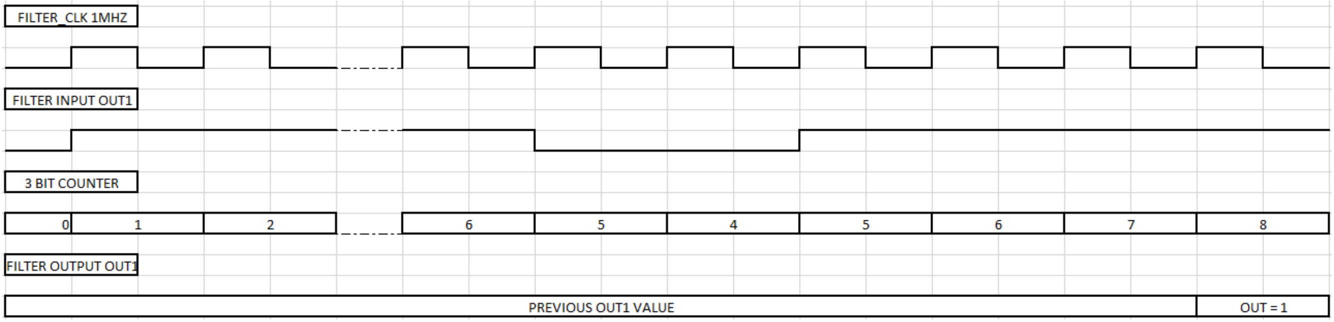

Figure 6-1. Low Pass Filter Averaging

The 3-bit counter can increment every time the counter detects a value = 1 at the filter input and can decrement when the counter detects a value = 0. As shown, the counter has counted up till 6, because the unfiltered OUT1 is 1 for 6us, next on the falling edge of OUT1, the counter decrements to 4, as the input stays low for 2us. All this while the filter output retains the previous value. After this, when OUT1 rises to 1 and stays high for 4 more cycles, the counter reaches value = 8 and the filter output updates to value = 1.

7 Summary

The ISO1228 is a powerful and feature packed tool that can create a robust design of an 8-channel isolated digital input application. The serial SPI modes can be operated in normal, burst, and continuous SPI modes that can be used to fit the system needs. The ISO1228 also has in-built glitch filters and a fault register to prevent and protect the system from various errors. ISO1228 can also switch to parallel output mode for faster data throughput when the fault is cleared.

8 References

- Texas Instruments, *ISO1228 Eight-Channel Isolated Digital Input with Current Limit and Diagnostics*, data sheet
- Texas Instruments, *ISO1228DFBEVM ISO1228 Evaluation Module for 8-Channel Isolated Digital Inputs in Sink Mode*
- Texas Instruments, *Space-Saving Design Techniques for Multichannel High- Voltage Digital Input Modules*, application brief.

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