Application Note

Migrating From Using HD3SS460 to TMUXHS4446

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ABSTRACT

This application note explains how to upgrade from using HD3SS460 to using TMUXHS4446 in a design. The document also highlights the key differences between HD3SS460 and TMUXHS4446.

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Trademarks

1 Introduction

HD3SS460 is a 4:6 passive mux that bi-directionally routes high-speed signals. HD3SS460 supports USB Type-C and Alternative Mode signals, as well any high-speed interface applications with common mode voltage range of 0-2 V and differential signaling with differential amplitude up to 1800 mVpp. Typical applications for HD3SS460 include PC and notebooks, tablets, docking stations, monitors, and more.

Due to increasing data rates and higher bandwidth requirements, in the spring of 2024, TI released TMUXHS4446, an upgrade to HD3SS460 supporting two times the bandwidth, a wider temperature range, lower power consumption, and stronger supply continuity. In addition, while the only control interface of HD3SS460 is GPIO, TMUXHS4446 is controllable through either GPIO or I2C.

To understand the differences between HD3SS460 and TMUXHS4446, including both improvements and additions, see Table 1-1.

Table 1-1. Parameter Comparison

Device	TMUXHS4446	HD3SS460
Data Rate Support	**10 Gbps**	5 Gbps
-3dB BW (relative to DC)	**10 GHz**	4.2 GHz
IL at 5 Ghz	**-1.8dB**	5 GHz not supported
RL at 5 GHz	**-15dB**	5 GHz not supported
Xtalk at 5 Ghz	**-45dB**	5 GHz not supported
Off Isolation at 5 GHz	**-21dB**	5 GHz not supported
Active power consumption	**340 µA**	600uA
Shutdown power consumption	**0.7 uA**	1uA
Supply voltage	3.3 V	3.3 V
IO voltage support	**1.8 or 3.3V**	3.3 V
Control interface	**I2C or GPIO**	GPIO
Temp support	**-40 to 105°C**	-40 to 85°C
Package	3x6mm	2.5x4.5mm
Die size	**0.8x2.4mm target (LBC9)**	1.14x1.68 mm (Bicom3ZL)
Multisource design	**Yes**	No

2 Migrating from TI HD3SS460 to TMUXHS4446

The following sections provide the necessary information explaining how to migrate from using HD3SS460 to TMUXH4446 in a design. Both pinout and package differences required design changes. Protocol differences between HD3SS460 and TMUXHS4446 are important as these improvements can change system implementation.

2.1 Pinout Differences

Table 2-1 includes the pin out differences between HD3SS460 QFN (RHR) (28) and HD3SS460 QFN (RHR) (30), and TMUXHS4446 QFN (RET) (40). TMUXHS4446 has additional unique pins due to the addition of the option to use I2C as the control interface, and these pins are described in Table 2-2.

Table 2-1. Pinout Differences

HD3SS460			TMUXHS4446		Description
Name	Pin		Name	Pin	
	RHR	RHN			
VCC	22	23	VCC	4, 7, 10, 23, 26, 29, 32	Power
GND	PAD	13, 28, PAD	GND	15, 18, 37	Ground
POL	3	3	-	-	Provides MUX control
AMSEL	8	8	-	-	Provides MUX configurations
EN	17	18	-	-	Enable signal; also provides MUX control
CRX1p,n	1, 2	1, 2	CRX1p,n	25, 24	Connector-side, high speed differential ± signals for USB-C RX/TX pins
CTX1p,n	4, 5	4, 5	CTX1p,n	28, 27	Connector-side, high speed differential ± signals for USB-C TX/RX pins
CRX2p,n	6, 7	6, 7	CRX2p,n	34, 33	Connector-side, high speed differential ± signals for USB-C RX/TX pins
CTX2p,n	9, 10	9, 10	CTX2p,n	31, 30	Connector-side, high speed differential ± signals for USB-C TX/RX pins
LnAn,p	15, 16	16, 17	DP0n,p	40, 39	System-side, high speed differential ± signals for DisplayPort DP0
LnBn,p	18, 19	19, 20	DP1n,p	3, 2	System-side, high speed differential ± signals for DisplayPort DP1
LnCn,p	20, 21	21, 22	DP2n,p	6, 5	System-side, high speed differential ± signals for DisplayPort DP2
LnDn,p	23, 24	24, 25	DP3n,p	9, 8	System-side, high speed differential ± signals for DisplayPort DP3
SSTXn,p	25, 26	26, 27	SSTXn,p	12, 11	System-side, high speed differential ± signals for USB TX/RX pins
SSRXn,p	27, 28	29, 30	SSRXn,p	17, 16	System-side, high speed differential ± signals for USB RX/TX pins
CSBU1,2	11, 12	11, 12	CSBU1,2	-	Connector-side, low speed SBU signal for USB-C SBU pin
SBU1,2	13, 14	14, 15	SBU1,2	22, 21	Connector-side, low speed SBU signal for USB-C SBU pin

Table 2-2. TMUXHS4446 Additional Pins

TMUXHS4446		Description
Name	Pin	
AUXn,p	20, 19	System-side, low speed SBU signal for USB-C SBU pins
MODE0	1	Control mode selection MODE0 = 1, I2C control MODE0 = 0, GPIO or pin control through CONF[2:0]
MODE1	13	I2C logic level control (MODE0 = 1) MODE1 = 0, 1.8V I2C logic level MODE1 = 1, 3.3 V I2C logic level
CONF0	35	GPIO control (MODE0 = 0) Switch configuration control for high-speed and low-speed pins. Refer to Device Functional Modes section for details.
A1		I2C control (MODE0 = 1) Configurable I2C target address bit
CONF1	36	GPIO control (MODE0 = 0) Switch configuration control for high-speed and low-speed pins. Refer to Device Functional Modes section for details.
SCL		I2C control (MODE0 = 1) I2C clock input
CONF2	38	GPIO control (MODE0 = 0) Switch configuration control for high-speed and low-speed pins. Refer to Device Functional Modes section for details.
SDA		I2C control (MODE0 = 1) I2C data input
A0	14	I2C control (MODE0 = 1) Configurable I2C target address bit

2.2 Package Differences

Table 2-3 includes a comparison between the packages HD3SS460 and TMUXHS4446.

Table 2-3. Package Differences

Part number	Package	Body size (NOM)
HD3SS460	QFN (RHR) (28)	3.50 mm x 5.50 mm
	QFN (RNH) (30)	2.50 mm x 4.50 mm
TMUXHS4446	QFN (RET) (40)	3.0 mm x 6.0 mm

2.3 Protocol Differences

In addition to pinout and package differences, HD3SS460 and TMUXHS4446 also differ in that HD3SS460 supports USB 3.2 Gen 1 x 1 and DP 1.2, and TMUXHS4446 supports USB 3.2 Gen 2 x 1and DP 1.4.

As mentioned in Table 2-4, the loss budget for each device differs in that for HD3SS460, the loss budget depends on the type of connectors used, but for TMUXHS4446, the loss budget is a maximum of 2 3 dB no matter which connectors are used. For a visual depiction and comparison of the loss budgets of USB 3.2 Gen 1 and USB 3.2 Gen 2, see the *System Loss* topic in *USB System Design Considerations: Switches and Redrivers*, white paper.

Table 2-4 addresses the primary differences between HD3SS460 and TMUXHS4446 as related to the distinct characteristics of USB 3.2 Gen 1 x 1, DP 1.2, USB 3.2 Gen 2 x 1, and DP 1.4.

Table 2-4. Protocol Differences

Device	HD3SS460		TMUXHS4446	
Protocol	USB 3.2 Gen 1 x 1	DP 1.2	USB 3.2 Gen 2 x 1	DP 1.4
Speed	5Gbps	5.4Gbps	10Gbps	8.1Gbps
Loss budget	Different for each connector		23 dB for all connectors	

As evidenced by the ability to support USB 3.2 Gen 2 and DP 1.4, TMUXHS4446 offers customers a design that enables higher bandwidth and a more robust loss budget.

3 PCB Layout Recommendations

Due to the sensitive nature of high-speed signals, there are specific layout recommendations that must be followed to preserve signal integrity. These layout recommendations are consistent for HD3SS460 and TMUXHS4446. The most important high-speed layout recommendations are as follows:

1. Minimize the trace length to prevent channel loss.
2. Match the signal length for positive and negative parts of differential signals.
3. Minimize the number of VIAS to prevent loss.

For a comprehensive guide covering high-speed layout recommendations, see the *High-Speed Interface Layout Guidelines* application note.

4 Summary

The migration from using HD3SS460 to using TMUXHS4446 in your design requires understanding the pinout, package, and protocol differences between HD3SS460 and TMUXHS4446. TI recommends the migration from HD3SS460 to TMUXHS4446 because TMUXHS4446 supports higher data rates, offers improved electrical performance, and provides stronger supply continuity.

5 References

- Texas Instruments, *USB System Design Considerations: Switches and Redrivers*, white paper.
- Texas Instruments, *High-Speed Interface Layout Guidelines*, application note.

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