Technical White Paper

Reduce System Design Time and Cost with Flexible RS-485 Transceivers

Vikas Kumar Thawani, Mani Bhushan Ray

ABSTRACT

RS-485 has been the most used wired communications interface in industrial applications for more than two decades now. Balanced differential signaling of RS-485 allows for rejection of common mode noise and facilitates communications over long distances in noisy industrial environments. RS-485 is a common communications port in most industrial applications such as factory automation, protection relay, solar inverter, energy meter, motor drives and building automation.

Based on the needs of the end-equipment, RS-485 networks have to be designed for different bus supply, logic interface supply voltage, network length and throughput. As a result, customers have to select, test and qualify multiple RS-485 transceivers available in the market to meet unique application requirements. Additionally, system designers develop different printed circuit boards (PCBs) for end nodes and middle nodes in a network because the end nodes usually require termination resistor to improve signal quality. This process consumes significant design bandwidth and resources, increasing the system design time and cost and delaying the time to market.

THVD1424 provides the flexibility to system designers to use the same device at any node location (end-node and middle-node) in any network, two wire (half duplex) or four wire (full duplex), slow or fast. Thus, by using THVD1424, a common PCB can be designed and configured via software for various application needs, saving considerable development time and effort.

Table of Contents

Trademarks

1 Typical RS-485 Networks and the Need for Termination

Figure 1-1 and Figure 1-2 illustrate typical RS-485 networks in either half-duplex or full-duplex configurations, respectively. In these topologies, the participating drivers, receivers, and transceivers connect to a main cable trunk via network stubs. A stub is the electrical distance between a transceiver and cable trunk, and essentially represents a non-terminated piece of bus line.

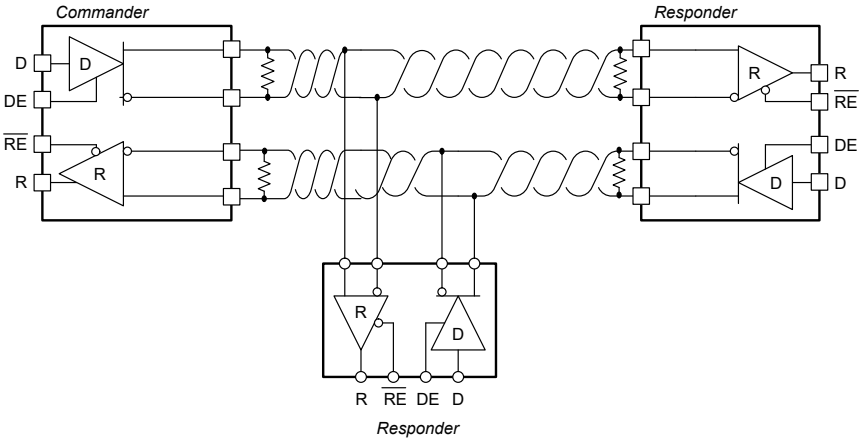


Figure 1-1. Full-Duplex Network

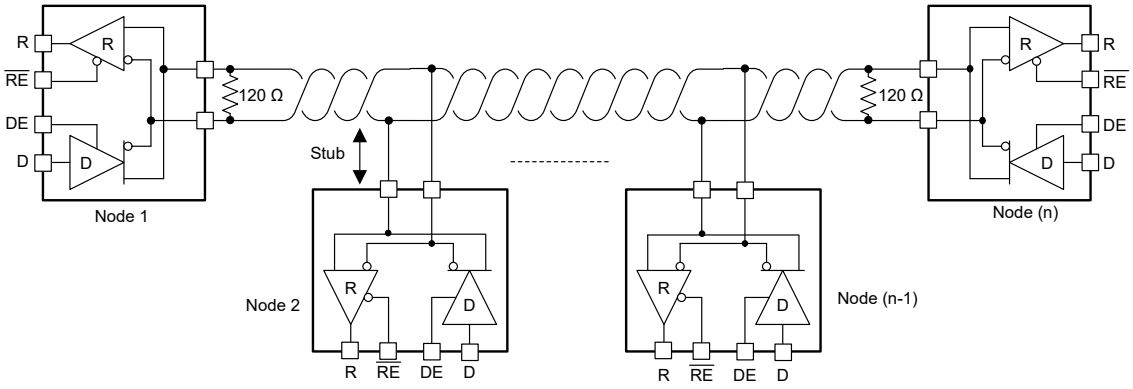


Figure 1-2. Half-Duplex Network

The full-duplex implementation requires two signal pairs (four wires), and full-duplex transceivers with separate bus access lines for transmitter and receiver. Full-duplex network allows a node to simultaneously transmit data on one pair while receiving data on the other pair- thus achieving high effective throughput. In half-duplex network, only one signal pair is used, requiring the driving and receiving of data to occur at different times. This configuration reduces the network cabling cost (compared to full-duplex network) at the expense of reduced throughput.

Most RS-485 transceivers available in the market are either half-duplex or full-duplex, meaning devices are in different pinout and packages. This is the first problem for system designers to select different devices for their half-duplex and full-duplex design platforms.

Electrical signal travels in the copper cable (physical medium) from the driver to all receivers on the network. While driving the network, the driver (TX) output impedance is low, whereas the receiver's (RX) input impedance is typically in kiloohms (kΩ). As shown in image below, every time the signal encounters impedance mismatch such as stubs of the middle nodes (at points A and B) or receiver input terminals (at Node n), some amount of signal is reflected back which interferes with the signal on the bus degrading the signal quality. Reflection factor (r) is given by Equation 1.

$$r = (Zt - Zo) / (Zt + Zo) \quad (1)$$

where Zt is the terminating impedance and Zo is the cable characteristic impedance

As per the transmission line theory, it is vital that the impedance mismatch discontinuities are limited to minimize reflections. To achieve this, recommended design practice is to keep stub lengths to a minimum and terminate the farthest node. If the signal can travel in both directions, both far ends of the network need to be properly terminated.

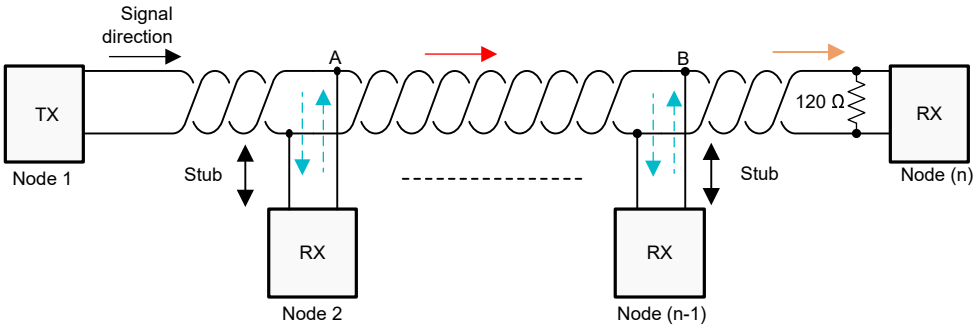


Figure 1-3. Signal Reflection Phenomena in an RS-485 Network

Bus termination is an effective method to improve signal quality. As shown Figure 1-1 and Figure 1-2, typically both end nodes are terminated with termination resistors whose value matches to the characteristic impedance of the transmission cable. In certain applications such as in building automation (HVAC, Thermostats, and so on), nodes can be added or removed from the RS-485 network to reconfigure it. This leads to second and third problem for system designers- application boards for end nodes have to be designed differently than the middle nodes, and a technician needs to manually intervene to re-configure the termination in network, which is prone to human errors such as inverting the polarity of the cable, improper termination, and so on.

2 Network Length, Data Rate, and Stubs

RS-485 standard provides guideline for selecting maximum operational data rate and network length as shown in Figure 2-1.

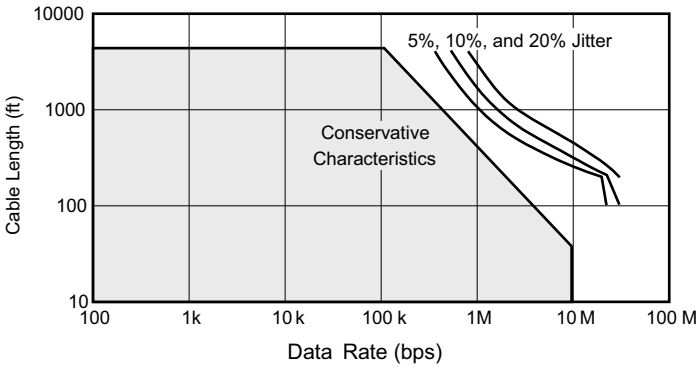


Figure 2-1. Cable Length vs Data Rate Characteristics

Figure 2-1 shows the inverse relationship between signaling rate and cable length corresponding to the tolerable jitter. Solid line is a conservative estimate with almost no jitter. Network length can be extended if the system is able to tolerate higher jitter in the signal (5%, 10%, and 20% jitter curves in the diagram) while still able to distinguish high and low bits properly. At lower data rates, DC resistance of the cable limits the maximum communication distance since cable resistance attenuates the signal. As the frequency of the signal increases, AC properties of the cable and rise/fall time of the driver starts limiting the network performance of speed vs distance.

Once the network length and operational data rate for an RS-485 network is decided, next task is to decide the maximum stub length to maintain good signal quality. As a general conservative guideline, the electrical length, or round-trip delay, of a stub is recommended to be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 2.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (2)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3 × 108 m/s)
- v is the signal velocity of the cable or trace as a factor of c
- v is the signal velocity of the cable or trace as a factor of c

This leads to the fourth problem for system designers – to select different devices for their slow or fast speed network designs.

3 Discrete Design for Switchable Termination and Duplex Switching

System designers trying to design a common PCB with switchable termination resistor, so that same PCB can be used across all nodes in an RS-485 network, can use optical relay drivers, such as opto-MOS. Opto-MOS is a device that responds to a logic input signal and enables or disables a low resistance semiconductor switch. Optical isolation enables the bus to be at any common mode voltage independent of the reference of control signal. Image below shows this design and extends the idea to include switchable duplex – meaning with the use of two extra opto-MOS, a design can be built that can act as half duplex or full duplex, with termination enabled or disabled.

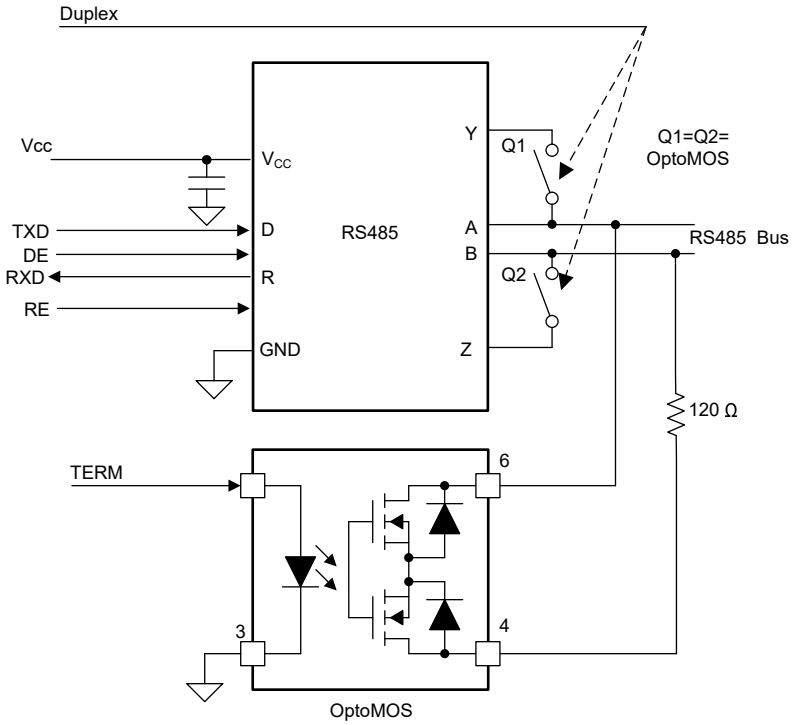
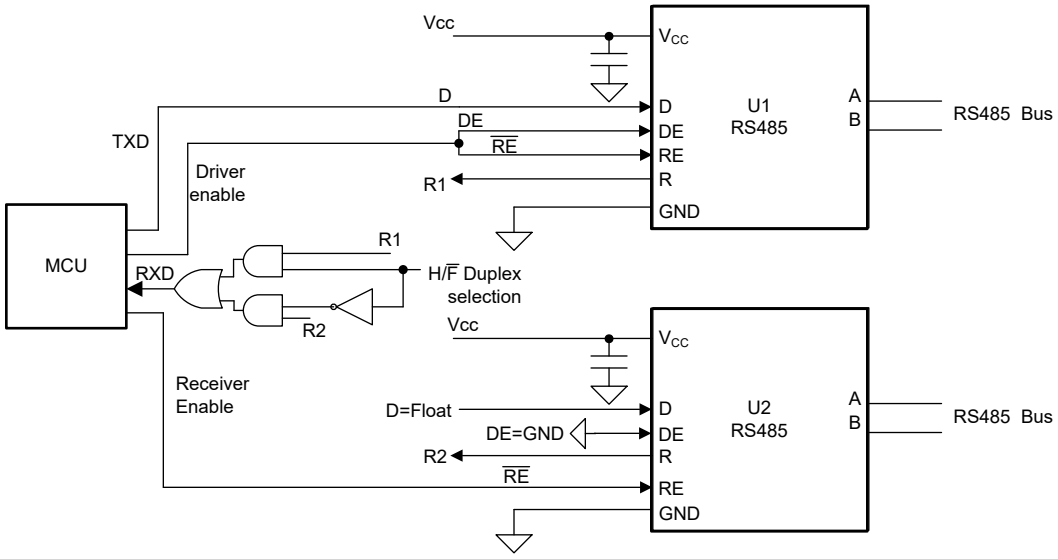


Figure 3-1. Opto-MOS Implementation for Switchable Termination and Duplex Switching

Issues with the previous design is that this occupies considerable board area and is expensive.

4 Discrete Design for Duplex Switching

Alternate discrete implementation for a design that can act as pin-controlled half duplex or full duplex is to use two half-duplex transceivers and build logic around as shown below to transmit and receive data for two-wire or four-wire networks.



Duplex Selection	RXD	U1	U2
High (half duplex)	R1	Acts as TX and RX. Driver enable signal controls it	Can be ignored for half duplex operation.
Low (Full duplex)	R2	Acts as TX	Acts as RX

Figure 4-1. Logic Implementation of Duplex Switching

Same issue with this design that this occupies considerable board area because of two RS-485 transceivers and logic gates.

5 THVD1424 and THVD1454 Flexible RS-485

All the problems described in the previous sections have one simple solution: THVD1424 and THVD1454.

Texas Instruments has released Industry's first truly flexible RS-485 transceiver. This family has two unique devices:

- THVD1424 has on-chip 120-Ω switchable termination across driver and receiver bus pins, pin-controlled duplex switching and slew rate control to enable a common device for all types of networks and at all node locations. This device can be used in half-duplex or full-duplex RS-485 networks by configuring the pin H/F. The device has slew rate control pin SLR which can be used to set the device in maximum 20-Mbps mode or slew rate limited 500-kbps mode. Termination resistors are controlled using two pins TERM_TX and TERM_RX. This device also has the ability to interface with low-voltage microcontrollers because of the presence of separate VIO pin supporting 1.65 V to 5.5 V. Bus supply voltage V_{CC} can be independent of V_{IO} and supports 3 to 5.5 V. All the features are packed in a tiny thermally efficient 16-VQFN package (3-mm x 3-mm)

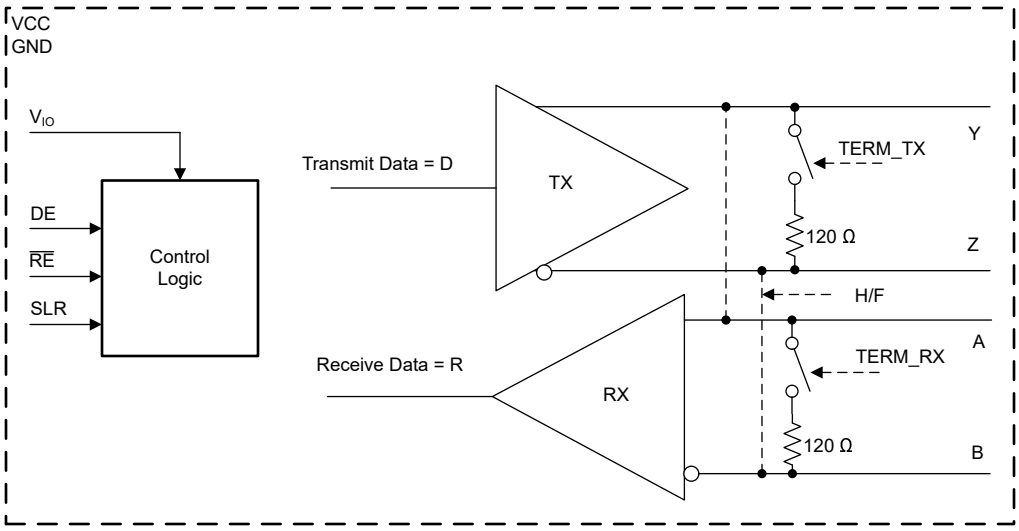


Figure 5-1. THVD1424 Block Diagram

- THVD1454 has a sub-set of features compared to THVD1424. THVD1454 is in space-saving 10-VSON package (3-mm × 3-mm) and is designed for only half-duplex networks. This device also has on-chip 120-Ω switchable termination across the bus pins and slew rate control. This device provides a excellent alternative to customers looking for pin compatibility with equivalent competition solutions.

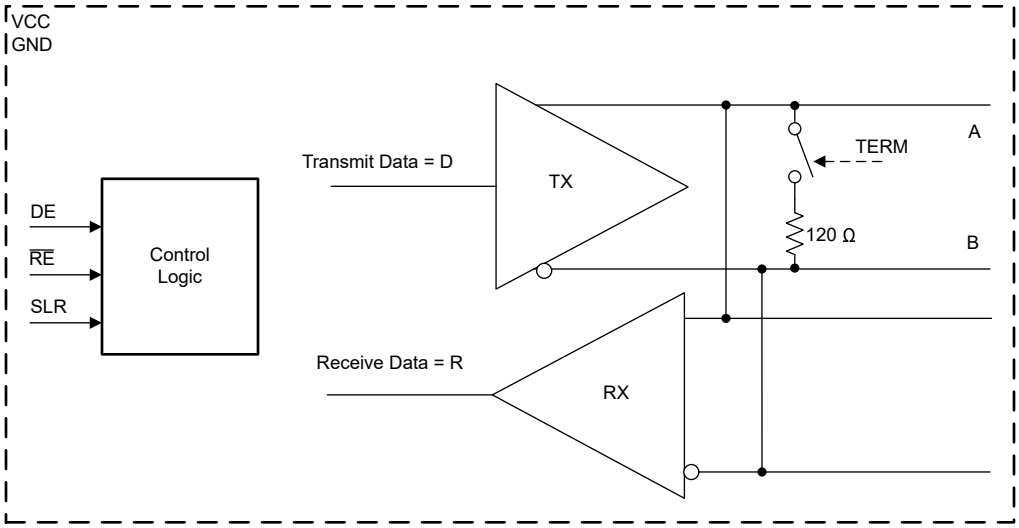


Figure 5-2. THVD1454 Block Diagram

Other unique features offered is:

Other unique features offered by both the devices are:

- Termination resistor across the bus pins can be enabled or disabled across the bus pins independent of the driver or receiver enable/disable states.
- Termination is tightly regulated over supply voltage 3 to 5.5 V, common mode voltage -7 V to 12 V and temperature -40°C to 125°C.
- The device can operate from 3.3 V or 5 V bus supply.
- Bus pins provide 1/8 unit load supporting 256 nodes on the bus.
- Failsafe receiver for bus open, short and idle conditions.
- Level 4 IEC 61000-4-2 ESD protection on bus pins: ±8 kV contact discharge/±15 kV air discharge.
- Glitch filter in receiver path for slow speed mode to filter out fast noise pulses.
- Extended industrial temperature range: -40°C to 125°C.
- Integrated protection such as bus short circuit current limiting, thermal shutdown and supply under-voltage.

6 Application Diagrams with THVD1424

Figure 6-1, Figure 6-2, and Figure 6-3 demonstrate the versatility of TI's Flexible RS-485 transceiver, THVD1424. Network diagrams highlight how THVD1424 fits for both half-duplex and full-duplex networks. Same board design is replicated at all node positions with just software configuration. This also eliminates manual intervention for termination re-configuration as it can be handled by software.

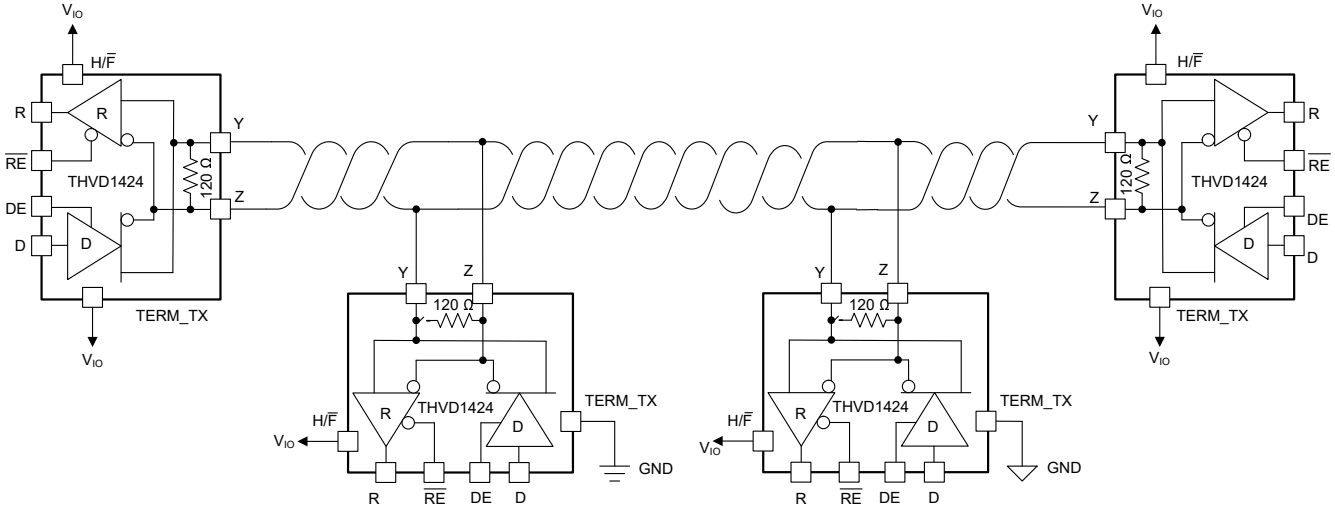


Figure 6-1. Half-duplex Network Using THVD1424

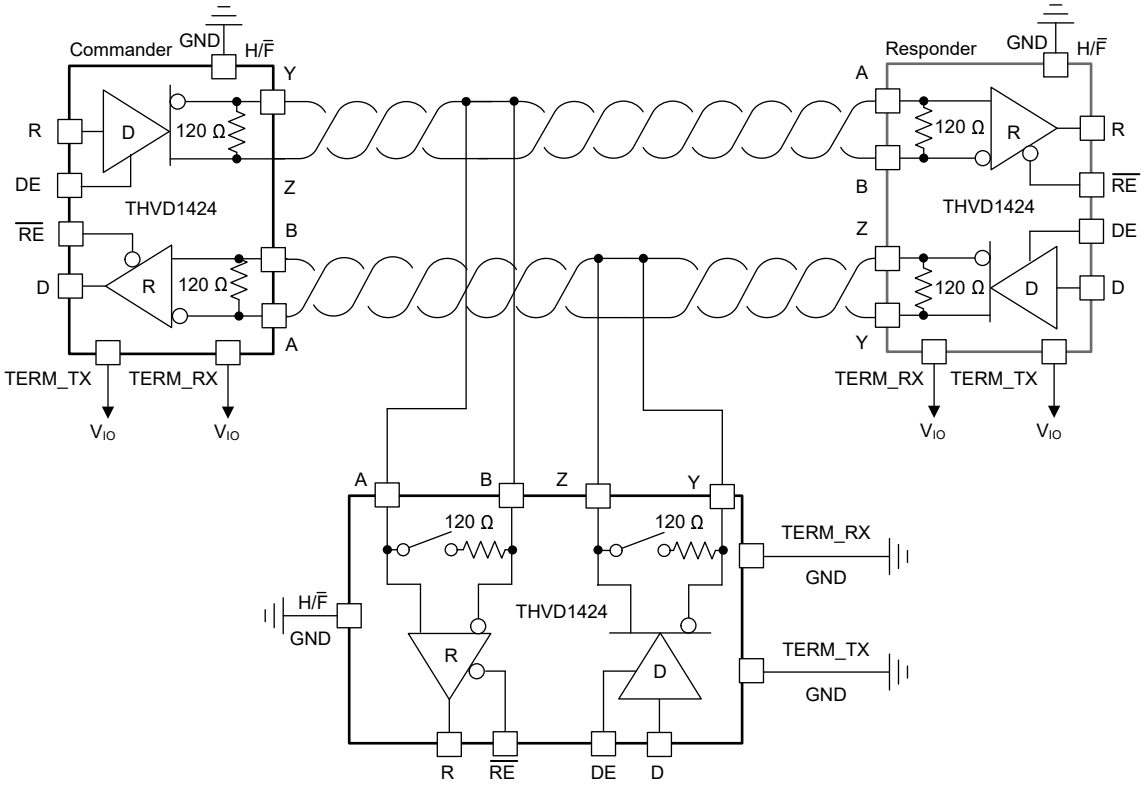


Figure 6-2. Full-duplex Network Using THVD1424

THVD1424 only needs two 1 uF bypass capacitors on supply pins, VCC and VIO, to operate, thus providing an extremely compact feature-rich design. All logic pins can be hard-wired to supply or ground and are located in sides of the package. All four bus pins are located on one side of the package to enable a flow-through layout. Three-dimensional image of device with bypass capacitors is shown in Figure 6-3.

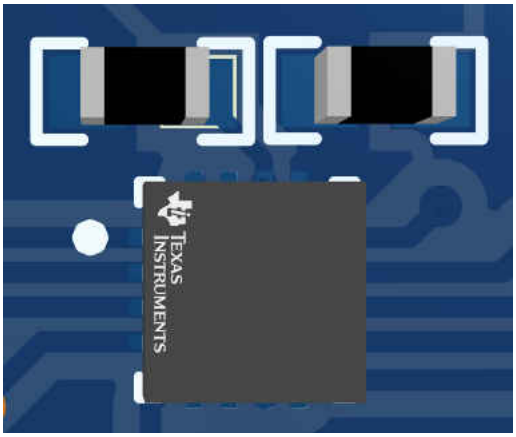


Figure 6-3. Layout Diagram of THVD1424

7 Experimental Results from Four Node Testing of THVD1424

A four-node half-duplex network was constructed using 50 feet twisted pair cabling and four THVD1424 boards connected as shown below. Ideal topology for multi-point network is daisy-chain, however the network built here is bus topology with stubs to show the impact of long stubs deteriorating the signal quality.

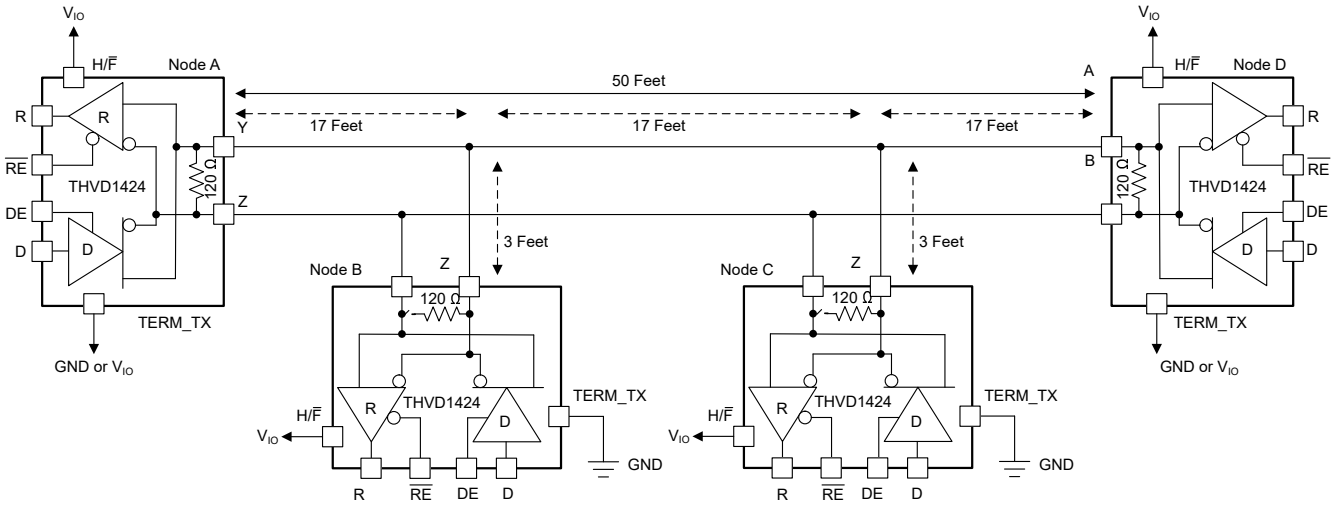


Figure 7-1. Network Set-up with THVD1424

Each node was connected to 5 V and ground was common between all nodes. Node B was driven using Function generator and bus waveforms were checked on Node A.

Case 1: Slew rate control (SLR) pin for each node was connected to ground to check the impact of termination at high speed. Node B driven at 2 Mbps

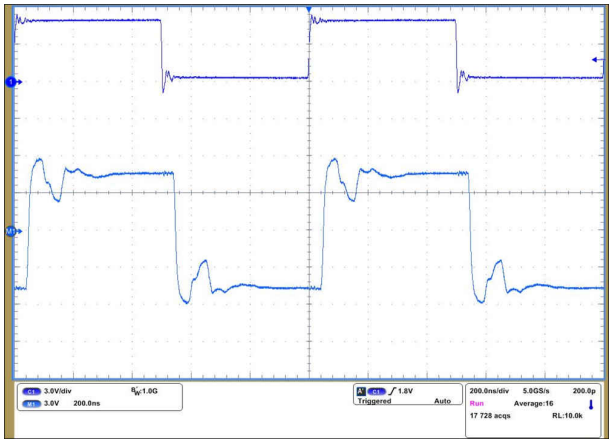


Figure 7-2. Node A and Node D Un-terminated with Signaling at 2 Mbps

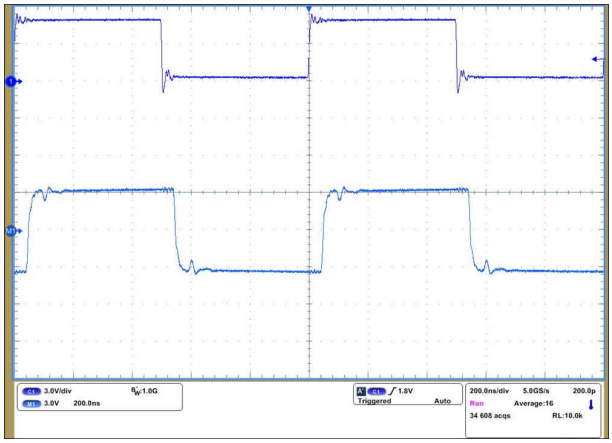


Figure 7-3. Node A and Node D Terminated with Signaling at 2 Mbps

Case 2: Node B driven at 10 Mbps

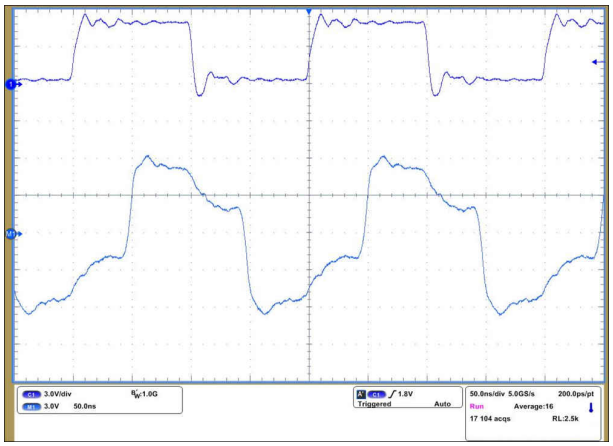


Figure 7-4. Node A and Node D Un-terminated with Signaling at 10 Mbps

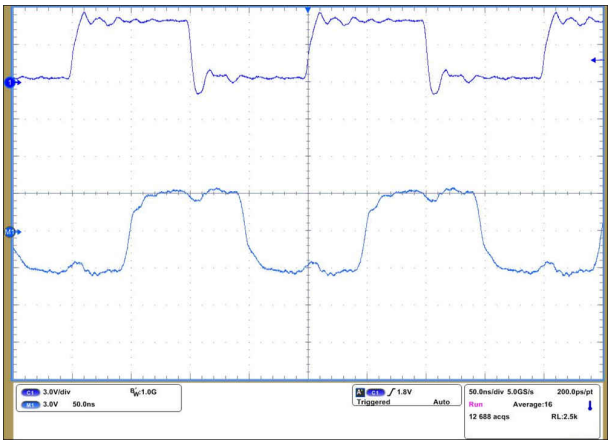


Figure 7-5. Node A and Node D Terminated with Signaling at 10 Mbps

Case 3: Node B driven at 20 Mbps

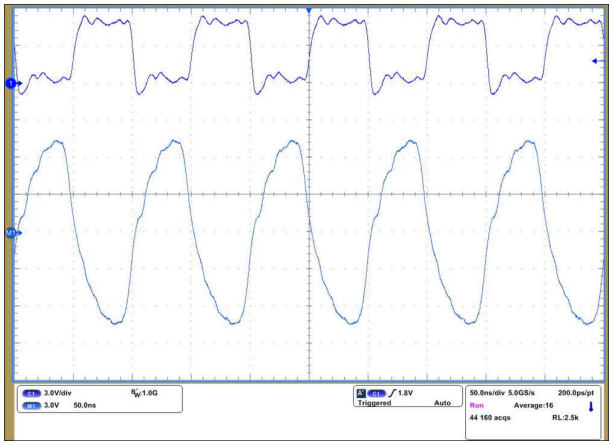


Figure 7-6. Node A and Node D Un-terminated with Signaling at 20 Mbps

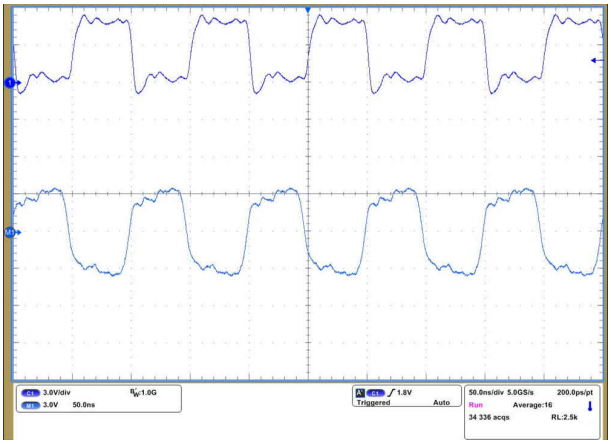


Figure 7-7. Node A and Node D Terminated with Signaling at 20 Mbps

Case 4: SLR pin was made High for all nodes and Node B was driven at 500 kbps.

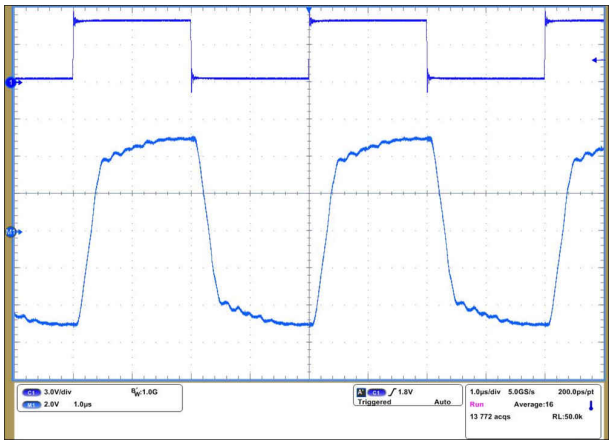


Figure 7-8. Node A and Node D Un-terminated with Signaling at 500 kbps

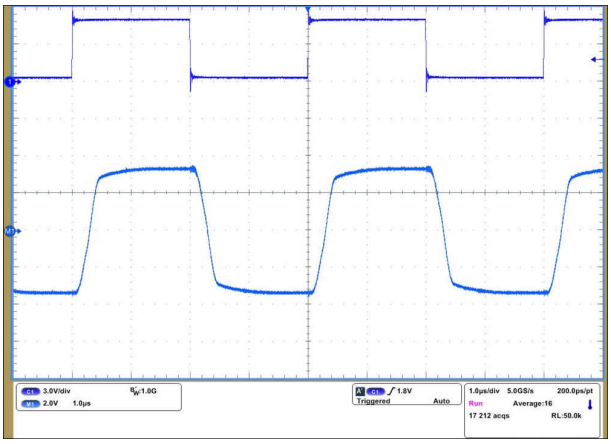


Figure 7-9. Node A and Node D Terminated with Signaling at 500 kbps

As shown from above waveforms, having both ends of the network terminated substantially improves the bus waveforms by reducing reflections. Even though 500 kbps is much slower speed and termination becomes optional at low speeds and at this distance, presence of termination still improves bus waveforms.

Please note: Terminated bus waveforms have smaller amplitude which is expected because unloaded driver differential output swings closer to supply and hence is larger than loaded driver output. Also stub length is intentionally kept longer than what would be encountered in actual networks for these transition times (~10 ns typical for driver set in 20-Mbps mode). Another note is 50-feet network length for 20 Mbps signaling rate will perform slightly worse due to AC losses of the cable, hence the waveforms even under terminated conditions are not ideal.

8 Conclusion

THVD1424 and THVD1454 devices from Texas Instruments offer a compelling solution to the common problems faced by system designers of RS-485 networks without increasing board space or solution cost. THVD1424 is first-in-industry RS-485 transceiver that provides true flexibility. Once the system designer tests and qualifies the device, it is ready to be used in all of their current and future design platforms- substantially reducing development cost, time and accelerating time-to-market. For quick evaluation, the THVD1424EVM evaluation module is available for THVD1424 and the THVD1454EVM is available for THVD1454.

9 Revision History

Changes from Revision B (March 2023) to Revision C (May 2023)	Page
• Added *THVD1454* throughout the publication	1

Changes from Revision A (January 2023) to Revision B (March 2023)	Page
• Updated the *Full-duplex Network Using THVD1424* image	8

Changes from Revision * (October 2022) to Revision A (January 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated *Full-Duplex Network* image	2
• Updated *Half-Duplex Network* image title	2

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265