Application Report

ISO7721/ISO7721-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 ISO7721/ISO7721-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1.1 Overview

This document contains information for ISO7721/ISO7721-Q1 (8-D and 16-DW package) to aid in a functional safety system design. Information provided are:

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- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

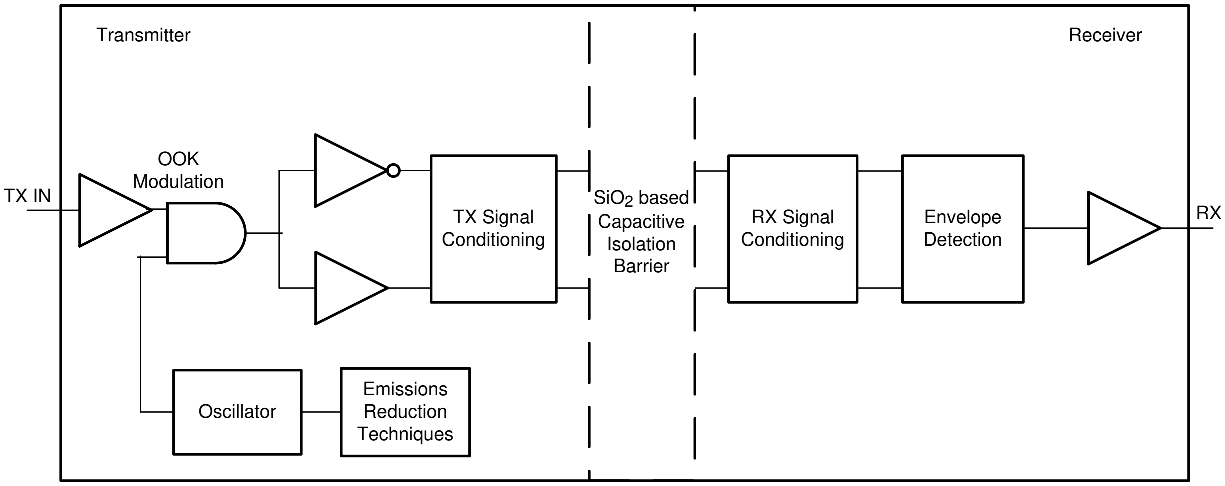

Figure 1-1. Functional Block Diagram

ISO7721/ISO7721-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

1.2 Functional Safety Failure In Time (FIT) Rates

1.2.1 8-D (narrow body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for the 8-D package of ISO7721/ISO7721-Q1 based on two different industry-wide used reliability standards:

- Table 1-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 1-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	3
Package FIT Rate	7

The failure rate and mission profile information in Table 1-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 1-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 1-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

1.2.2 16-SOIC (wide-body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for the 16-DW package of ISO7721/ISO7721-Q1 based on two different industry-wide used reliability standards:

- Table 1-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 1-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 1-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: TBD mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 1-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 1-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

1.3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISO7721/ISO7721-Q1 in Table 1-5 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 1-5. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT state undetermined	35%
OUT not in timing or voltage specification	30%
OUT stuck to default state	25%
OUT stuck high	5%
OUT stuck low	5%

The FMD in Table 1-5 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

1.4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ISO7721/ISO7721-Q1 (8-D and 16-DW package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 1-7 and Table 1-11)
- Pin open-circuited (see Table 1-8 and Table 1-12)
- Pin short-circuited to an adjacent pin (see Table 1-9 and Table 1-13)
- Pin short-circuited to supply (see Table 1-10 and Table 1-14)

Table 1-7 through Table 1-14 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 1-6. Note that when pin short to ground case is discussed, only same side ground shorts are considered.

Table 1-6. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

1.4.1 SOIC-8 Package

Figure 1-2 shows the ISO7721/ISO7721-Q1 pin diagram for the 8-D package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the ISO7721/ISO7721-Q1 datasheet.

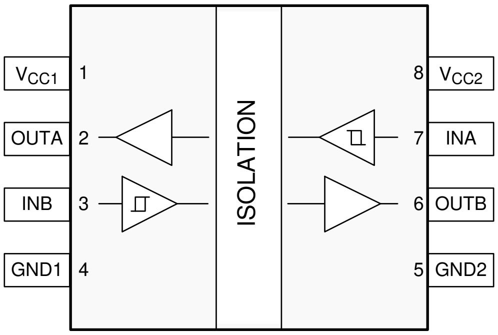

Figure 1-2. Pin Diagram (8-D Package)

Table 1-7. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	No power to the device on side-1. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage may be plausible.	A
OUTA	2	OUTA stuck to low. Communication from INA to OUTA corrupted. If INA is driven logic high for extended duration, OUTA stuck low can create short between supply and ground resulting in high current, possible device damage.	A
INB	3	Input signal shorted to ground, so output (OUTB) stuck to low. Communication from INB to OUTB corrupted.	B
GND1	4	Device continues to function as expected. Normal operation.	D
GND2	5	Device continues to function as expected. Normal operation.	D
OUTB	6	OUTB stuck low. Data communication from INB to OUTB lost. If INB is driven logic high for extended duration, OUTB stuck low can create short between supply and ground resulting in high current, possible device damage.	A
INA	7	INA stuck low. Data communication from INA to OUTA lost.	A
V_{CC2}	8	No power to the device on side-2. OUTB pin state undetermined.	B

Table 1-8. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	Operation undetermined. Either device is unpowered and OUTA state undetermined, OUTB=default logic state or through internal ESD diode on INB pin, device can power up if INB is driven to logic high. If INB has current sourcing capability to provide regular operating current of device, ESD diode conducts that current and device damage plausible.	A
OUTA	2	No communication to INA channel possible as OUTA state undetermined.	B
INB	3	No communication to INB channel possible. OUTB stuck to default state (High for ISO7721-Q1 and Low for ISO7721F-Q1).	B
GND1	4	Device unpowered on side1. OUTA state undetermined, OUTB goes to default state (High for ISO7721-Q1 and Low for ISO7721F-Q1).	B
GND2	5	Device unpowered on side-2. OUTA goes to default state (High for ISO7721-Q1 and Low for ISO7721F-Q1), OUTB state undetermined.	B
OUTB	6	State of OUTB undetermined. Data communication from INB to OUTB lost.	B
INA	7	No communication to INA channel possible. OUTA stuck to default state (High for ISO7721-Q1 and Low for ISO7721F-Q1).	B
V_{CC2}	8	Device unpowered on side-2 and state of OUTB undetermined.	B

Table 1-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	OUTA	OUTA stuck high. Communication corrupted for channel A. If INA is driven logic low for extended duration, OUTA stuck high creates short between supply and ground, possible device damage.	A
OUTA	2	INB	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
INB	3	GND1	INB shorted to ground, so output (OUTB) stuck to low. Communication from INB to OUTB corrupted.	B
GND1	4	INB	Already considered in above row.	B
GND2	5	OUTB	OUTB pin stuck low. Communication corrupted. If INB pin is driven high for extended duration, OUTB pin stuck low creates a short between supply and ground with possible device damage.	A
OUTB	6	INA	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
INA	7	V_{CC2}	INA shorted to supply, so output (OUTA) stuck high. Communication from INB to OUTB corrupted.	B
V_{CC2}	8	INA	Already considered in above row.	B

Table 1-10. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	No effect. Normal operation.	D
OUTA	2	OUTA stuck high. If INA is driven low for extended duration, OUTA stuck high creates high current path between supply and ground, with possible device damage.	A
INB	3	INB pin stuck high. Communication corrupted. OUTB stuck high.	B
GND1	4	Device side-1 unpowered. Observe that the absolute maximum ratings for INB/OUTA pins of the device are met, otherwise device damage may be plausible.	A
GND2	5	Device side-2 unpowered. Observe that the absolute maximum ratings for INA/OUTB pins of the device are met, otherwise device damage may be plausible.	A
OUTB	6	OUTB stuck high. Communication disrupted. If INB is low for extended duration, OUTB being stuck high creates a short and can damage the device.	A
INA	7	OUTA stuck high. Communication disrupted.	B

Table 1-10. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC2}	8	No effect. Normal operation.	D

1.4.2 SOIC-16 Package

Figure 1-3 shows the ISO7721/ISO7721-Q1 pin diagram for the 16-DW package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the ISO7721/ISO7721-Q1 datasheet.

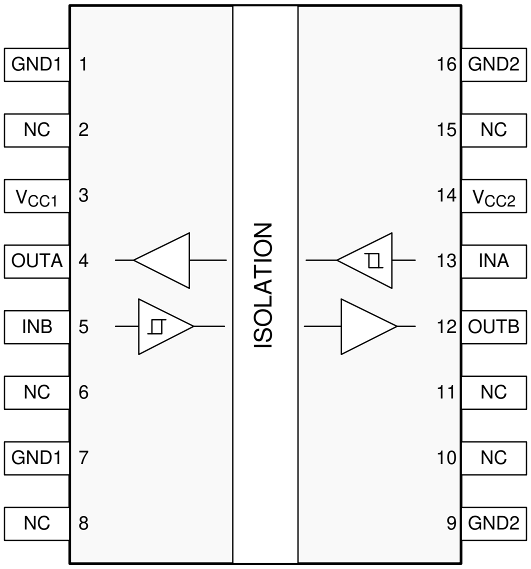

Figure 1-3. Pin Diagram (16-DW Package)

Table 1-11. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND1	1	Device continues to function as expected. Normal operation.	D
NC	2	Device continues to function as expected. Normal operation.	D
V_{CC1}	3	No power to the device on side-1. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage may be plausible.	A
OUTA	4	OUTA stuck low. Communication from INA to OUTA corrupted. If INA is driven high for extended duration, OUT stuck low creates high current path between supply and ground, possible device damage.	A
INB	5	Input signal INB shorted to ground, so output (OUTB) stuck to low. Communication from INB to OUTB corrupted.	B
NC	6	Device continues to function as expected. Normal operation.	D
GND1	7	Device continues to function as expected. Normal operation.	D
NC	8	Device continues to function as expected. Normal operation.	D
GND2	9	Device continues to function as expected. Normal operation.	D
NC	10	Device continues to function as expected. Normal operation.	D
NC	11	Device continues to function as expected. Normal operation.	D
OUTB	12	OUTB stuck low. Data communication from INB to OUTB lost. Device damage possible if INB is driven high for extended period of time.	A
INA	13	Input signal INA shorted to ground, so output (OUTA) stuck to low. Communication from INA to OUTA corrupted.	B
V_{CC2}	14	No power to the device on side-2. OUTB pin state undetermined.	B
NC	15	Device continues to function as expected. Normal operation.	D
GND2	16	Device continues to function as expected. Normal operation.	D

Table 1-12. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND1	1	Device gets return ground through pin7. Normal operation.	D
NC	2	Device continues to function as expected. Normal operation.	D
V_{CC1}	3	Operation undetermined. Either device is unpowered and OUTA undetermined state, OUTB=default logic state or through internal ESD diode on INB pin, device can power up if INB is driven to logic high. If INB has current sourcing capability to provide regular operating current of device, ESD diode conducts that current and device damage plausible.	A
OUTA	4	Channel A communication corrupted. OUTA state undetermined.	B
INB	5	No communication to channel B possible. OUTB stuck to default state (High for ISO7721-Q1 and Low for ISO7721F-Q1).	B
NC	6	Device continues to function as expected. Normal operation.	D
GND1	7	Device gets return ground through pin1. Normal operation.	D
NC	8	Device gets return ground through pin1. Normal operation.	D
GND2	9	Device gets return ground through pin1. Normal operation.	D
NC	10	Device gets return ground through pin1. Normal operation.	D
NC	11	Device gets return ground through pin1. Normal operation.	D
OUTB	12	State of OUTB undetermined. No data communication possible on channel B.	B
INA	13	No communication possible to channel A. OUTA stuck to default state (High for ISO7721-Q1 and Low for ISO7721F-Q1).	B
V_{CC2}	14	Device unpowered and state of OUTB undetermined.	B
NC	15	Device continues to function as expected. Normal operation.	D
GND2	16	Device gets return ground through pin9. Normal operation.	D

Table 1-13. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND1	1	NC	Device continues to function as expected. Normal operation.	D
NC	2	V_{CC1}	Device continues to function as expected. Normal operation.	D
V_{CC1}	3	OUTA	OUTA stuck high. Communication to INA channel corrupted. If INA is driven low for extended duration, OUT stuck high creates a high current path between supply and ground, possible device damage.	A
OUTA	4	INB	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage	A
INB	5	NC	Device continues to function as expected. Normal operation.	D
NC	6	GND1	Device continues to function as expected. Normal operation.	D
GND1	7	NC	Device continues to function as expected. Normal operation.	D
NC	8	GND1	Already considered above.	D
GND2	9	NC	Device continues to function as expected. Normal operation.	D
NC	10	NC	Device continues to function as expected. Normal operation.	D
NC	11	OUTB	Device continues to function as expected. Normal operation.	D
OUTB	12	INA	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
INA	13	V_{CC2}	INA stuck high. Communication disrupted. OUTA stuck high.	A
V_{CC2}	14	NC	Device continues to function as expected. Normal operation.	D
NC	15	GND2	Device continues to function as expected. Normal operation.	D
GND2	16	NC	Already considered above.	D

Table 1-14. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND1	1	This can create potential difference between pin1 and pin7, causing high current to flow in device and potential device damage.	A
NC	2	Device continues to function as expected. Normal operation.	D
V_{CC1}	3	Device continues to function as expected. Normal operation.	D
OUTA	4	OUTA stuck high. Communication corrupted. If INA is driven logic low for extended duration, OUTA stuck high can create high current path between supply and ground, possible device damage.	A
INB	5	INB pin stuck high. Communication corrupted. OUTB state high.	B
NC	6	Device continues to function as expected. Normal operation.	D
GND1	7	This can create potential difference between pin1 and pin7, causing high current to flow in device and potential device damage.	A
NC	8	Device continues to function as expected. Normal operation.	D
GND2	9	This can create potential difference between pin9 and pin16, causing high current to flow in device and potential device damage.	A
NC	10	Device continues to function as expected. Normal operation.	D
NC	11	Device continues to function as expected. Normal operation.	D
OUTB	12	OUTB stuck high. Communication disrupted. If INB is low for extended duration, OUTB being stuck high creates a short and can damage the device.	A
INA	13	INA pin stuck high. Communication corrupted. OUTA state high.	B
V_{CC2}	14	Device continues to function as expected. Normal operation.	D
NC	15	Device continues to function as expected. Normal operation.	D
GND2	16	This can create potential difference between pin9 and pin16, causing high current to flow in device and potential device damage.	A

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