*Application Note*

# *Comparative Analysis of Two Different Methods for Gate-Drive Current Boosting*

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**ABSTRACT**

Increasing drive current for switching devices is a common requirement in high-power converters. As the size of the switching devices (IGBT, MOSFET) increases, there is a need to drive them with larger current for faster switching. There is also a need to drive multiple devices in parallel to reduce conduction losses at higher currents. TI offers high-current gate drivers with typical 10-A drive strength, such as the UCC5390 and UCC21732, which is sufficient for many high-power modules. In some cases, upwards of 20-A peak current is required and in these cases, external buffers should be used. This decouples the load from the driver integrated circuit (IC) and can provide thermal benefits in addition to optimized switching efficiency for the power switch.

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## Trademarks

# 1 Introduction

This document analyzes two methods to increase the drive current from integrated gate-driver ICs. The performance of both the methods is compared by building boards and testing them at various conditions. These circuits are discussed in further detail in subsequent sections.

# 2 Current Boost With BJT Totem Pole Stage

The most common current-boosting method is the use of an NPN-PNP transistor pair. The gate-drive output from the integrated driver is applied as the base drive for this transistor pair. Figure 2-1 shows the schematic of such a current boost circuit using the isolated gate-driver ISO5852S.

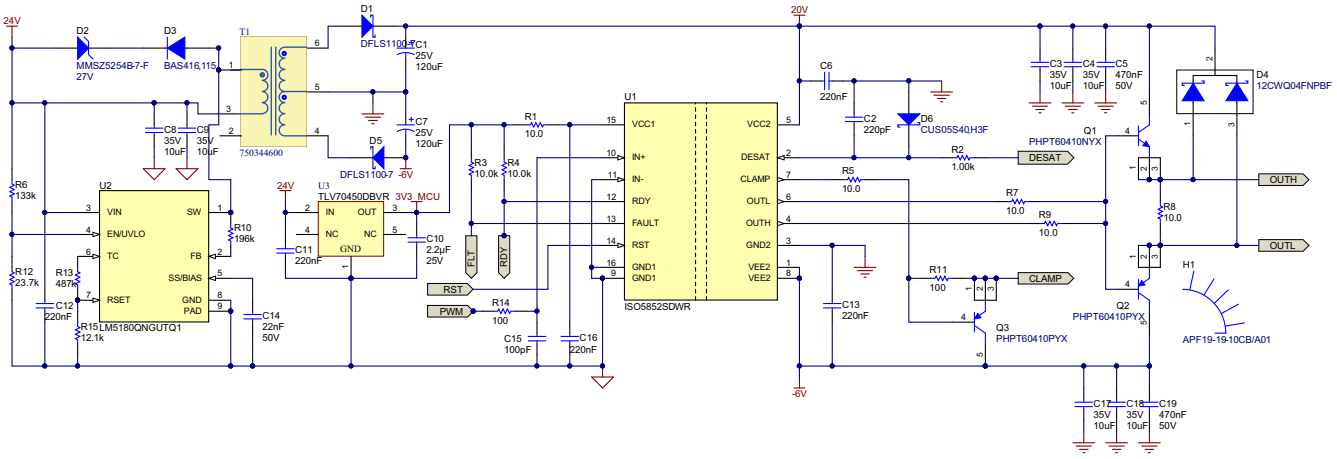



**Figure 2-1. High-Current Gate Driver Using ISO5852S and BJTs**

Signal isolation for the PWM input from MCU is provided by the driver IC itself. The gate-driver IC provides an isolation of 5.7 $kV_{RMS}$ and can source and sink 2.5 and 5 A of current, respectively. Power isolation is achieved by an isolated flyback power supply built around the LM5180 device, a primary side regulated flyback converter with integrated 100-V MOSFET. For input side to output side isolation, a flyback transformer from Wurth Elektronik (part no: 750344600) is used. The use of this controller allows this gate-driver circuit to be compatible with 24-, 15-, or 12-V auxiliary power supplies. The primary (MCU) side of the ISO5852S can either be powered using the MCU power supply itself (by depopulating U3 and connecting the MCU supply to 3V3_MCU input), or by a 5-V supply generated by a TLV70450 LDO from the auxiliary power source. The gate-drive power generated by the flyback power stage is suitable for both IGBTs and SiC MOSFETs, as it is has dual outputs of +20 V and –6 V. The RST and PWM signals are from the MCU – PWM is the drive signal and RST (active low) is used for resetting the gate driver after clearing a fault event due to the DESAT pin detecting a short circuit of the power switch. About 10-ns noise filtering is provided on the PWM input. The FLT and RDY signals are status indication signals back to the MCU – FLT indicating by active low a fault situation detected by the gate driver and RDY indicating by active high that the driver is ready to receive PWM input.

On the output side, the NPN and PNP totem pole stage does current amplification. The BJTs that were used for current amplification were PHPT60410NYX and PHPT60410PYX, with a 20-A peak current rating. Because of the use of transistors in the active region, the drive outputs will be reduced by 0.7 V–0.8 V from the power-supply rails. This is not a significant problem with such high drive voltages. Also, adding a resistor between the base and emitter of the external transistors will allow the output voltage to reach the rail voltages. The ISO5852S device has an internal Miller clamp capable of sinking 2.5 A, typical. This pin can also be configured to drive an external PNP transistor for an external clamp. Using an external clamp increases the effectiveness by positioning it much closer to the gate of the power switch. With a sufficiently high negative bias of –6 V, it is not essential to use the Miller clamp, but is included as additional safety and also for demonstration of current boosting of the Miller clamp output. The diodes in D4 protect the output transistors from overvoltage during transient situations.

The DESAT overcurrent protection function in ISO5852S is maintained in this gate driver without any change from the recommended sensing circuit. However, due to the current boosting on the output drive, the slow turn-off DESAT protection might not work well without some modification of the circuit. The R16 – C20 network will ensure that the drive current during a DESAT event will be diverted away from the base of Q2 for the

required amount of turn-off time. The values of these components can be calculated using Equation 1 and Equation 2:

$$C = \left(I \times T_{off}\right) / \left(V_P - V_N\right) \quad (1)$$

where

- I is the value of the internal current source which is 130 mA
- $T_{off}$ is the desired turn-off time
- $V_P$ is the positive drive voltage
- $V_N$ is the negative drive voltage

The value of R16 can be estimated using the inequality in Equation 2:

$$R > \left(V_P - V_N\right) / 5 \quad (2)$$

## 3 Current Boost With Saturated MOSFET Totem Pole Stage

An alternate scheme for drive current boosting is given in Figure 3-1. Two N-channel MOSFETs are used as current boosting devices. As they are operated as saturated switches, the drive current is only limited by the on-time resistance and hence can achieve much higher current levels.

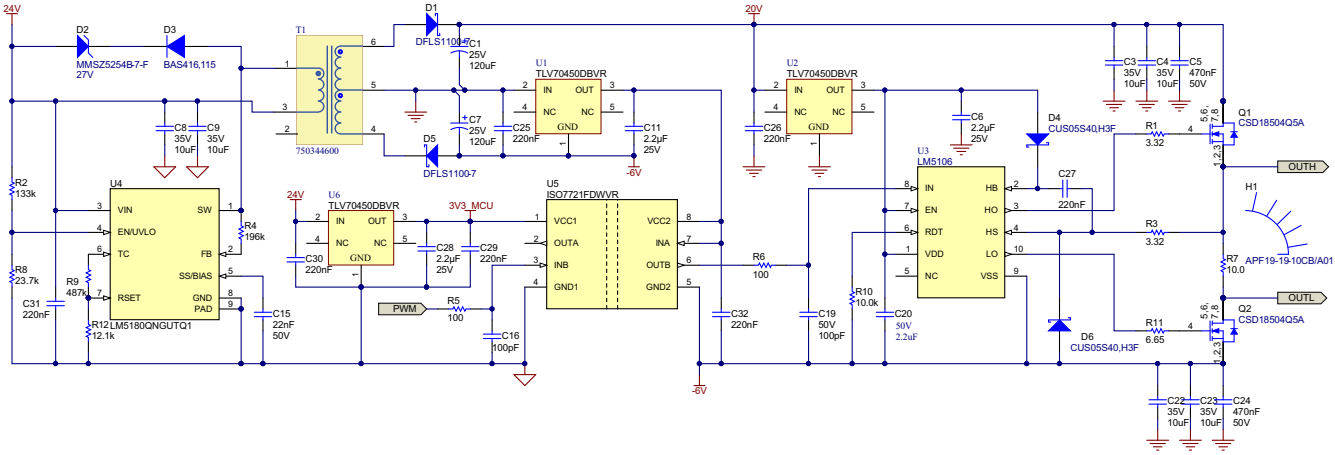



**Figure 3-1. High-Current Gate Driver Using LM5106 and MOSFETs**

In this circuit, signal isolation is provided by a digital isolator (ISO7721). To drive the driver MOSFETs, a low-voltage half-bridge driver IC (LM5106) is used. The power supply is the same as the previous circuit. However, a couple more LDOs are required to power the secondary side of the digital isolator and the half-bridge driver. The secondary side of the digital isolator is referred to the –6-V negative drive supply. So to power this side, a 5-V supply referred to this level is needed. This is provided by a 5-V LDO connected to the secondary return. For the gate-drive voltage for the driver MOSFETs (and the half bridge driver), a voltage of around 10 V (referred to the negative drive supply) is needed. This is generated by another 5-V LDO referred to the secondary return. This gives a total of 11 V (5 V from the LDO and 6 V from the negative drive supply) referred to as the negative drive supply.

For half-bridge drivers, typically two PWMs are required – the main PWM for the upper MOSFET and a complementary PWM for the lower MOSFET. However, the LM5106 half-bridge driver can generate the complementary signal internally with a dead-time determined by a programming resistor. This saves the need to have the complementary signal generated by the MCU. However, the half-bridge driver will need a level-shifted drive voltage to address the upper MOSFET. In this circuit, this voltage is provided by a bootstrap circuit comprising of D4, C27 , and R3 under the assumption that there is sufficient on-time for the lower MOSFET to charge. With the component values used in this circuit, the typical charging time is under 1 µs. That means, for PWM inputs with less than 1-µs off-time, the bootstrap capacitor might not be able to charge to the full supply voltage. Also, for low PWM frequencies (below a few 100 Hz), the bootstrap capacitor will not be able to hold the charge for the entire cycle. If such conditions are expected to be present, it is recommended to use an additional

isolated supply to power the high-side – this can easily be generated by adding one more winding on the flyback power supply used. This will allow even 100% duty cycle operation.

The upper-side MOSFET is switched in accordance with the PWM input, while the lower MOSFET is switched based on the complementary of the PWM input resulting in output drive with the same polarity as the input PWM. As the drive current can be as high as 100 A, sufficient decoupling is required on the positive and negative drive-supply rails. If needed, additional capacitors can be added externally. This high peak current-drive capability is not required for most power devices, but by utilizing FETs of this power level, thermal dissipation can be greatly reduced when driving with peak currents of 20 A or higher. The peak current can be limited by using the external gate resistor since too high a peak current can result in undesirable ringing at the gate and uncontrolled slew rates of the power switch.

## 4 Implementation Details

Both the circuits were made in the same size: 50-mm length, 30-mm width, and 13-mm overall height. They have the same external pin-out, allowing them to be tested under the same conditions. There are 10-mm high heatsinks attached to the board to cool the drive BJTs and MOSFETs. These boards are made in such a way that they can be mounted very close to the device being driven. The pictures of the boards follow:

The board in Figure 4-1 is referred to as *Board 1*, hereafter.

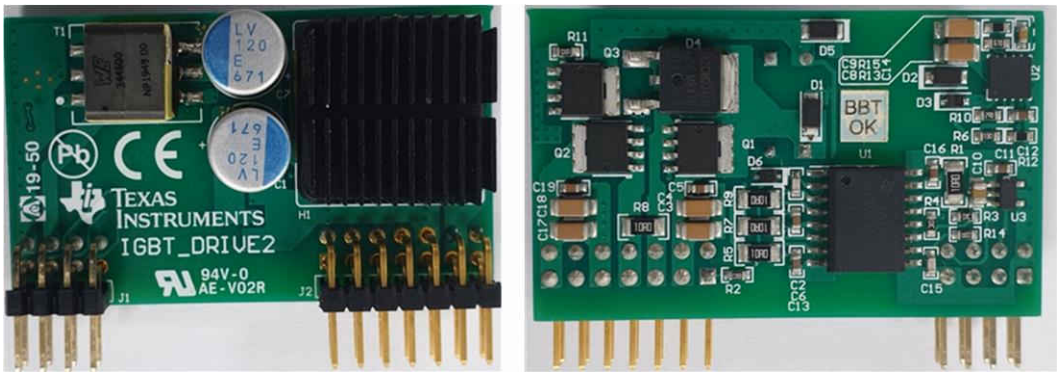



**Figure 4-1. High-Current Gate-Driver Board Using ISO5852S and BJTs (Top and Bottom View)**

The board in Figure 4-2 is referred to as *Board 2*, hereafter.

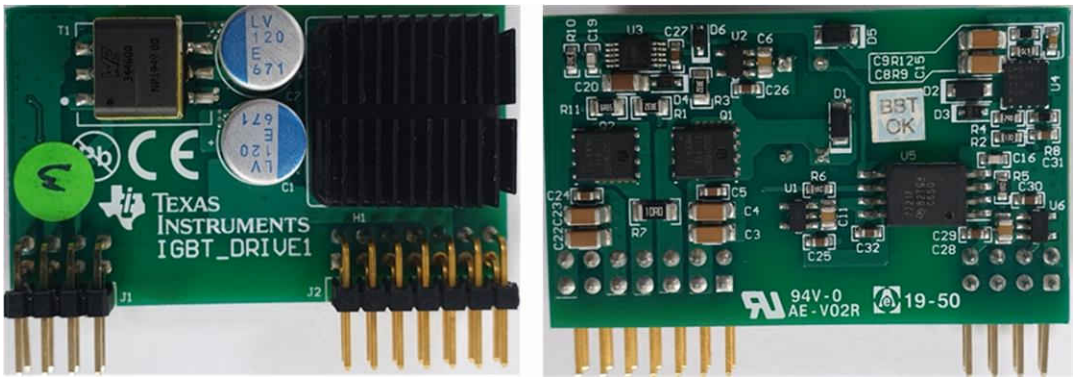



**Figure 4-2. High-Current Gate Driver Board Using LM5106 and MOSFETs (Top and Bottom View)**

## 5 Performance Results

Drive current: driving a total load of around 1 µF. Magenta – drive current, Green – drive voltage.

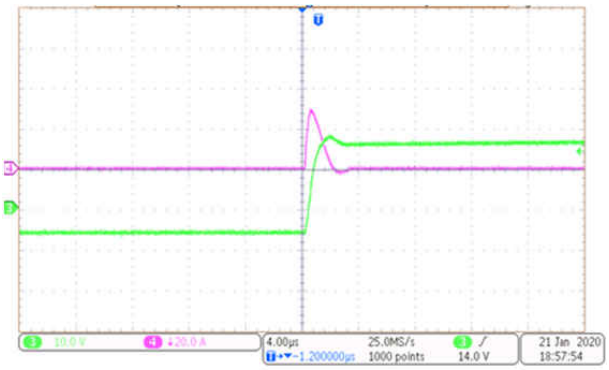


**Figure 5-1. Drive-Current Waveform (Board 1)**

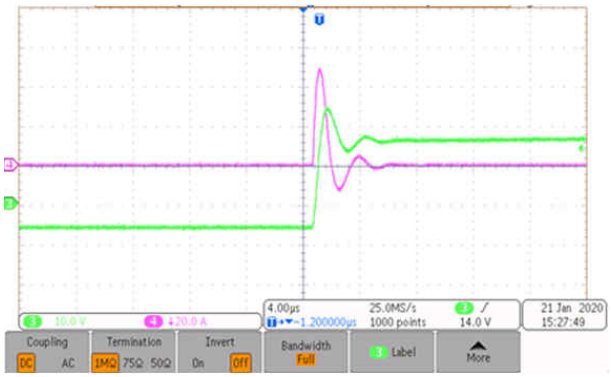
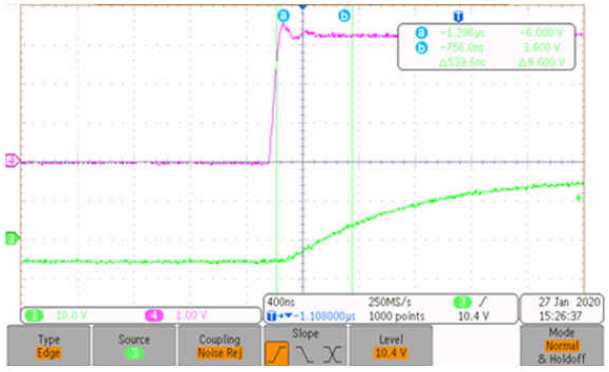


**Figure 5-2. Drive-Current Waveform (Board 2)**

*Board 1* gives about 30-A drive current and *Board 2* is able to give above 50 A.

Board 1 propagation delay: driving a total load of 470 nF. Magenta – PWM input, Green – drive voltage.



$V_{IH}$ is the logic threshold of the input PWM and the $V_{TH}$ is the FET typical threshold.

**Figure 5-3. Board 1 Propagation Delay $V_{IH}$ to $V_{TH}$**

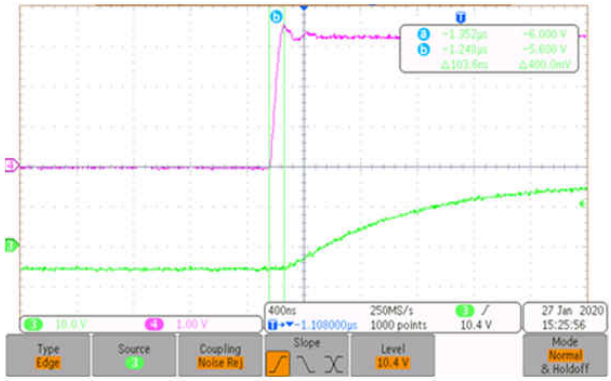


**Figure 5-4. Board 1 Propagation Delay Start of Input to Start of Output**

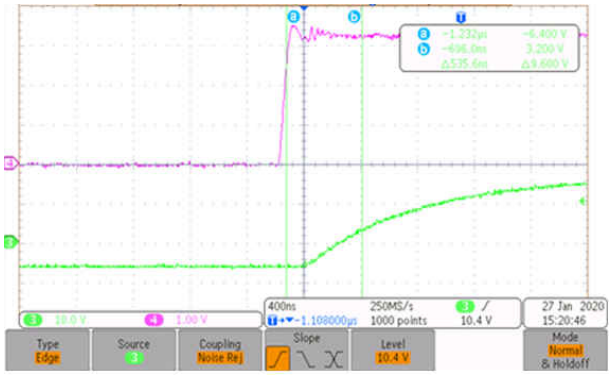


**Figure 5-5. Board 2 Propagation Delay $V_{IH}$ to $V_{TH}$**

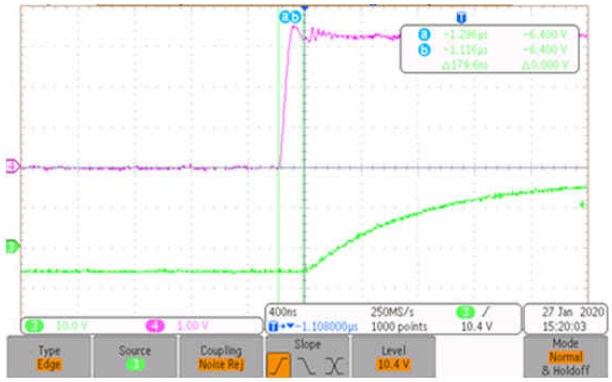


**Figure 5-6. Board 2 Propagation Delay Start to Start**

Both the boards have around 540-ns propagation delay from $V_{IH}$ to $V_{TH}$. However, measured from the start of waveforms, *Board 1* has a lower delay of 100 ns compared to 180 ns for *Board 2*.

The thermal performance of the boards with no airflow while driving 1 µF at 10 kHz is shown in Figure 5-7 and Figure 5-8.

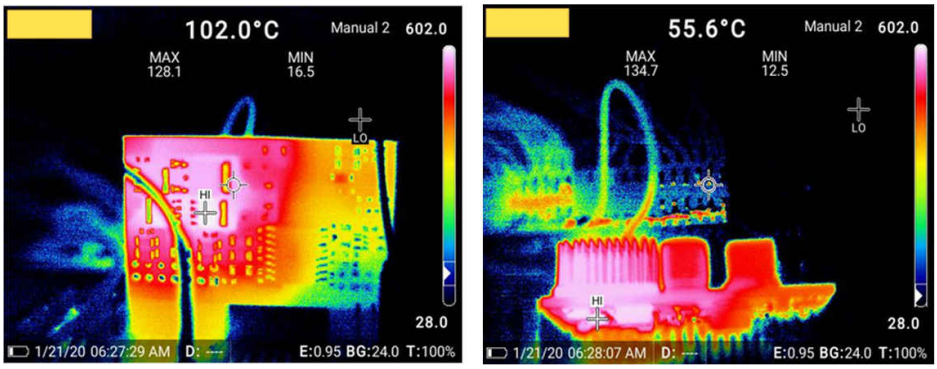



**Figure 5-7. Board 1 Thermal Profile**

Figure 5-7 shows that the driver transistors are the hottest components and that the temperature goes as high as 135°C.

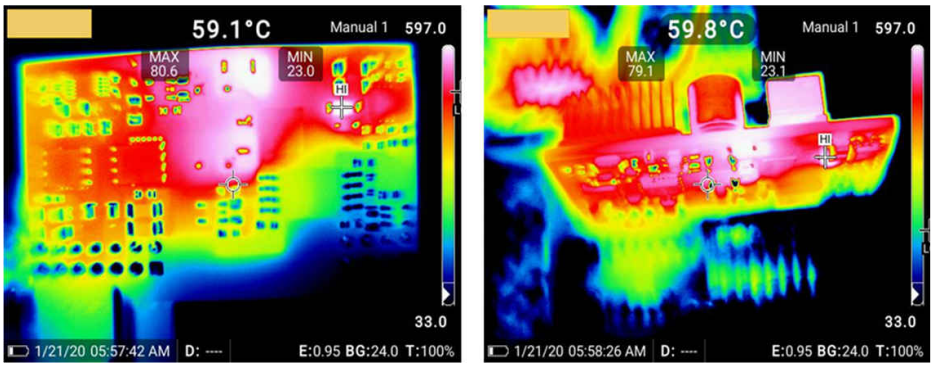



**Figure 5-8. Board 2 Thermal Profile**

Figure 5-8 shows that the flyback converter IC is the hottest component with a temperature of around 80°C.

*Board 2* bootstrap (C27) voltage variation while driving 1 µF. Red – PWM input, Blue – C27 voltage, Green – output voltage across the 1-µF capacitor.

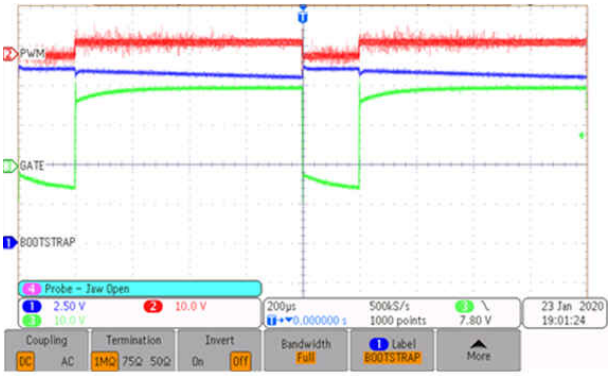



**Figure 5-9. Bootstrap Voltage at 1 kHz**

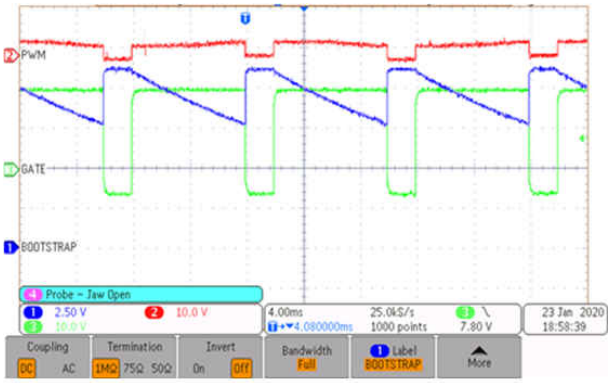



**Figure 5-10. Bootstrap Voltage at 100 Hz**

There is very little droop in voltage at 1 kHz. Even at 100 Hz, the minimum voltage is maintained above 7.5 V at 80% duty cycle and hence no noticeable effect in the output waveform.

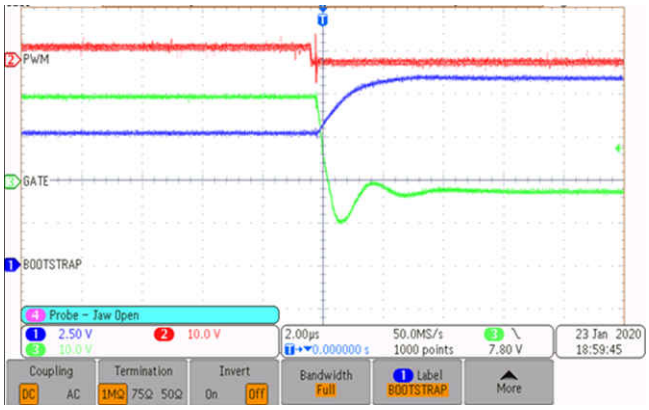



**Figure 5-11. Bootstrap Voltage Charging Time**

The bootstrap capacitor gets charged in around 1 µs.

*Board 1* Miller clamping: Driving 470 nF with 18 Ω. Magenta – clamp current, Green – drive voltage.

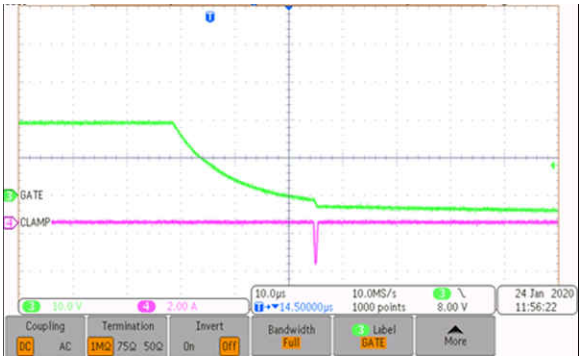



**Figure 5-12. Miller Clamp Current**

The Miller clamp is able to hold the gate voltage close to the negative bus in spite of the high gate-drive impedance. Gate-drive resistance is intentionally made around 18 Ω to push some current into the clamp. For effectiveness of the Miller clamp, the transistor must be placed as close as possible to the gate and source terminals.

*Board 1* DESAT slow turn-off operation while driving 470 nF with 1-Ω drive resistance. Blue – PWM input, Green – Output voltage, Magenta – DESAT input.

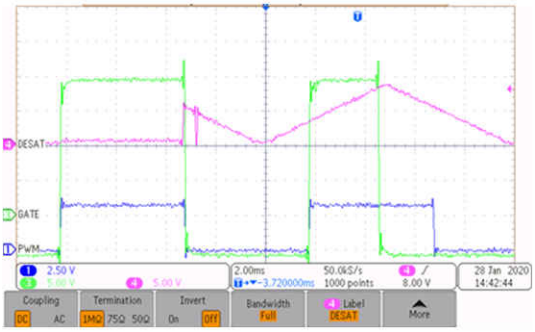



**Figure 5-13. DESAT Turn off Without R16 and C20**

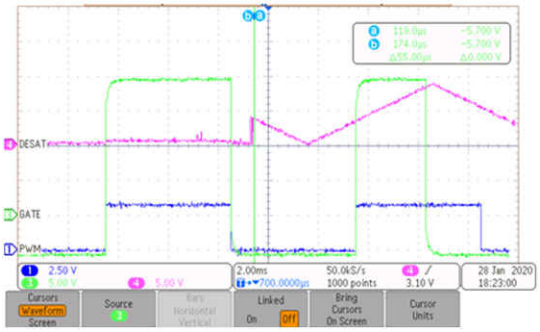



**Figure 5-14. DESAT Turn off With R16 and C20**

The R-C network at the OUTL pin helps restore slow turn-off operation with external current boosting.

## 6 Comparison of the Two Methods

Both the methods are capable of providing current-boosted drive output. However, the saturated MOSFET-based drive can achieve much higher drive currents due to the lower impedance offered by the saturated MOSFETs. The BJT drive is relatively higher impedance, as they operate in active region and hence will not be able to reach the drive current levels achieved by the other method while using devices of comparable size. Also, the availability of high-current BJT devices is far less compared to high-current MOSFETs. While driving similar devices, the BJT-based driver will dissipate more power in it than the MOSFET based driver, due to the relatively higher impedance of the BJT. The relatively cooler operating temperature increases the reliability of the MOSFET-based driver .

The major advantage with the BJT-based driver is the simplicity of the circuit. It has fewer components and a much simpler power scheme. It also allows easy extension of the features built inside the driver IC like DESAT protection, Miller clamp , and so forth. For the MOSFET-based driver, these functions should be built externally, if needed. So the overall size of the gate driver will increase due to external DESAT protection and clamping circuitry. However, the MOSFET-based driver gives more flexibility for isolation, as it depends on the transformer and digital isolator only. There are more devices to choose from in case of specific isolation requirements.

## 7 Conclusion

Boards were designed and made for BJT-based and MOSFET-based current-boosted gate drivers and their comparative performance was evaluated. The MOSFET based saturated drive was found to be able to give more drive current and was relatively cooler while driving similar loads. The BJT drive was simpler with the ability to extend the protection features offered by the gate driver IC used. The BJT drive also provides a much higher level of integration.

## 8 References


- Texas Instruments, *LM5106 100-V Half-Bridge Gate Driver With Programmable Dead-Time Data Sheet*
- Texas Instruments, *ISO5852S High-CMTI 2.5-A and 5-A Reinforced Isolated IGBT, MOSFET Gate Driver With Split Outputs and Active Protection Features Data Sheet*


## 9 Revision History

| Changes from Revision * (February 2020) to Revision A (February 2022) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the publication | 1 |

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