Application Report
SLLA427–November 2018

TLINx441 LDO Performance

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ABSTRACT

To understand if a low dropout (LDO) voltage regulator supports the system requirements several factors have to be considered. Integrated LDOs present opportunities for small board space while at the same time presenting challenges for the system design. Package, ambient temperature input and output voltages must be considered when designing the system. These contribute to the junction temperature of the semiconductor (LDO) which determines the performance of the LDO. This application note considers the performance of the LDO that is integrated in the TLIN1441x and TLIN2441x devices in relationship to these factors.

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Trademarks

1 Introduction

What is a Low Drop Out (LDO) voltage regulator? In the simplest terms, it is a component that takes a higher input direct current (DC) voltage and reduces this DC voltage to a level that the circuit requires. An example of this would be a 3.3 V regulator that is powered off of a 5 V system. There are many parameters that could be considered when evaluating a LDO. Examples are, but not limited too; input voltage, output voltage and current requirements. LDOs are offered as a stand alone device or integrated into a device that has more functionality. The TLINx441x family of devices has integrated an LDO and is the basis for this application note.

2 Device Overview

The TLINx441(x) family is a Local Area Network (LIN) system basis chip (SBC) supporting 12 V (TLIN1441x) and 24 V (TLIN2441x) battery automotive systems integrated with a LIN transceiver as well as other functionality. The (x) determines the devices's Low Drop Out (LDO) voltage regulator output voltage: (3) represents 3.3 V ± 2% and (5) represents 5 V ± 2%. The TLIN1441x device can source up to 125 mA of current as long as certain factors are understood and designed properly. The TLIN2441x device can source up to 70 mA of current as long as certain constraints are understood and designed for. These factors include package, supply voltage and ambient temperature.

3 Device Description

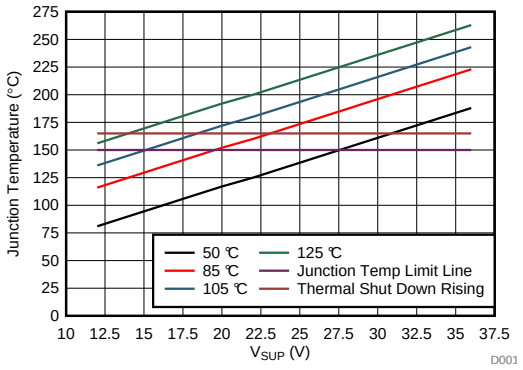
The supply voltage, V_{SUP}, and ambient temperature, T_A, will be considered first. As the output voltage, V_{CC}, is fixed. A change in V_{SUP} can impact the overall LDO performance and thermal considerations. The equation ($V_{SUP} – V_{CC}$) x I_{CC} is used to arrive at the power consumption of the device. As an example, if V_{SUP} = 28 V, V_{CC} = 3.3 V and I_{CC} = 100 mA, then the power consumption of the device is 2.47 W. This is realized as heat which impacts the junction temperature, T_J, of the silicon. This power number is part of the evaluation to determine the impact to overall performance. Temperature is the next consideration as higher the ambient temperature means higher junction temperature. The theoretical junction temperature can be calculated by taking the calculated power and multiplying it with the package thermal resistance and adding the ambient temperature. Selecting the correct thermal resistance is application dependant but in TLINx441x applications, $R_{\Theta JA}$ is the parameter of focus. In the example above, the junction temperature is calculated using $R_{\Theta JA}$ = 35.5 °C/W. $R_{\Theta JA}$ is the thermal resistance between the package and the ambient air surrounding the package, measured in change in degrees celcius per watt of power dissipation. For the TLINx441xDMT package the value is 35.5 ˚C/W. At the time of publishing, this is the best in the industry for this type of package (VSON) and allows for higher performance whether that is supporting higher currents with higher V_{SUP} or T_A.

$$(P \times R_{\Theta JA}) + T_A = T_J \rightarrow (2.47W \times 35.5\ °C/W) + 85\ °C = 172.7\ °C \quad (1)$$

This is above the junction temperature of 150°C and results in a thermal shut down event as the T_J is above 165 °C. Using $R_{\Theta JB}$ = 11.8 °C/W provides a junction temperature of 114.2 °C as an example of how proper thermal considerations can improve the performance of the LDO. $R_{\Theta JA}$ and $R_{\Theta JB}$ are package and board design dependent and shown here for a high-k board. If best thermal practices are followed with airflow and heatsinks for the board; using $R_{\Theta JB}$ provides higher performance but is beyond the scope of this application note. $R_{\Theta JB}$ is the thermal resistance between the silicon junction and the board. Packages with thermal pads tend to have better $R_{\Theta JB}$ performance than packages without.

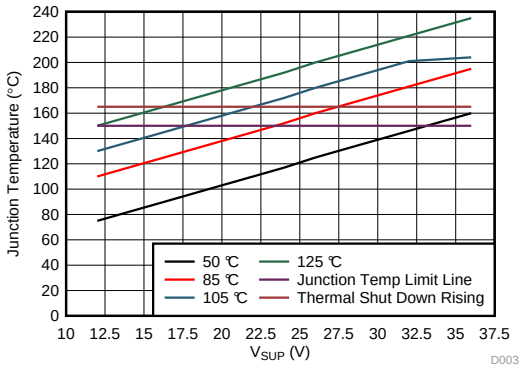
When considering packages, the thermal characteristics are important to consider. Considering the list of thermal information in a data sheet one can see up to four thermal resistance parameters. These are important to understand as they contribute to the equation used to determine the silicon junction temperature which predicts when the device may reach the thermal shut down limit. For the TLINx441x devices, the thermal resistance $R_{\Theta JA}$ is considered. In automotive applications, the expectations is that the ambient temperature saturates the system; thus the $R_{\Theta JA}$ is used to understand how the device performs.

The TLINx441x is designed with a maximum junction temperature of 150 ˚C and has a built in thermal shut down feature at 165 ˚C. The junction temperature is the temperature the CMOS transistor's junction should not exceed to meet long term reliability. The thermal shut down feature exists to protect the device incase an external fault causes the junction temperature to rise enough to damage the device. The three following charts show the theoretical junction temperature based upon V_{SUP}, Ambient Temperature and amount of current being sourced. The graphs have two lines that represent the maximum junction temperature, dark green, and the rising temperature thermal shut down point, dark red. When the device is consistently operating in the temperature region between the maximum T_J and thermal shut down the life of the device may shorten. The application design should keep the junction temperature below the green line, maximum T_J. Figure 1 to Figure 3 show the theoretical performance with the 5 V output based upon a 125 mA, 100 mA and 70 mA output load. Figure 4 to Figure 6 show the same data but are based upon a 3.3 V output.



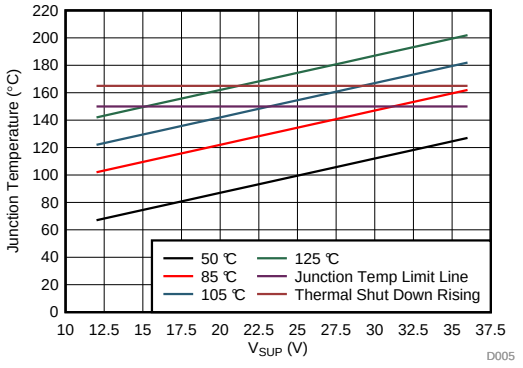
V_{CC} = 5 V at 125 mA Load

Figure 1. Junction Temperature vs Ambient Temperature



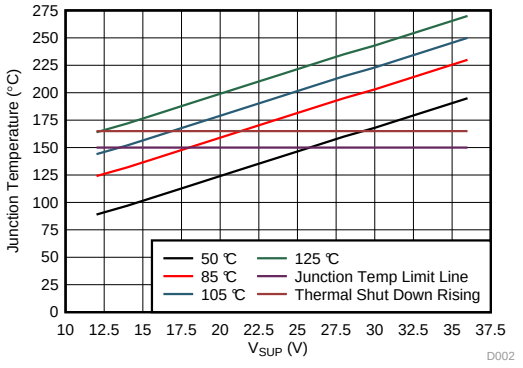
V_{CC} = 5 V at 100 mA Load

Figure 2. Junction Temperature vs V_{SUP} vs Ambient Temperature



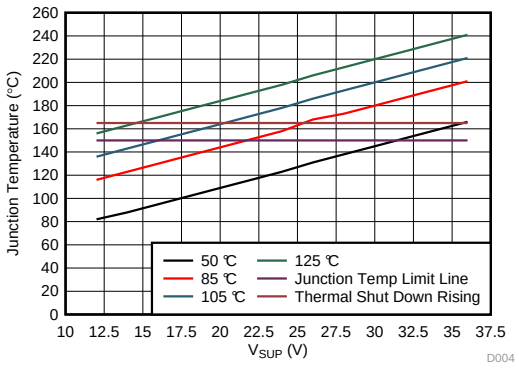
V_{CC} = 5 V at 70 mA Load

Figure 3. Junction Temperature vs V_{SUP} vs Ambient Temperature



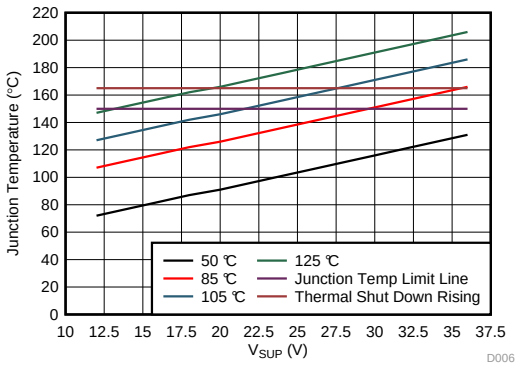
V_{CC} = 3.3 V at 125 mA Load

Figure 4. Junction Temperature vs V_{SUP} vs Ambient Temperature



V_{CC} = 3.3 V at 100 mA Load

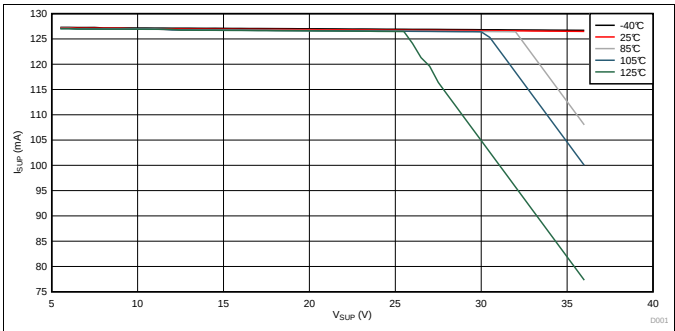
Figure 5. Junction Temperature vs V_{SUP} vs Ambient Temperature



V_{CC} = 3.3 V at 70 mA Load

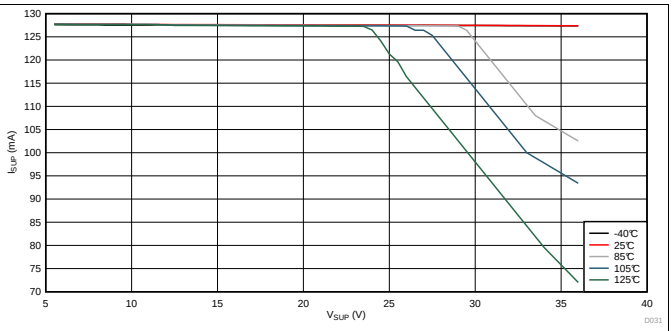
Figure 6. Junction Temperature vs V_{SUP} vs Ambient Temperature

The actual performance of the LDO aligns with the expected theoretical values when using the evaluation module and a thermal stream. Figure 7 to Figure 14 provide the data based upon 125 mA, 100 mA and 70 mA load for both 5 V and 3.3 V.



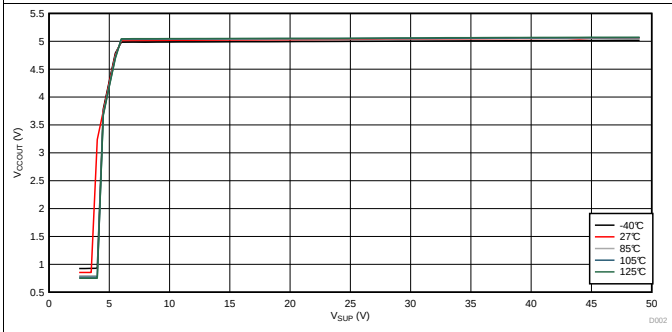
V_{CC} = 5 V

Figure 7. LDO Output Current vs V_{SUP} vs Ambient Temperature



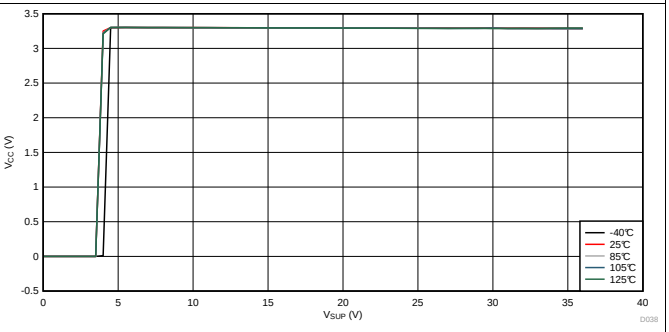
V_{CC} = 3.3 V

Figure 8. LDO Output Current vs V_{SUP} vs Ambient Temperature



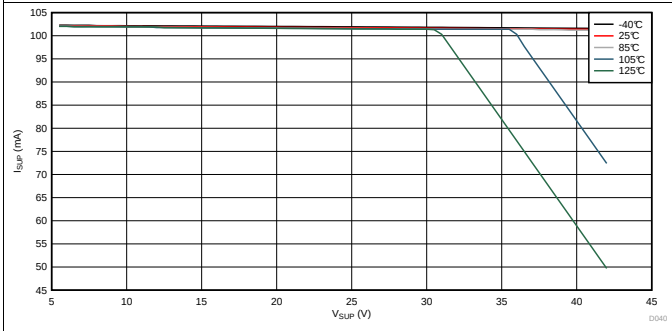
I_{SUP} Load = 125 mA

Figure 9. LDO Output Voltage vs V_{SUP} vs Ambient Temperature



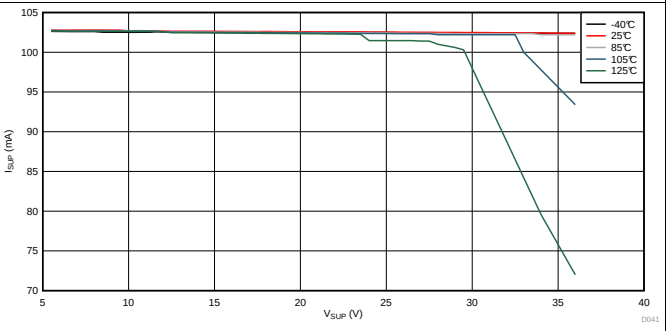
I_{SUP} Load = 125 mA

Figure 10. LDO Output Voltage vs V_{SUP} vs Ambient Temperature



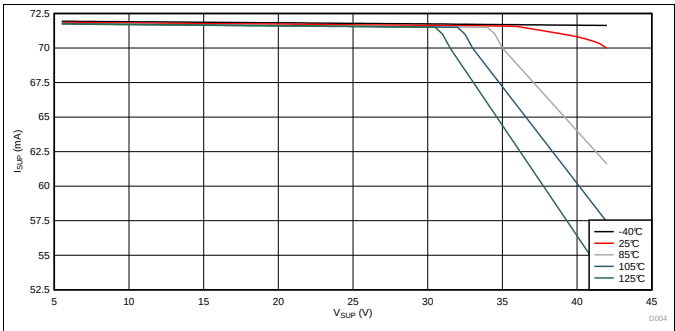
V_{CC} = 5 V

Figure 11. LDO Output Current vs V_{SUP} vs Ambient Temperature



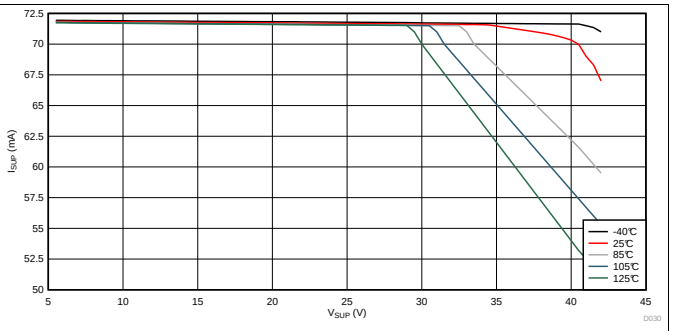
V_{CC} = 3.3 V

Figure 12. LDO Output Current vs V_{SUP} vs Ambient Temperature



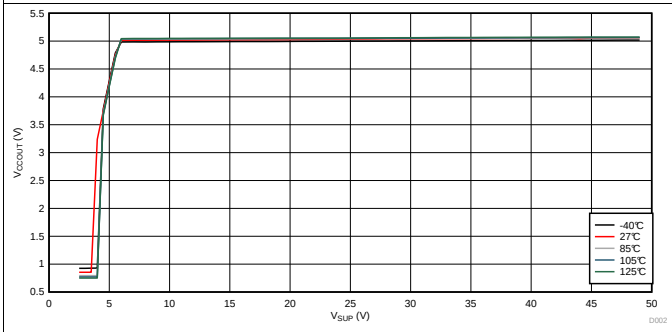
V_{CC} = 5 V

Figure 13. LDO Output Current vs V_{SUP} vs Ambient Temperature



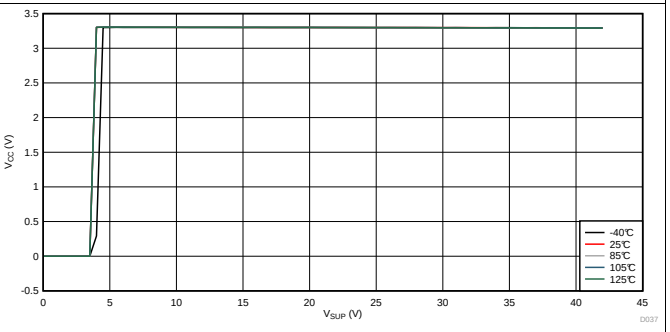
V_{CC} = 3.3 V

Figure 14. LDO Output Current vs V_{SUP} vs Ambient Temperature



I_{SUP} Load = 70 mA

Figure 15. LDO Output Voltage vs V_{SUP} vs Ambient Temperature



I_{SUP} Load = 70 mA

Figure 16. LDO Output Voltage vs V_{SUP} vs Ambient Temperature

One area of interest is what happens during V_{SUP} ramp down between 1 V and regulated 5.5 V when the device is in sleep mode. Does the LDO consume significant current during this ramp? The reason for this interest is to make sure the device does not consume enough current to drain the battery if a system level failure happens and V_{SUP} is stuck in this range. Figure 17 and Figure 18 shows the ramp down performance of the TLINx441x device when in sleep mode for the 5 V and 3.3 V LDOs.

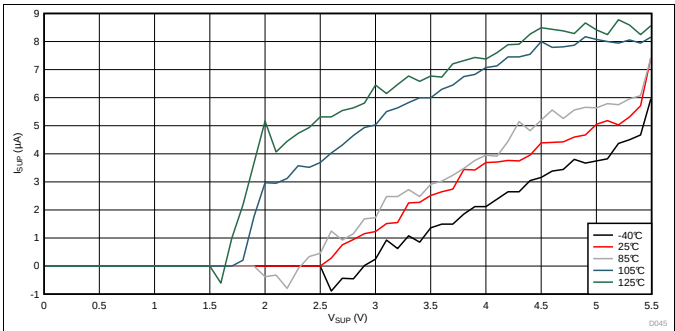


Figure 17. 5 V LDO Sleep Mode Ramp Down

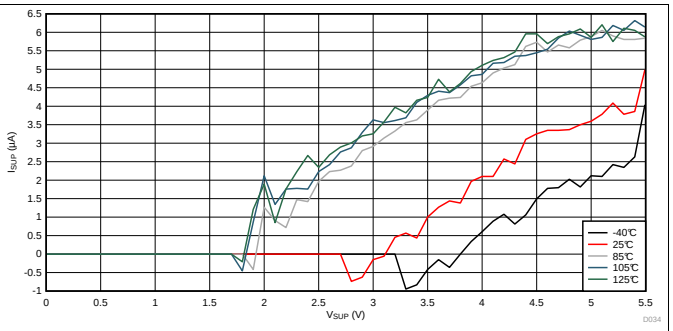


Figure 18. 3.3 V LDO Sleep Mode Ramp Down

4 Summary

When considering the LDO sourcing requirements in a system many factors need to be considered. For the best performance, special care must be taken to design a board and system that meets the thermal needs. For devices that have thermal pads, the thermal pad must be soldered to a good solid ground plan. Based upon the data, Table 1 provides typical performance for specific data points.

Table 1. TLINx441x Family Performance

Device	V_{CC} (V)	I_{CC} (mA)	V_{SUP} (V)	T_A (°C)
TLIN14413DMT-Q1	3.3	125	14	85
TLIN14415DMT-Q1	5	125	14	85
TLIN24413DMT-Q1	3.3	70	28	85
TLIN24415DMT-Q1	5	70	31	85

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