

# TUSB213 Schematic Checklist

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## ABSTRACT

This application report is for the TUSB213, a USB High-Speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel. TUSB213 is agnostic to USB Low Speed (LS) and Full Speed (FS) signals while USB High Speed (HS) signals are compensated. This schematic checklist provides a brief explanation of each device pin and the recommended configuration of the device pin for default operation. Use this information to check the connectivity for each TUSB213 on a system schematic.

This document is intended to aid design at the system level for general applications but should not be the only resource used. In addition to this list, customers are advised to use the information in the TUSB213 datasheet, TUSB213 EVM User's Guide and associated documents to gain a full understanding of device functionality.

Note: This device needs to have its thermal pad connected to ground for RGY packages. Project collateral discussed in this application report can be downloaded from the following URL: [www.ti.com/lit/zip/SLLA393](http://www.ti.com/lit/zip/SLLA393).

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## 1 TUSB213 Schematic Checklist

**Table 1. TUSB213 Schematic Checklist**

Pin Name	Pin Number	Pin Description	Recommendation
VCC	12	3.3-V power	Parallel array of 1 $\mu$ F and 0.1 $\mu$ F capacitors on VCC to GND
VREG	8	1.8-V LDO output.	Connect a 0.1 $\mu$ F capacitor between VREG and GND
GND	7	Ground	GND must be connected to GROUND
RSTN	14	Device disable/enable.	Connect a 0.1 $\mu$ F capacitor between RSTN and GND. A second option is to control this pin externally. The device should not be enabled until the power on ramp has settled to 3 V or higher to ensure a correct power on reset of the digital circuitry.
EQ	1	USB High Speed boost select via external pull down resistor. Sampled upon power up, no real time changes.	PD resistor connected to the EQ pin, the value options are 160 W (max), 1.4 - 2 K $\Omega$ , 3.7 - 3.9 K $\Omega$ or 6 K $\Omega$ (min) for the EQ levels 0 - 3 respectively. See Table 3 in datasheet.
D1P	10	USB High Speed positive port.	Make sure the USB2 signals DP/DM polarity corresponds to the pins D <sub>x</sub> P/D <sub>x</sub> M respectively.
D1M	9	USB High Speed negative port.	Make sure the USB2 signals DP/DM polarity corresponds to the pins D <sub>x</sub> P/D <sub>x</sub> M respectively.
D2P	7	USB High Speed positive port.	Make sure the USB2 signals DP/DM polarity corresponds to the pins D <sub>x</sub> P/D <sub>x</sub> M respectively.
D2M	8	USB High Speed negative port.	Make sure the USB2 signals DP/DM polarity corresponds to the pins D <sub>x</sub> P/D <sub>x</sub> M respectively.
SDA	11	In I2C Mode, Bidirectional I2C data pin. In Non-I2C Mode, no function.	I2C Mode: 4.7 k $\Omega$ (5%) pull-up resistor required for I2C Mode. Non-I2C Mode: This pin must be floating or connected to ground.
SCL/CD	13	In I2C Mode, I2C clock pin. In Non - I2C mode, Flag indicating that a USB device is attached.	I2C mode: I2C clock pin [I2C address = 0x2C], 4.7 k $\Omega$ (5%) pull-up resistor required for I2C Mode. Non-I2C mode: CD can be connected to a LED in series with a resistor to GND. If no LED is needed, the pin can be left unconnected.
DC_BOOST/ENA_HS	9	I2C Mode: Pin is reserved for testing. Non-I2C Mode: DC Boost set before reset then becomes flag indicating that channel is in High Speed mode.	Ensure DC_BOOST/ENA_HS upon reset has correct input voltage for desired DC gain. This can be set via resistive divider with pull-down and pull-up (to 3.3 V) resistors between 22 k $\Omega$ to 47 k $\Omega$ . See Table 3 in TUSB213 datasheet. After reset pin outputs flag indicating High Speed mode.
NC	2,3	N/A	Leave unconnected.

Notes: Common mode chokes placed as close as possible to the USB connectors. Verify the pinout of the USB connectors. Verify pin-out of TUSB213 matches datasheet. Always refer to the datasheet of this device for complete descriptions of each pin

## 2 References

- [TUSB213 USB 2.0 High Speed Signal Conditioner Datasheet](#)
- [TUSB213EVM Users Guide](#)

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