Application Report
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Troubleshooting SN65DSI8x - Tips and Tricks

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ABSTRACT

The purpose of this document is to provide guidelines for debugging common SN65DSI83, SN65DSI84, and SN65DSI85 issues, and to also answer the most frequently asked questions about these devices.

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Trademarks

1 General FAQ

1.
- Q: Does the SN65DSI8x support command mode?

  A: No. The SN65DSI8x also does not support the DSI Virtual capability or reverse direction (peripheral to processor) transmissions.

2.
- Q: How can I turn the ULPS mode on?

  A: The Ultra-Low Power State entry command should be issued by the host per the MIPI DPHY spec definition. Please refer to the MIPI DPHY specification for the details of the ULPS entry and exit procedure.

3.
- Q: Is it possible to use the SN65DSI8x as a CSI receiver?

  A: No.

4.
- Q: In the datasheet, what does R_{LVDS_DIS} stand for?

  A: This value represents the pull-down value of the LVDS output not enabled by the configuration registers. For example, if the LVDS_LINK_CFG is set to 1, the LVDS CHB outputs are not enabled but they will have the pull-downs of about ~1K.

5.
- Q: Are there any layout suggestions for LVDS trace length?

  A: The trace length is heavily dependent upon the PCB routing/cables used. The typical drive strength is dependent upon the VOD setting and the termination. Please note that the SN65DSI8x has an option for either 100 or 200-Ω near end termination. Although the example used in this app note is for a different TI LVDS device, the general recommendation remains the same for the

performance of the LVDS system design: Performance of LVDS With Different Cables.

6.

- Q: Does TI have a reference driver code for the SN65DSI8x?

  A: Under request, we can provide a sample code that we use in Linux for OMAP to configure the DSI8x. This code executes the initialization sequence for the SN65DSI8x and configures the device registers. This is only a sample code; the user must modify the values in the code to match the required resolution, video format, etc. This sample code can be used to configure the DSi8x devices from Linux. The DSI interface is fully supported on the OMAP mainline Linux kernel in the following address: sample code.

NOTE: The initialization sequence in the sample code may be outdated and not match the datasheet. The initialization sequence in the datasheet must be followed.

7.

- Q: Does the SN65DSI8x support my panel resolution?

  A: To determine whether or not your resolution will be supported depends on the clock frequency. The equation for the LVDS CLK frequency is:

$$\text{LVDSCLK} = \text{Hactive} \times \text{Vactive} \times \text{Frame Rate} \times (1 + \%\text{blanking}) \tag{1}$$

  where Hactive are the active horizontal pixels and Vactive are the active vertical pixels. For example a 1920 x 1080 resolution panel has Hactive = 1920 and Vactive = 1080. The minimum DSICLK frequency to meet the line time requirement is:

$$\text{DSICLK} = \frac{\text{LVDSCLK} \times \text{bpp}}{2 \times \#\ \text{of DSI DataLanes}} \tag{2}$$

  The LVDS CLK frequency range for the SN65DSI8x is 25 - 154 MHz, and the DSI CLK frequency range is 40 - 500 MHz.

  Equivalently, if the total horizontal and total vertical pixels (active pixels plus the blanking pixels) are known then the frequency is just:

$$\text{LVDSCLK} = \text{Htotal} \times \text{Vtotal} \times \text{Frame Rate} \tag{3}$$

  The panel datasheet should have the Htotal and Vtotal information.

  So for example, you are using a 1920 x 1200 resolution panel with a frame rate of 60 Hz, 10% blanking, and 24 bpp color. Also, assume that you will use 4 DSI data lanes. Using the equations above, the required LVDS CLK frequency is 153.6 MHz and the minimum DSI CLK frequency is 460.8 MHz. Since these are within the clock frequency specifications in the datasheet, this resolution is supported.

  For dual-channel interfaces, you need to divide the LVDS CLK frequency equation by 2 (since there are 2 LVDS output clocks). For example, you are using a 2560 x 1600 resolution panel with a frame rate of 60 Hz, 10% blanking and 24 bpp color. Let's also assume that 8 DSI data lanes will be used (4 data lanes per channel) so the SN65DSI85 is required. With the equations above, the required LVDS clock frequency per channel is 135 MHz and the minimum DSI CLK frequency per channel is 406 MHz. Since these are within the clock frequency specifications in the datasheet, this resolution is supported.

8.

- Q: How do I calculate the line time?

  A: The line time is calculated by the DSI-Tuner tool in the "Outputs" window. Alternatively, you can calculate the line time manually with the equation:

$$\text{Line Time} = \frac{\text{Htotal}}{\text{LVDSCLK}} \tag{4}$$

  and:

$$\text{Line Time} = \frac{\text{Htotal} \times \text{bpp}}{2 \times \#\ \text{of DSI DataLanes} \times \text{DSICLK}} \tag{5}$$

2 Debug Procedure

2.1 Register Configuration

Make sure to use the DSI-Tuner tool to generate the video timing and the configuration register values required to transfer the DSI data to the LVDS panel. If part of the window of the tool is cut off, then please post to our forum on https://e2e.ti.com/ to get a modified version of the tool.

Make sure to not modify any reserved or undefined bit fields (e.g. bits 7 and 6:5 in address 0x10) as this may result in incorrect device operation.

2.2 Schematic/Layout

For best schematic/layout practices, reference the EVM and Hardware Implementation Guide.

2.3 Initialization Sequence

It is very important that the initialization sequence specified in the datasheet is implemented correctly. If it is not followed then it is very likely that the SN65DSI8x will get into undesirable states and not operate correctly.

2.4 Test Pattern

Check to see if the test pattern can be displayed correctly to help isolate the issue. The test pattern does not use the DSI input (except the DSI CLK as an option). If the test pattern can be correctly displayed but the display is incorrect during normal operation, then likely there is an issue on the DSI side (signal integrity, etc.). The test pattern output can be configured with the DSI-Tuner. There are also instructions in the datasheet. The test pattern should look like this:

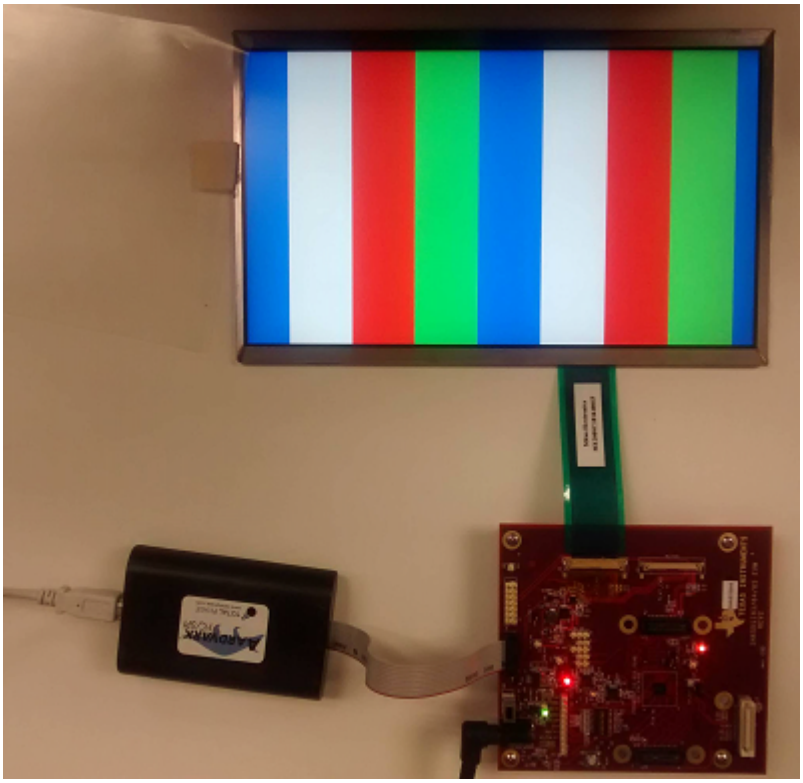

Figure 1. Test Pattern

2.5 No Output Video

1. Make sure the initialization sequence is implemented correctly.
2. Check to see if the test pattern can be displayed correctly. If it does not look like the test pattern in Figure 1 then most likely something is wrong with either the register configuration or the video timing parameters.
3. Verify that the timing configuration provided by the DSI video source is correct per the recommendation generated by the DSI-Tuner tool. Video input timing, register configuration, and the panel timing requirements all have to match up for the video streaming to work without errors.
   - The LVDS output timing programmed in CSR MUST match the LVDS panel specification.
   - There is no need to match horizontal or vertical video CSR configurations to the DSI input values except for the CH*_ACTIVE_LINE_LENGTH (number of active pixel). In other words, as long as the line time is met, the blanking parameters on the LVDS side do not need to exactly match the blanking parameters on the DSI side. However, the active pixels always need to match.
   - The number of active pixels presented on DSI_Input MUST match the programmed value in the CSR:CH*_ACTIVE_LINE_LENGTH_LOW/HIGH.
4. The line time (horizontal sync to the next horizontal sync) on the input must match the line time on the LVDS interface.
   - The DSI8x does not realign timing, so if the line time is different then there will be issues.
   - Even if the DSI source is outputting streams in a burst manner, it is important for the DSI source to fill in the rest of the line time with blanking packets (or LP11) to meet the line time requirement.
   - The line time is calculated by the DSI-Tuner tool in the “Outputs” window, and is the total amount (including blanking) of horizontal pixels divided by the LVDS clock frequency.
   - If the line time is measured to be smaller than what the tool generates, then the rest of the line time must be filled in with blanking packets or by driving LP11 power state.
   - If the line time is measured to be larger than what the tool generates, then it’s likely the minimum DSI CLK frequency is not being met, so the DSI CLK frequency needs to be increased.
5. Check that the actual number of active DSI data lanes matches the SN65DSI8x register configuration.
6. Check for signal integrity issues on the DSI CLK and HS data lanes. Also, check for any irregularities with the LVDS CLK output.
7. Check that the DSI_CLK range register is programmed to match the actual DSI CLK rate. Check if the LVDS CLK frequency is correct.
8. Check that VCORE is 1.1V. VCORE is an output that requires a 1uF capacitor to ground and must measure 1.1V for proper operation (see datasheet for more details).

There are also error reporting registers that the system software can read to help with system debug. The error status registers are at offset 0xE5 and/or 0xE6. Individual error conditions at address 0xE5 and/or 0xE6 can be reported via IRQ pulses by enabling the corresponding error status bits at offset 0xE1 and/or 0xE2. Refer to the datasheet for details in the IRQ operation and the error reporting mechanism.

3 References

Reference the following applications notes for additional resources to help with your design:

- Hardware Implementation Guide
- DSI-Tuner Guide
- EVM
- MIPI DSI and D-PHY specification

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